Biomedical Ultrasound: Fundamentals of Imaging and Micromachined Transducers

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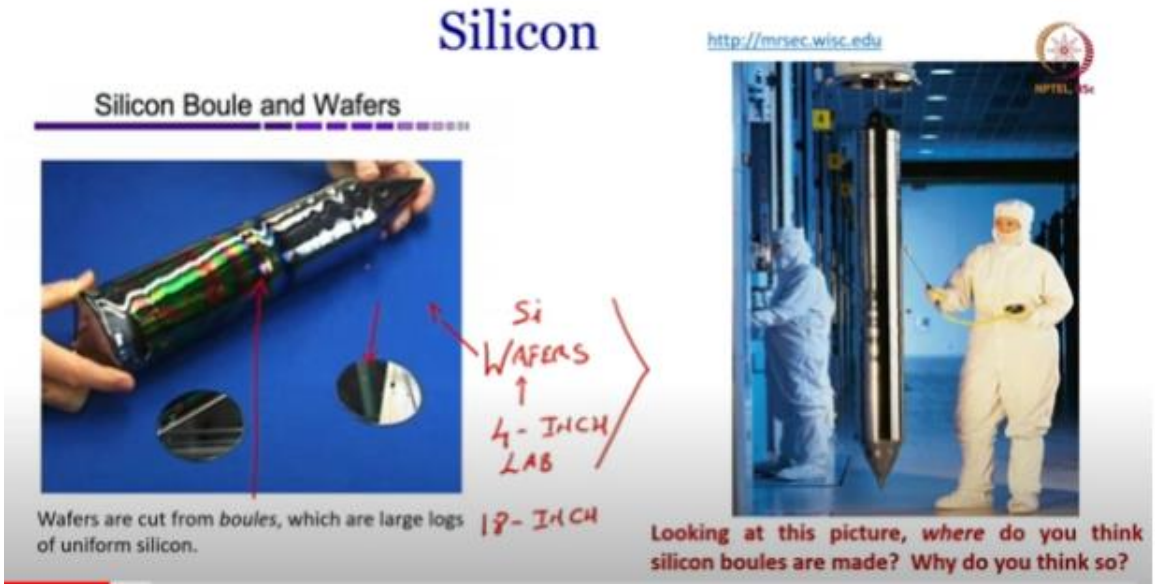
Lecture: 13
Silicon and Silicon Dioxide

Hello and welcome to this lecture, we will be talking about the substrate that is primarily used for ultrasound transducer fabrication. So, this substrate is silicon and 90% of the ICs or integrated circuits that are manufactured today is using this substrate. Now for fabricating ultrasound transducers we start with silicon and then grow silicon dioxide. Silicon being a semiconductor and silicon dioxide being an insulator is a combination of both of the technologies. We will be looking at how to fabricate a silicon wafer and how to manufacture the silicon wafer from the foundry and then how to grow silicon dioxide on the silicon wafer in the labs.

There are techniques which will be learning through this course for example, we look at the physical vapor deposition techniques, the chemical vapor deposition techniques, the micro machining techniques both bulk micro machining and surface micro machining technique. We also look at the wet etching and dry etching techniques and then finally we will see how you can use the combination of all of those along with photolithography which is the heart of the micro fabrication. And we will then see how to utilize the understanding from all these lectures. to fabricate a ultrasound transducer. And we will be focusing on piezoelectric micromachine ultrasound transducer and there are lot of applications of this particular transducer right from the healthcare to the infrastructures (understanding the health of infrastructure) then in the automotive industry.

Let us start understanding silicon and silicon dioxide. If you see the left image on the slide below, it shows the wafer that are are cut from the boules. Boules are large log of uniform silicon. So, the question comes: how we can fabricate this kind of log of silicon and what process techniques are there to form the wafers that we are going to use.



So, when I say silicon wafers and we are going to use 4 inch wafers, this is mostly for the lab environment. If you go to industry it would be 18 inch wafers as well. Now, we will also see how silicon wafer is fabricated or how it is diced or cut from this large log of uniform silicon. We also have to understand that given a silicon wafer what is the crystal orientation of this wafer. Is it 100, 111 or is it 110 just by looking at it. So, we will understand how we can identify the kind of silicon wafer and also whether it is an extrinsic silicon or it is an intrinsic silicon. Also in extrinsic silicon whether it is n type or p type. So, we should know all these things before we fabricate anything.

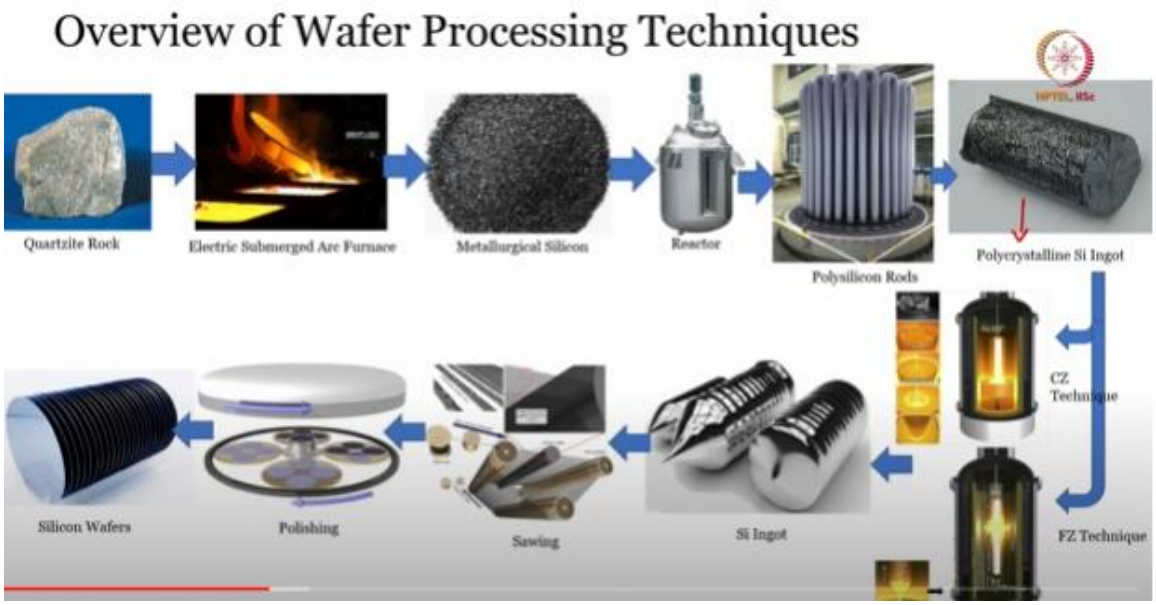
The next question here is that looking at this picture where do you think silicon boules are made and why do you think so that is a question.

Why is all this gowning required? This is called personal protective equipment and also called the clean room gowns. So, the long cylinder you see there is a silicon boule and then the engineer is wearing all the PPEs and and checking the silicon boule. The question is, where do you think silicon boule are made? So, the answer would be that it should be in a clean room or foundry environment.

We are not going into details about how the clean rooms are developed or designed, but in general you should know what the clean rooms class can be. So, the class of clean room can be class 10000, class 1000, class 100, class 10, or class 1. As you go towards lower class that means class 1 from the higher class like class 10000, the cleanness of the clean room would be better and and in one of the short lecture, I will also explain how one can design or understand the class of a clean room. So the answer to our question would be that the silicon boules are made in clean room foundry.

Now why do you think it is so? The answer is because if you work in a clean room the contamination level reduces significantly and we can get a better undoped silicon wafers. Undoped here means unintentional doped. Intentional doping is fine because we have to create n type or p type. But if the environment has a lot of contaminants it will contaminate the entire process. So, to avoid this contamination we go for the clean room environment.

So, the next slide is the overview of the entire wafer processing technique. We start with the quartzite rock, then we have the electric submerged arc furnace, once it is done we have metallurgical silicon. Once the metallurgical silicon is there we put it in a reactor to form poly silicon rods, and once poly silicon rods gets ready we call as a polycrystalline silicon ingot. Now from polycrystalline we have to make it a single crystal. So, we have two different techniques. One is CZ technique or so, Czochralski technique and second means FZ technique or float zone technique.



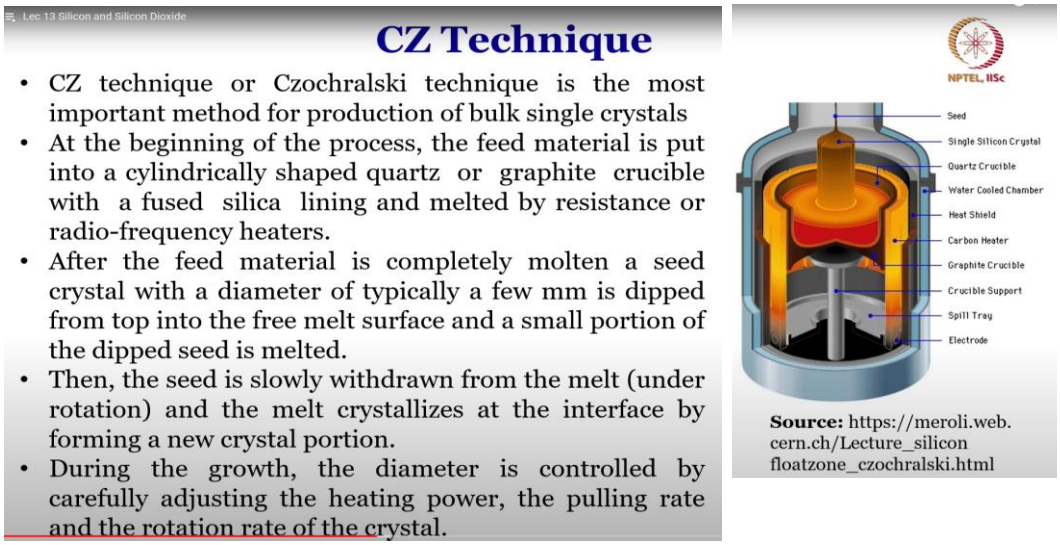
If you open a VLSI technology books you will see these techniques are standard techniques by which we can have a silicon semiconductor grade materials or we can also have much more pure silicon wafers using float zone technique each has its advantages disadvantages we will look into that. When we go for one of the techniques to form a single crystal silicon ingot, the output is our silicon boule or silicon ingot silicon boule or we can say silicon ingot. Now, once you have this, the next step to slice it. Slicing is nothing but sawing using a diamond wires and it is a wire moving in one direction and then another wire moves another direction. Once, we saw the silicon wafers from the silicon boule, we have a silicon which is not polished. Then we go for polishing which involves several techniques: one is lapping followed by chemical and mechanical polishing.

These silicon wafers can be single side polished or double side polished. Single side polished wafer are less costly compared to double side polished wafers. Now if you also have understood this much you might also know that India is now planning to have a semiconductor chip manufacturing foundry. So, we will fabricate different kind of integrated circuits and then we will package it right here. So, it starts from silicon wafer which we get from the silicon foundries. So, silicon foundry to chip manufacturing there is a lot of differences. As far as I understand we are not going to form the silicon foundry, but we are going to have a chip manufacturing units which will fabricate different kind of integrated circuits.

So, I hope that you understand the overview of wafer processing technique. So, with that let us go to the next one. So, let us start with the CZ technique I told you that there are two techniques the first one is CZ technique and second one is float to zone technique.

So, we will go for the first one and the first technique is the CZ technique. CZ technique or Czochralski technique

So, the Czochralski technique is the most important method for production of bulk single crystals and it has multiple processes. So, at the beginning of the process the feed material is put into cylindrically shaped quartz or graphite crucible with a fused silica lining and melted by resistance or radio frequency heaters. So, we focus on this particular paragraph and it says that at the beginning of the process the feed material is put into the cylindrical shaped quartz. This is a seed crystal top. Then there are electrodes which is nothing but the resistance or radio frequency based electrodes. There is a heat shield and then we also have a graphite crucible with a very high melting point.



So, there is also a graphite crucible support and a spill tray in case of spills. And then there are electrodes at the bottom. So, this is the internal structure. From the external perspective we have heat shield to avoid any heat coming outside on the surface of the particular tool. Then we have water cooled chamber which will keep the outside surface cool. We have a quartz crucible inside and a graphite crucible is outside the quartz crucible is inside and then we have single crystal silicon forming. So, what happens is initially the polycrystalline material is fed into this particular quartz or graphite crucible,and then it gets melted. Once it gets melted we insert the seed crystal into this melted region and we slowly pull it up. While we are pulling it we rotate it as well. If our seed crystal is rotated in a clockwise direction then the quartz crucible is rotated in counter clockwise direction or vice versa. That means if the quartz crucible is rotated in clockwise direction the seed crystal is rotated in counter clockwise direction.

So in the beginning of the process this feed crystal or the feed material is put. In this case our feed material would be polysilicon. It is loaded into the crucible and once it is loaded

it is melted using heater. Now we merge seed crystal into this melted zone; we pull it up and then we rotate it like I mentioned.

As the feed crystal is completely molten, a seed crystal with a diameter of typically a few millimeter is dipped from the top into the free melt surface and a small portion of the dipped seed is melted. So, we dip the seed material which is seed crystal and then we slowly withdraw the seed crystal from the melt under rotation and it crystallizes at the interface by forming a new crystal portion. During the growth we can control the diameter by adjusting the heating power or the rate of pull and the rotation rate. Now, with this technique we get electron grade silicon or EGS. The silicon is pulled at an optimized rate that minimizes defects and yields a constant ingot diameter from 4 inch to 18 inch

We can change the diameter by adjusting the power, pull rate and rotation. Impurities can be doped into this silicon ingot intentionally or unintentionally. And the intentional impurities that we dope would create either a N type or a P type silicon.

So, all impurities have different solubilities in solid and in the melt. And if you want to find out an equilibrium segregation coefficient which we denote by Ko then this equilibrium segregation coefficient Ko is defined as a ratio of equilibrium concentration of the impurity in solid(Cs) to that in the liquid (Cl) at the interface and that is given by

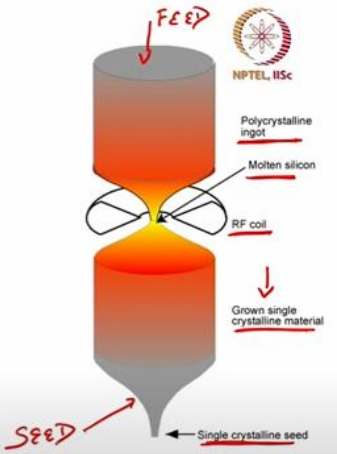
$$Ko = Cs/Cl$$

The impurities segregate to the melt and the melt becomes progressively enriched with impurities as the crystal is being pulled.

Let us go to the FZ technique or float zone technique. So, the float zone technique or FZ technique is based on the zone melting and that was invented by Theuerer in 1962. Here what happens is that there is a polysilicon polycrystalline ingot, there is a molten silicon, there is a radio frequency coil, grown single crystal material and single crystal crystalline seed. So, how does it work and how this single crystal silicon ingot is grown.

FZ Technique

- FZ technique or Float Zone technique based on the zone-melting principle and was invented by Theuerer in 1962. A schematic setup of the process is shown in Figure.
- A melt zone is established between the lower seed material and upper feed material by applying localized heating
- The floating zone is moved along the rod (by means of relative motion of the heating device) in such a way that the crystal grows on the seed (which is below the melt) and simultaneously melting the feed material above the floating zone.
- The seed material, as well as the feed rod, is supported but no container is in contact with the growing crystal or the melt, which is held in place only by surface tension.



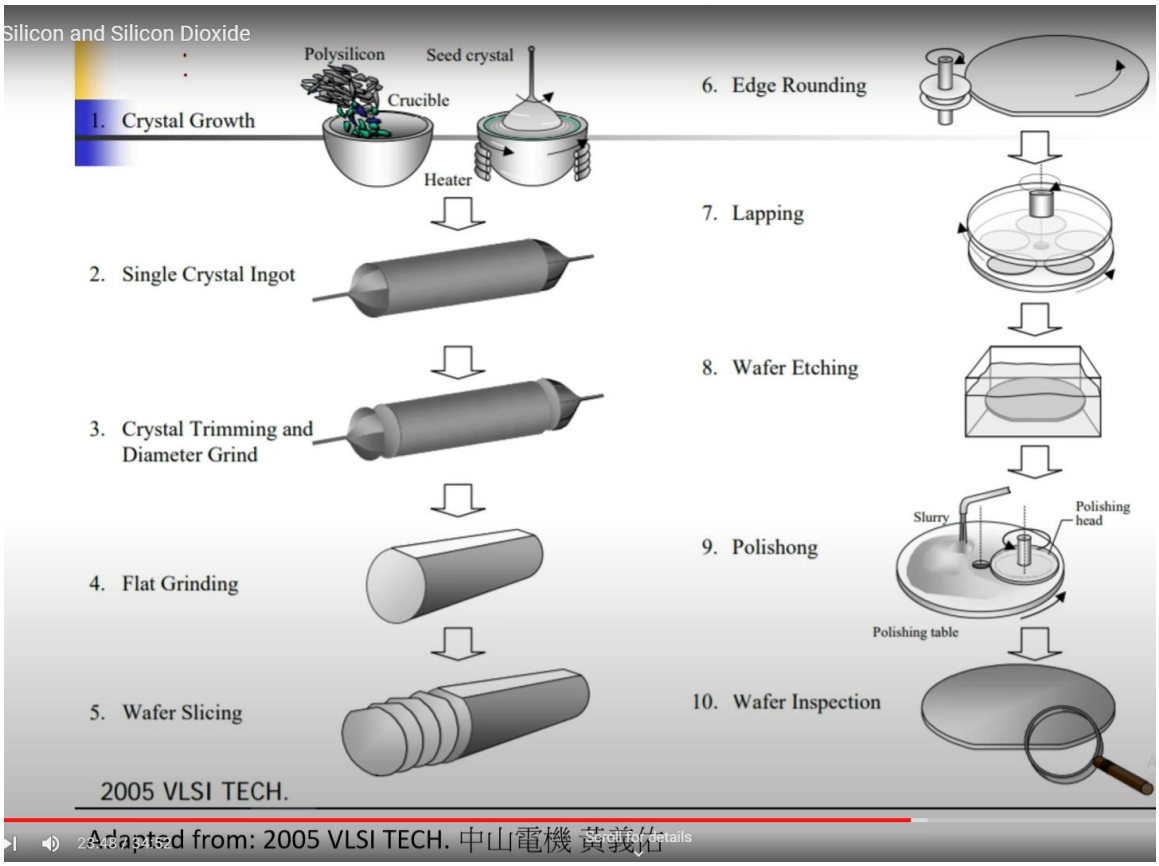
Source: https://www.pveducation.org/pvcdrom/manufacturing-si-cells/float-zone-silicon

A melt zone is established between lower seed material and upper feed material. This is done by heating it the feed material when it comes in contact with the seed material using the radio frequency coil. The floating zone is moved along the rod that means, this will move along the rod in such a way that the crystal grows on the seed. So, that this will keeps on melting and this keeps on fabricating like growing.

The seed material as well as the feed rod is supported but no container is in contact with the growing crystal. In the earlier case if you see there were multiple contacts. Everything is in contact with the crucible and the heater and so on. But in this case we do not have that. So, even though the feed material and seed material is supported there is no contact with the growing crystal and the melt which is held in place only by the surface tension. What is the usefulness of that? The use of this is that the impurities in the molten region tend to stay in molten region rather than be incorporated into solidified region and because of this a very pure single crystal region to be left after the molten region has been passed. And this is because of the impurities will only be in the molten region and when it solidifies the impurities will not come into the solid surface and thus will have a pure single crystal silicon. Due to the difficulty in growing large diameter ingots the FZ wafers are more expensive. float zone crystals are preferably used when low oxygen concentration is an important criteria.

So, now once the silicon ingot is ready, either using our CZ technique or using the float zone technique the next step is, to get the single crystals ingot The next step here is crystal trimming and diameter grinding. So, we trim the crystal from the edges and then we do a flat grinding. All the wafers would possibly have this flat grinding and we call this as a primary flat there are certain wafers which will not have any flats. Most of the

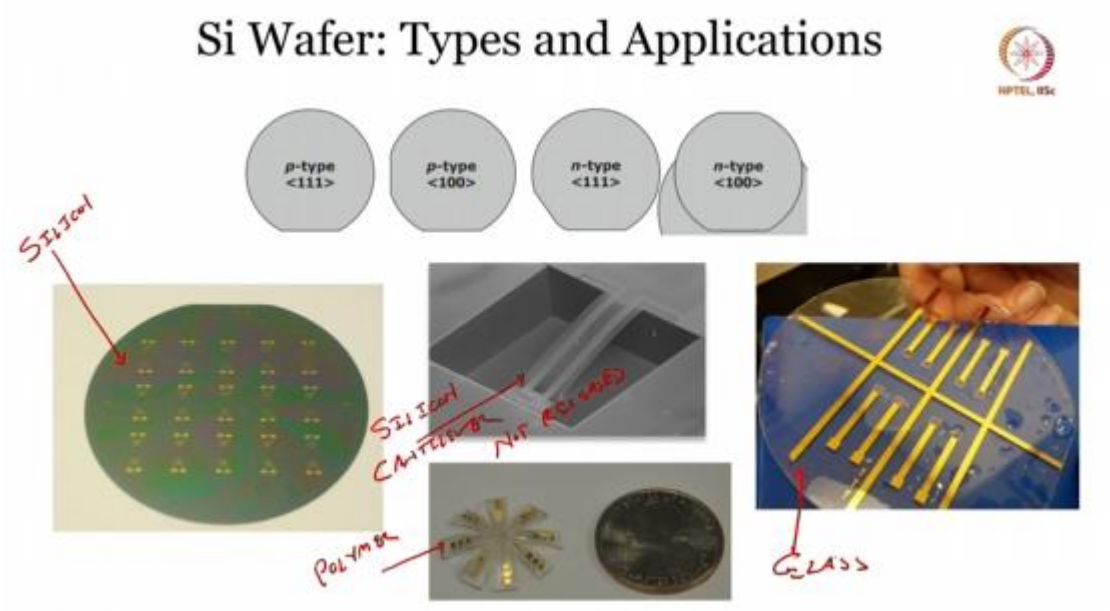
wafers that we are going to use it for our sensors, for MOSFETs, for the transducers those wafers would have primary flat and there is a reason of having primary flat and I will tell you of the reason in few slides.



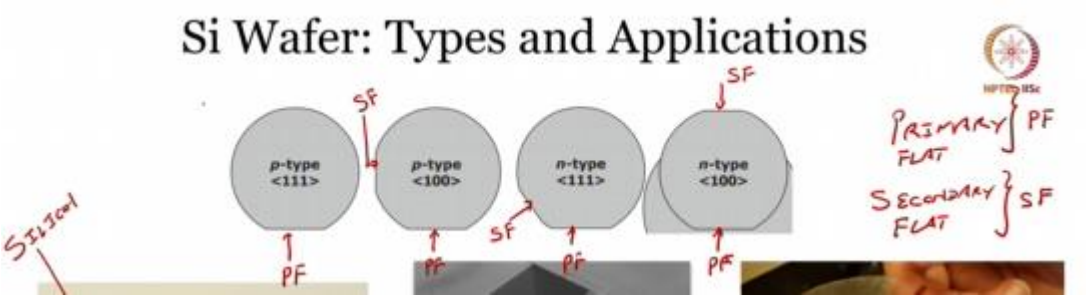
So,after the flat grinding we do wafer slicing. This wafer slicing is done using the sawing and then followed by edge rounding. After that, lapping is done and then you can go for chemical wafer etching followed by polishing called chemical mechanical polishing. There is a slurry, and a polishing head and the wafer is loaded and it is polished. Finally, once it is done we look at the wafer and inspect it for any defects. So, this is the process of creating silicon wafers from single crystal ingot.

So, as you can see here some of the techniques are shown for example, how the diamond coated wire is used on the silicon ingot and how the wafers are sliced and how lapping is done.

Now we move on to Silicon wafer types and applications. So, here what you see on the figure below 3 substrates. There is glass, polymer, and silicon. One of the substrates has a silicon cantilever and the cantilever is not etched, and it is not released. You can see that different substrates can be used for micromachining. So, what is cantilever if you have seen the diving board in swimming pool that is a cantilever the balcony of high rise buildings or any building is a cantilever.



So, the silicon cantilever here is shown to explain that the material which is used as a substrate can be silicon which is semiconductor can be polymer, glass or any other material as well. Now, I told you that the wafers that we will be using would have the one very clear flat which we call as a primary flat and then there is a secondary primary flat, let us we say in short PF, secondary flat SF. So, you see thye PFs and SFs labelled in the figure.



So, if there is only primary flat we call this wafer as P type 111. If the secondary flat is at 90 degree with respect to the primary flat we call P type 100. If the secondary flat is at 45 degree with respect to primary flat we call N type 111. if it is at 180 degree with respect to the primary flat we call this as a N type 100. Now, I hope you appreciate the reason of why primary flat is created. There can be multiple reasons, from aligning point of view and other things, and it is easier for end user to identify the type of the wafer, whether is n type or p type and what orientation of the wafer it is P type 111, P type 100, N type 111 and N type 100.

Now we come to that time in the lecture where I can show you how the wafer looks like. I am going to use a tweezer to hold the wafer. It is absolutely not okay to not use gloves. We have to use gloves. But since this demo I am using a tweezer without gloves. So, for now let us try to hold the wafer and from this wafer can you identify the kind of orientation of this wafer.

This is a primary flat on top and there is secondary flat in the bottom. So, if there is secondary flat with respect to primary flat at 180 degree it is N type 100.

Now, again you can see the mirror like reflection on both sides. So both sides are polished. When the both sides are polished we call it the double side polished wafer.

So, now you would know what is double side wafers what are single side wafers what is a tweezer. Tweezer itself can be of different type to hold the wafer.

So, now what we will do in the next lecture is we will look at silicon dioxide because like I said silicon being a semiconductor, if we start processing and deposit a metal on silicon wafer or if I deposit semiconductor on semiconductor, then the wafer is a short. So, before we go for this process in which we deposit several different kind of metals, I want to first show what are the techniques for silicon dioxide growth. We call it thermal oxidation. So we will see thermal oxidation in the next class till then I hope that now you are clear about how silicon wafer is manufactured and how we can quickly identify what is the type of silicon wafer and what are the orientations of the silicon wafer. So till then take care and I will see you in next class. Bye for now.