Design and Analysis of VLSI Subsystems
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Lecture - 83
Static Timing Analysis - Part 6

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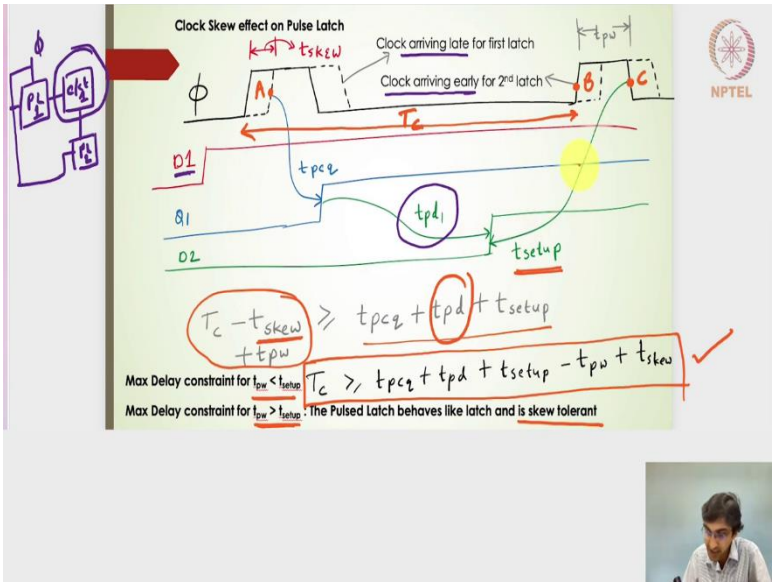

In this particular chapter, we will have a look into this particular lecture we will have a look into the skewing effects on the pulse latch which was left. We had earlier seen the skewing effect on the flip flops as well as on the transparent latches. Let us take this pulse latch design, let me also pick my pointer here.

In this particular timing diagram I have clearly shown the pulse latch. The circuit diagram of this pulse latch remains the same. We will use the pulse latch here PL1 which will go to the combinatorial circuit number 1, and then it will go to the pulse latch number 2. As we know that the clock here will be there and then the same clock is will be going into the pulse latch 2. For finding the maximum delay constraints or establishing the t_{pd} the maximum t_{pd} that needs to be a characterized for the combinatorial circuit number 1.

We always see the worst case condition and then the worst case condition is the PL1 receives the clock which is kind of delayed and the PL2 receives a clock which is kind of early, because we do not know the really the placement of the latches in the chip and that

is where the skewing effect comes into the picture and then the skewed clock characteristics, if it is available we will consider the worst case condition.

Here in the clock designs I have drawn the skewed effect of the clock. Here the t_{skew} is kind of characterized and then made available to us. If I consider this the t-skewing parameter with respect to the clock, we say that at this particular clock the black lines not the dotted ones, the black lines is the clock which is arriving early.

The dotted lines are the one which I am saying that the clock is arriving late. As per our condition that the worst case condition the first pulse latch is going to receive the arriving late clock and the second pulse latch is going to get the early clock. With that in mind, let us then try to understand the data flow of this particular data that the subsystem design. If this D1 is the input to this latch 1, this is the latch 1, the D1 is the input. If it is made available before this skewed clock then I will get the Q1 signal after the clock to Q propagation delay and that goes to the combinatorial circuit number 1 which will give the output after the propagation delay of the combinatorial circuits.

Then this particular delayed or this particular output of the combinatorial circuit should be made available at least before the t_{setup} of the clock that is going to the latch number, the pulse latch number 2 and that the clock for the pulse latch number 2 is nothing but the clock arriving early.

I have drawn the t setup time with respect to this the black line clock signal and not with respect to the dotted lines because this is the clock that has been arriving early. Here the t_{pcq} I have drawn with respect to the dotted lines because the pulse latch is actually having receiving the clock that is arriving late.

If this is the particular timing diagram and its parameters associated with it, what should be the clock time period or what should be its propagation delay of the combinatorial circuit that we need to design? if I consider this particular clock time period from black line to the black line or dotted lines to the dotted lines that will be Tc.

If I notice this Tc - t_{skew} will give me this particular dotted lines to this particular point. The Tc - t_{skew} will give me starting from here a point A, I will write it and then for two here point B and if I have A and B, I can do A B plus the t_{pw} will give me this Tc point.

Now I have this particular whole duration where I can actually use the t_{pcq}, t_{pd1} and then the t_{setup}, on right hand side I have t_{pcq}, t_{pd1} and t_{setup} and on the left hand side I can say that the points A to C, the duration from the A to C which is nothing but,

$$T_c - t_{skew} + t_{pw} \geq t_{pcq} + t_{pd} + t_{setup}$$

This particular A to C point should be greater than or equal to the other 3 parameters. In that sense what we have is the t_{pd} value is now should be the maximum t_{pd} value turns out to be Tc - $t_{skew} + t_{pw} - t_{pcq} - t_{setup}$. notice that if the t_{skew} was not there, the t_{pd} value would turn to be higher, if it is there the t_{pd} value turns out to be lesser. the maximum delay constraints has been reduced further. This is the overall expression for the clock time period, for the pulse latch with the pulse which has been generated by the clock and then having the clock is having the skewing characteristics.

The maximum delay constraints for the t_{pw}, the t_{pd} the pulse width that has been given to the pulse latch is actually very very small then we will have this particular expression. But if the maximum delay constraints if you are trying to see for the pulse width to be very very large compared to the t_{setup}, then it behaves like a latch and we know that the latches it is actually skew tolerant.

In fact, the propagation delay that is for the combinatorial circuits if we design for the latch it is kind of skew tolerance. The t_{pd} value does not have an expression where the t skew is involved and that is what is likely to happen even if we have the t_{pulse} width to be very very higher. If the pulse width is lower that is when we will have this particular expression.

In this particular case, in this particular diagram, I have drawn the pulse width to be low compared to that of the t_{setup} and that is kind of seen here and the t_{pulse} width is very very small compared to the t_{setup}.

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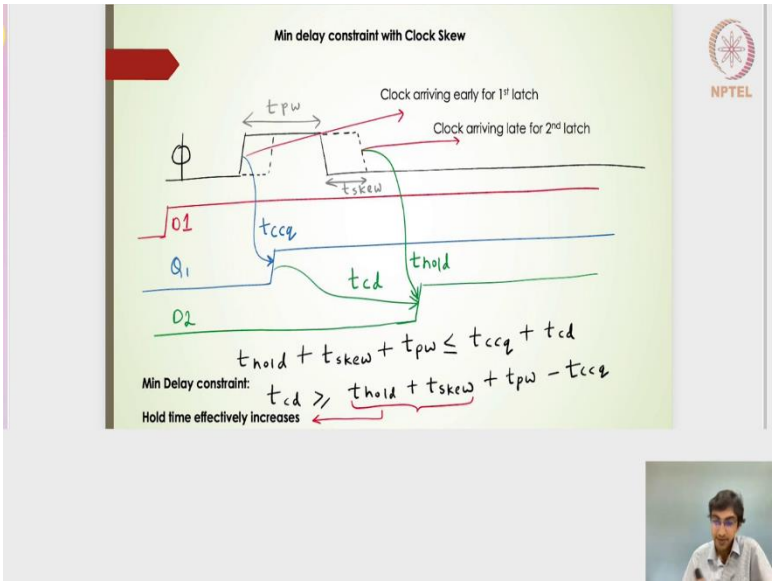

Moving ahead. What should be the minimum delay constraints with the clock skewing? For understanding the minimum delay constraints we will say that the pulse latch 1 will get the clock that is arriving early and then the pulse latch 2 will get the clock which is the dotted lines which is arriving late.

The clock arriving early for the first latch and the clock arriving late for the second latch and with this t_{pw} also there the t_{hold} will be with respect to this dotted line after the t_{pw}.

If the 1st latch is receiving the signal D1 and its output which will be the contaminated output t_{ccq} will start with respect to the first rising transition with respect to the pulse signal. I will get the t_{ccq} followed by the Q1 will go to the combinatorial circuit number 1 and then the combinatorial circuit number 1 will throw the contaminated output after the t_{cd} time duration.

I will have a t_{cd} time duration. But we need to ensure that the t_{ccq} and t_{cd} should surpass this t_{hold}, that it will be getting captured in the second clock and not in the first pulse. For the second the pulse latch what we need to do is it should get the output captured not in the first pulse, but rather it should be captured in the second pulse. For doing that we know we need to make sure that the t_{cd} value and then the t_{ccq} should be able to surpass this t_{hold}.

If I look into the expressions here

$$t_{hold} + t_{skew} + t_{pw} \leq t_{ccq} + t_{cd}$$

What it means is the,

$$t_{cd} \geq t_{hold} + t_{skew} + t_{pw} - t_{ccq}$$

Effectively what we are seeing is the t_{hold} if the t_{skew} is added, if the t skew is characterized in the minimum delay constraints the t_{cd} value increases, needs to be increased when the t_{skew} was not there.

Effectively the t_{hold} is going to be increased, the t_{hold} time effectively increases, if I consider t_{skew} as one of the t_{hold} parameters. With the t_{pd} t_{pw} also the t_{cd} value will be increased. If I consider the pulse latch with respect to the flop designs, the flop design does not have this t_{pw} parameter and my t_{cd} that we will design for the flop designs.

When I compare with the t_{cd} when we use it for the pulse latch designs, we will not have this t_{pw} parameter. Thereby for the flop designs the t_{cd} is much more relaxed whereas, for the pulse latch in the t_{cd} parameters is much more constrained because my t_{cd} value has to be necessarily,

$$t_{cd} \geq t_{hold} + t_{skew} + t_{pw} - t_{ccq}$$

Then it goes closer to that of the t_{pd} of the combinatorial circuits. In that sense we will have much more constraints in the pulse latch designs, hope this is clear. Moving ahead.

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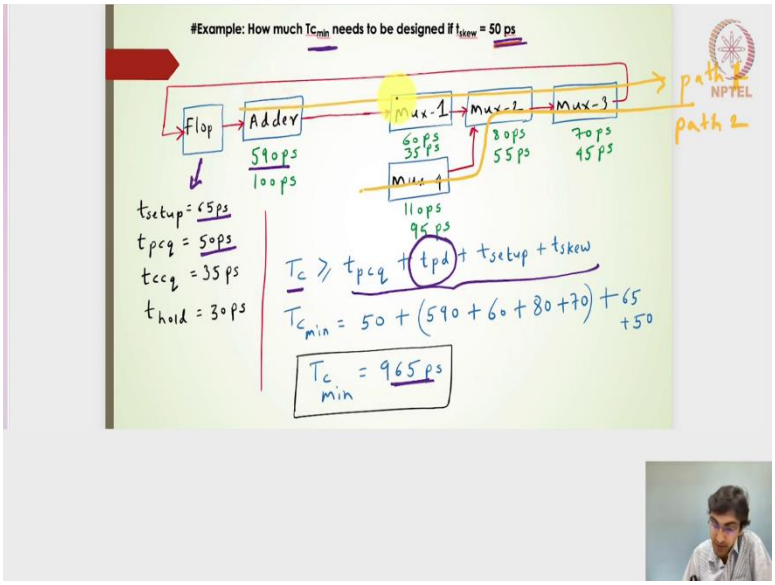

Let us see an example here of the t_{skew} of 50ps, and we have the flop designs and then the adder mux 1, mux 2, and mux 3 and then we also have another data path here. There is one data path coming from adder, muxs, 3 muxs, this is path 1 and then there is another path here the mux 4, mux 2, mux 3, this is the path 2. The propagation delay and then the contamination delays of this particular blocks combinatorial circuits blocks are given here 590, 60, 80, 70.

Contamination delays are also given here 100ps, 35, 45 and 45ps. For the mux 4 the propagation delay is 110 and then the contamination delay of 95ps is given. The flop is only one flop, but at the output of these combinatorial circuits will pass into the flop designs and then keep doing that for every clock cycles. The question here is what should be the Tc minimum that needs to be designed, so that to accommodate that t skewing factor of 50ps.

The flops characteristics is also given here t_{setup}, t_{pcq}, t_{ccq}, and t_{hold}. The minimum clock time period that needs to be addressed or that needs to be designed is Tc should be greater than or equal to and this is a flop design, I will use the flop design timing diagram parameters which will be nothing but the $t_{pcq} + t_{pd} + t_{setup} + t_{skew}$.

Remember that in the timing diagrams we had seen on one side Tc minus of t skew, on the other side we had $t_{pcq} + t_{pd} + t_{setup}$ and then Tc - t_{skew} should be greater than or equal

to these 3 parameters. I have taken the t skew on this particular side. We will get the clock time period is it should be greater than or equal to this particular 4 parameters.

The Tc minimum is nothing but,

$$T_{c_{min}} = 50 + (590 + 60 + 80 + 70) + 65 + 50$$

$$T_c = 965ps$$

The minimum clock time period that has to consider the clock skewing is also 965ps and I have not introduced the path 2 here. The path 2 anyways the propagation delay will be less because considering the adder which is 590ps and comparing with this particular path of 110, 80 and 70 this particular path of adder mux 1, mux 2 and mx 3 will be much more higher.

My t_{pd} value here, if I consider the path 1 will be more higher than that of the t_{pd} for the path 2, this becomes my critical path or this becomes the path where the delay was delay is higher.

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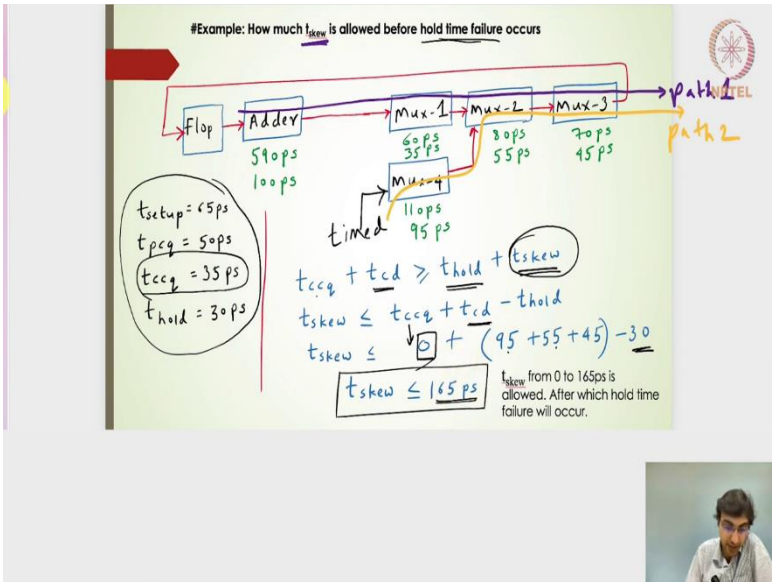

In the same example the same designs where we have the path 1 and part 2, how much is the t skew that has been allowed before the whole time failure occurs? let us say that the clock characteristics are not given to us and then we are supposed to design it and then say that what should be that clock skewing and then let us say that the clocks are available in

the standard cell libraries. Based on the skewing parameters I can actually choose the clock standard cell library, in that sense what should be the t-skewing characteristics.

If I have this particular subsystem design of the data path system design, we still have the two paths one is the adder path, path number 1 and another path is this one, the muxs are going to mux 2, max 3, this is path number 2, alright, and then we need to find out how much t skew is allowed before the whole time failure occurs.

It is a whole time, it is basically the minimum of the contamination delays, the minimum of the contamination delay for the path 1, the contamination delay of the path 2 and whichever is one is minimum we should consider that.

If I consider the contamination delays, we definitely know that the adder of 100ps and 135ps is actually more than that of 95ps. I will have to consider this path 2 designs for considering the whole time failure. The $t_{cd} = 95 + 55 + 45$.

If I am trying to find out the timing diagram and then express my t_{hold} time, we know that for a flop designs the t_{skew}, the skewed clock is there for the next flop.

$$t_{ccq} + t_{cd} \geq t_{hold} + t_{skew}$$

$$t_{skew} \leq t_{ccq} + t_{cd} - t_{hold}$$

$$t_{skew} \leq 0 + (95 + 55 + 45) - 30$$

$$t_{skew} \leq 165\text{ps}$$

Here the t_{ccq} I am considering it to be 0 which is not appropriate which is not correct. In the sense, what we are assuming is in this particular data path system this mux 4 input to the mux 4 should also be timed. We are considering it is not to be timed at all and it is appearing from the first clock.

The t_{skew} from 0 to 165 is kind of allowed which is kind of inappropriate if we consider this to be 0, what do we do?

Let us say that this mux 4 is also timed that means, that we will also use some kind of a flop here which will have the same characteristics as that of this. If I use this t_{ccq} I will get this 35ps, this 35ps has to be added here. It will go to 165 + 35ps.

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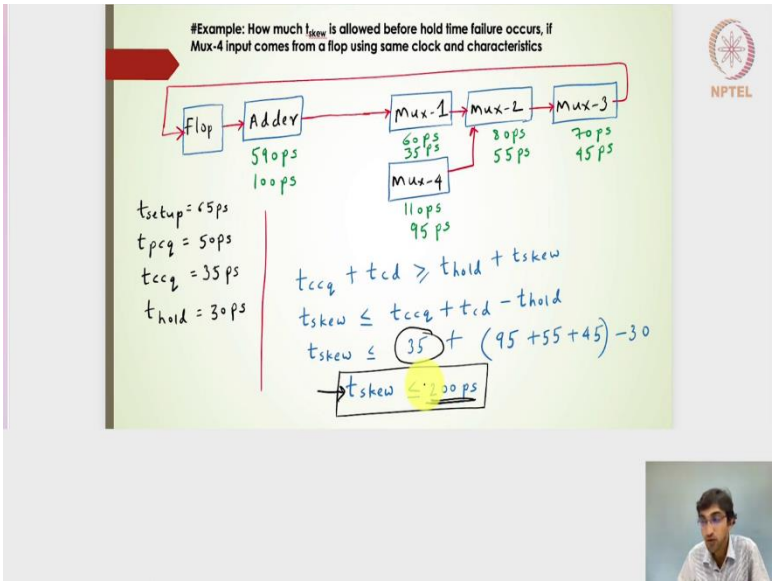

In fact, the t skew that can be allowed is 200ps because I have considered this mux 4 input to be a timed one, which has 35ps. My t_{skew} that is allowable is around 200ps and what we are assuming here is the mux 4 whatever is a timed one, so that particular flop and then this particular flop are actually having the same characteristics.

Now if I know that this is the t_{skew} that could be allowed in this particular circuit design, I can easily choose a clock which is having thus then the skewing from 0 to 200ps, not more than 200ps. If it is more than we will have a hold time failure. Hope this is clear. This completes the static timing analysis part and then where we had seen this clock skewing effect for the pulse latch and also we considered some of the examples for the flop designs and then what should be the skewing factor or what is the allowable screwing factor that we can choose for a clock for in this particular data path subsystem example.

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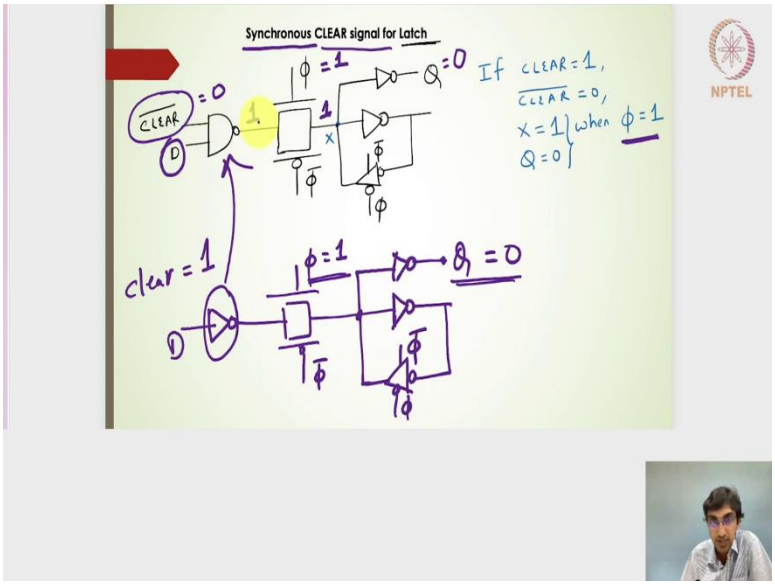

In this particular the short lecture, I am just going to introduce the latch designs generally in a latch or a sequential designs, we will see the clear signals and then the set signals or the preset signals. Now, how do we accommodate that clear signals as well as the preset or the set signals in the CMOS latch designs?.

Notice that this particular latch designs if I consider a CMOS latch this is nothing, but the transmission gate, this is what we have. The ϕ goes here assuming that this is a positive level latch and then we have an inverter at the output side to make it insensitive to the noise and then we have a tri-state inverter to ensure that this particular node is statisticized.

The statisticizing is we keep the strategizing only during the opaque state that is when during the ϕ going low that is why we are giving a tri-state inverter here with a clock of $\overline{\phi}$, and ϕ here. Another inverter is added here in the Q signal because if I have this inverter and then this inverter, it can bring back the output noise signal and that is why we have this particular inverter here to ensure that the output noise is not coupled inside the latch.

We used to have this inverter to ensure that the input noise is not coupled into the it is not passed into the latch internals of the latch, this is our latch design. But now if I want to introduce a clear signal, what it means is if the clear is 1, the output should be 0. If it is a synchronous clear signal, what it really means is only when the clock is high if the clear is pressed, during any time in the clock level being high then we will get the clock to be 0, output to be 0.

When the clock is actually low even if I press the clear signal continuously, we will not get any output to be 0, we will the previous state output. That is what it means the synchronous clear signal for this latch. One easiest way to do is replace this inverter with that of the NAND gates.

An two input NAND gate, where the one input is the D input signal the other one is the clear signal or rather the $\overline{clear}$ signal. If the clear is 1 here when the $\phi = 1$, when the $\phi = 1$ that means, in the transparent mode or when the latch is kind of tend to be operating.

When the clock is 1 at a high level we can say that the clear is 1, the $\overline{clear} = 0$. This will become 0 and then the output of this NAND gate irrespective of the D input, irrespective of D whether it is 1 or 0 it will give me 1. This will throw a 1 here because the transmission gate is going to pass because the $\phi = 1$ here and then the $Q = 0$. That is why this particular circuit design we can say that it is synchronous clear signal for the latch for the CMOS latch.

When $\phi = 1$, $X = 1$ and then $Q = 0$ and if I have the $\phi = 0$ here and even if I press the clear = 1, the $\overline{clear} = 0$, even then irrespective of the input I will get a 1 here, but the $\phi = 0$. This 1 is not passed to the other side of the transmission gate and that is why we call this design as a synchronous clear signal for the latch.

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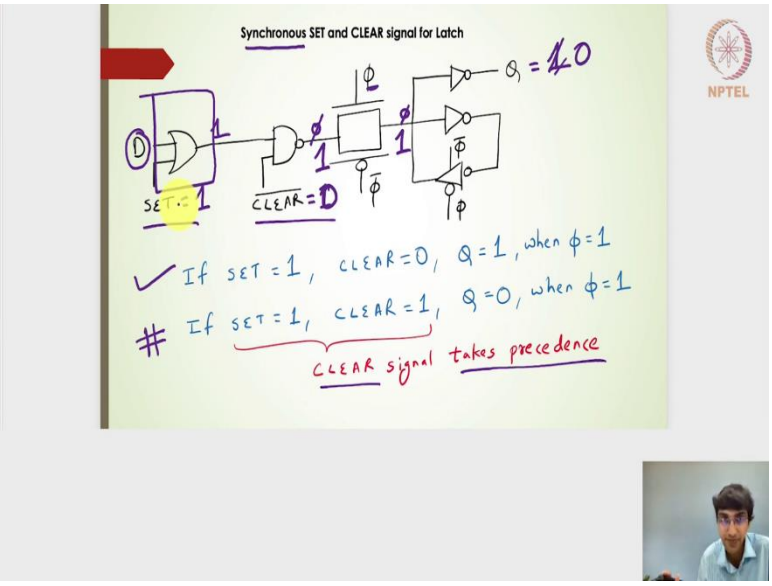

In the previous slide, we had seen how do we clear the output of the latch design. Here in this particular case, we are using a preset or a set signal. The preset or a set signal is likely to give an output of 1 here and in this particular circuit design it is not only the latch, but also the preset as well as the clear control signals both of them have been accommodated or incorporated. Both of them are applied for a synchronous set of the latch.

That means, whenever the $\phi = 1$ and if one of the control signals are operating that is when we will get the Q to be 1 or 0. If it is set then we will get the Q = 1, if it is clear is pressed then the output will be 0. In this particular case, let us say that the set is 1 here and let us say clear is not at all pressed, such clear will be 0.

The $\overline{clear} = 1$ and irrespective of the D input here because the set is pressed to 1, I will get an output of 1 here which will throw an output of 0 here, the 0 is passed during the clock level is high, and this is going to give an output of 1.

When the set is pressed when the clock is high that means, the synchronous set signal for the latch that is when I will get the output to be 1. When the clock is not 1 or the clock is not high that means, that the clock is low and if I keep on pressing the set signal, then even though I will get a 1 and a 0 here it will not be passed to the through the transmission gate. In that sense, I will not get the output of 1 when the clock is low.

Similarly, if I have both the control signals, if I want to press the clear I will depress the set signal I will not activate the set signal and then press the clear signal. This $\overline{clear} = 0$ and then that 0 is going to make the output of the two input NAND gate to be 1. This 1 is going to pass through the transmission gate and Q = 0 instead of 1. Based on the clear or the set signal that has been pressed we will get the output to be 0 or 1, that clears this particular part of the slide.

Now, here I have actually written one particular condition where there could be a contention. Although you will not realize that, but let us say that what happens if the set is 1 and the clear is also pressed. The $\overline{clear}$ instead of 1 it is actually 0.

You mean in that particular case if the set = 1 no matter whatever is the D value here, D input value it will be 1 here. But because the clear = 0 here, that means, clear is pressed here, that means, $\overline{clear} = 0$. The two input NAND gate is going to throw an output of 1

here, because the $\overline{clear}$ = 0 and if that is 1, then this will be 1, when I am assuming that the clock is high and then the output Q = 0.

When both of them are actually pressed, the clear actually takes the precedence. The clear signal takes the precedence here, if both of them are activated at the same time or of the both of them are pressed at the same time. The designer although this control signals are made available the designers when they are controlling the signals the set and the clear, one should be careful that both of them will not be pressed at the same time.

The other way is to give the set more precedence is they swap the positions of the set and then the clear. This particular NOR gate if I put it here and then the NAND gate if I put it here, the other input of the NAND gate is the D signal and then this particular input is the clear, then in that case the set will take the more precedence than that of the clear signal, hope this is clear.

In this particular slide what we have seen is the synchronous set and clear signal for the latch that has been accommodated into the latch design, because it is a synchronous signal that means, that whenever the latch is operating that is the latch is in the transparent mode that is when the clock is high, then only if I press the set and clear signal we will get the output to be high or low, based on what the control signal is being pressed. Hope this is clear. Moving ahead.

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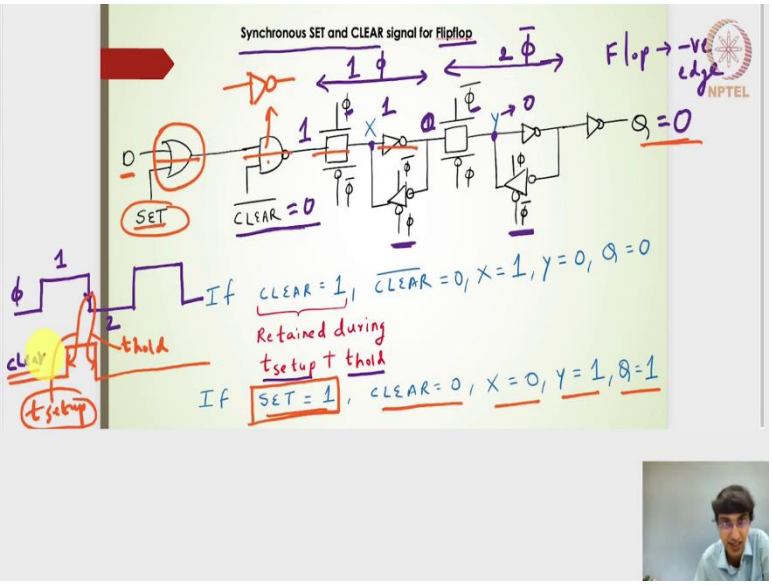

Let us take a look at the synchronous set and clear signal for a flip flop. In the last slide we had seen for the latch design. In this particular case, if I use the same thing the set and the clear and then this particular portion is going to give me one particular latch. This is the first latch, and then another transmission gate is going to give me the second latch.

The first latch is operating in the high level of the clock, the second latch is operating in the low level of the clock. This particular flip flop is a negative edge flip flop, that is what negative edge flip flop, triggered flip flop.

The reason is nothing but if the input is passed through the high level of the clock and then it has to wait till the negative clock does the transition of the clock does the negative edge transition and then goes into the negative level of the clock or the low level of the clock, that is when the input is passed through the next transmission gate and then it appears at the output.

During the negative edge of the clock that is when the input from this particular flip flop will be passed to the output. These two particular the tri-state inverters are placed here. This particular tri-state inverter, and this particular tri-state inverter will ensure that the node X and Y are subsequently statisticized. It does not you know it makes sure that those nodes are statisticized and not dynamic anymore.

This tri-state inverters are there they are operating in the opaque mode of this particular latch 1 and opaque mode of this particular latch 2. Notice that this particular tri-state inverter is actually operating in the complement of this clock for the latch 1 and then this particular tri-state inverter is operating in the complement of this clock for the latch 2.

If the latch 2 is operating at the $\overline{\phi}$ that is the low level, this tri-state inverter will operate in the high level of the clock. If this particular latch is operating in the high level of the clock, this tri-state inverter will operate only in the opaque mode that is the low level of the clock.

With this particular understanding we have the set and clear signal here and we want the synchronous set and clear signal for the flip flop. If the clear is 1 here and let us say the set is disabled, if a set is disabled means set = 0 and if the clear is made pressed, I will get a $\overline{\text{clear}} = 0$.

Irrespective of the D signal here I will get a 1 here and then this 1 if it is a positive level that has been running around, I will get a 1 here. Then I will get X = 1 and then Y = 1 at this particular or rather this will be 0 and then Y = 0 in the $\overline{\Phi}$ and then this 0 will be passed into the output 0.

But notice here that I need to press this clear signal and it has to be pressed for the entire duration of the t_{setup} time and then the hold time. If I press the clear signal and then release it then the D will take the precedence. What I mean is if I have a clock here, I am drawing the clock signal here, we know that the latch number 1 operates here and then the latch number 2 operates here and then so on. This is the negative edge trigger flop that is, I am drawing the negative edge of the clock.

The clear signal, this is the clock signal and then let me draw the clear signal also. The clear signal should be pressed, before the t setup time and it should be retained till the t_{hold} time at least, this is the t_{hold} time. I am going to write it as the t_{hold} and this is as the t_{setup} time.

It has to be pressed for this particular duration of the t_{setup} and t_{hold}, so that the output of here the output of 1 is passed to the X node as 1 and then after the inverter it is to be 0. This 0 should be made available as soon as this particular negative edge transition appears, so that 0 will pass across this particular transmission gate and make the Q to be 0.

Now, the question is if I actually do not retain it during this setup and hold time, if I actually make this clear signal come down. If I do not maintain it for this t_{setup} time and if it comes down, then there is a possibility that the clear when it comes down. The D signal whatever the D input was there it might take the precedence and then pass at the output we will actually get a D output, whatever is the D signal that has been provided to the flop that might appear, it might actually get sneaked in.

Even if you wanted to have a clear signal we will not get the clear or we will not get the output to be 0, that is a possibility. To avoid that we ensure that the clear signal should be pressed at least before the t_{setup} time and should be held high till the t_{hold} time.

Similarly, if I want the set signal or the preset signal then the Q = 1, in that sense the clear is disabled or the clear signal is depressed or made it 0. If set = 1, I will get a 1 here and then that will be followed and then the Q = 1.

That is what I have given. If the clear is made 0 and then set is made 1, I will get an X = 0 and then Y = 1 because X = 0 and then Y = 1 and then from 1 the Q = 1. Again notice that the set signal should be ensured that it is retained for the t setup and t hold time.

One more information here is if you notice the latches or the flip flop designs, we used to have an inverter here instead of the two input the NAND gate, alright and then our t_{setup} time if I really want to characterize the t_{setup} time for a particular latch or a flip flop here, it used to be this particular inverter delay followed by the transmission gate delay followed by this particular inverter delay.

Now, what we have done is this particular NAND gate is been accommodated instead of the inverter to accommodate or incorporate this clear control signal. My t_{setup} time or rather the characterizing the t_{setup} time for this particular flip flop designs or the latch designs will be instead of the inverter delay it will be now be the two input NAND delay followed by the transmission gate and followed by the inverter.

That my t_{setup} time will be re-characterized for this particular circuit. If I want to have the clear, this will be the updated t setup time because my circuit is now slightly updated, the updated setup time. The clear should be pressed for an updated t setup time plus the t hold time, that I will get the Q to be 0.

Similarly, if this is my circuit design, the set signal should be ensure that it is stays high for this part of the delay plus this part of the delay plus this part of the delay and then plus this part of the delay. That determines the t or whatever the set signal should be made high till this all these 4 components before the negative edge of the clock and then plus the t hold time.

While we are pressing or while we expect or while we are trying to do the clear, the output to be clear, the clear should be there before the updated t_{setup} time. Whereas, for the set signal whereas, for pressing the set signal, we have to ensure that we have to also accommodate this particular delay as well apart from the t_{setup} time that has been characterized by this NAND gate delay, transmission gate delay and inverter delay.

I need to whenever I am pressing or whenever I am expecting the set Q = 1 or presetting the flip flop designs, ensure that it is slightly early. The set signal of the preset signal

should be slightly earlier than the t_{setup} time which I use it for the clearing the signal or providing the D input.