Design and Analysis of VLSI Subsystems
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Lecture - 82
Static Timing Analysis - Part 5

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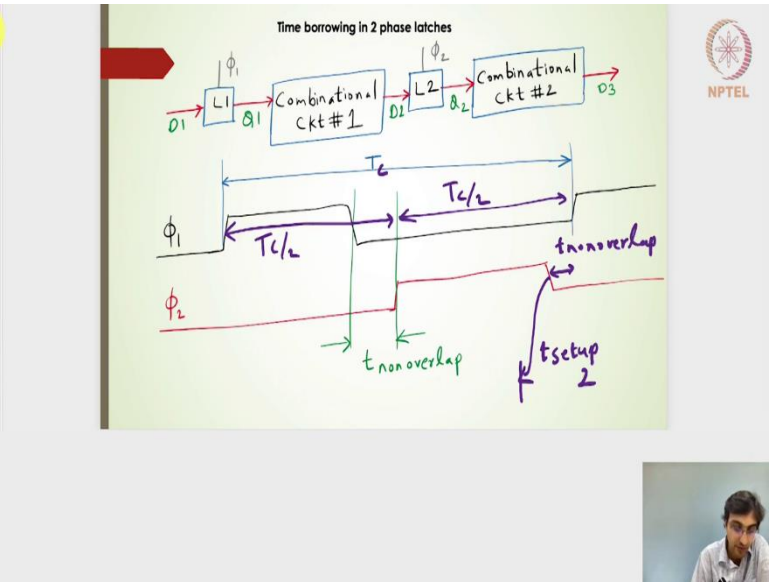

This is a particular circuit diagram, let me also pick my pointer. This is the overall subsystem diagram here at a block level. I have the latch 1 here, latch 2 here and in between the combinatorial circuit number 1 followed by the combinatorial circuit number 2 which is there in between the latch 2 and latch 3.

In this case what we are saying is the combinatorial circuit 1 can actually borrow the time from the second clock high level and the maximum borrowing time is nothing but Tc/2. If this is Tc/2 and this is Tc/2 making one particular clock cycle. I am going to write it as Tc and it can borrow or it can extend the combinatorial circuit output can extend till we have the set up time associated with the latch 2.

It can extend up till this particular portion of the time and the maximum $t_{borrow} \leq \frac{T_c}{2} - t_{nonoverlao} - t_{setup}$.

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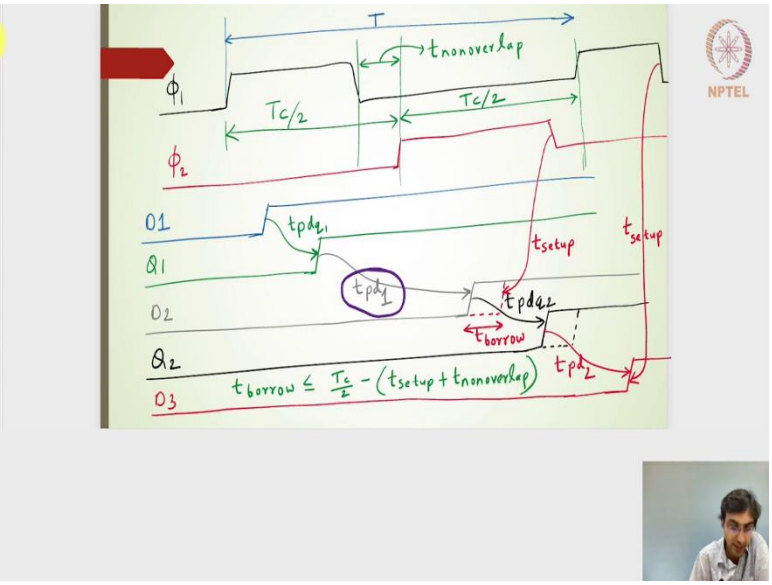

This is what in the timing diagram I have drawn here the D1 is the signal at the input of the latch 1. The output of the latch 1 will be coming out after the t_{pdq} and then D2 signal which is the output of the combinatorial circuit number 1 will come at after the t_{pd1}. The t_{pd} the propagation delay of the combinatorial circuit number 1 and the second latch output will come after the t_{pdq2} and then the combinatorial circuit number 2 is going to come out after the propagation delay of the combinatorial circuit number 2.

In this whole sequence of the output that is been generated after the every blocks, this one the combinatorial circuit number 1 which is supposed to operate and then make the signal available in this particular region of the time or in this particular region of the time, because it is supplying the combinatorial circuit number 2 is supplying the output as an input to the latch number 2. The latch number 2 can actually capture till it reaches the t_{setup} with respect to the clock going low. It can extend the combinatorial circuit can actually extend or borrow the maximum $t_{borrow} \leq \frac{T_c}{2} - t_{nonoverlao} - t_{setup}$. I hope this is clear.

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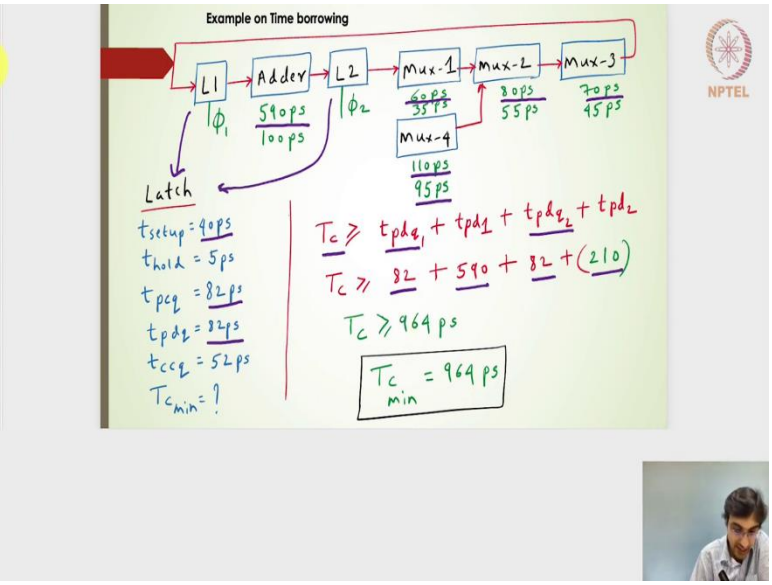

Now, just to take an example of the time borrowing, let us see this particular subsystem level diagram. We have the latch 1 here and then latch 2 here and in between there is an adder block which is taking around 590ps, the propagation delay. It is kind of very very heavy considering the 3 blocks here mux 1, mux 2, mux 3, which is taking around 60pss of propagation delay, 80ps and then 70ps the propagation delay.

The other delays that is been mentioned here is 100pss, 35ps 55 and 45ps are nothing, but the contamination delays. There is another path here coming from mux 4 mux 2 and mux 3 and which the mux 4 has is characterized with a propagation delay of 110ps and 95ps.

With this particular parameter and then with the latch parameters which is characterized to t_{setup} of 40ps t_{hold} of 5pss t_{pcq} of 82 t_{pdq} of a 82ps and then the contamination clock to q is also given. One is to find out what is the minimum clock time period and that is something we can easily find. Looking at the timing diagram we can say that the minimum.

$$T_c \geq t_{pdq1} + t_{pd1} + t_{pdq2} + t_{pd2}$$

In that sense t_{pd}, I am assuming that the L2 L3 and the L1 and L2 latches have the same characteristics. I will use the t_{pdq1} and t_{pdq2} parameters to be the same, both the latches has the same parameters which is given here.

$$T_c \geq 82 + 590 + 82 + 210$$

$$T_c \geq 964\text{ps}$$

$$T_{c_{min}} = 964\text{ps}$$

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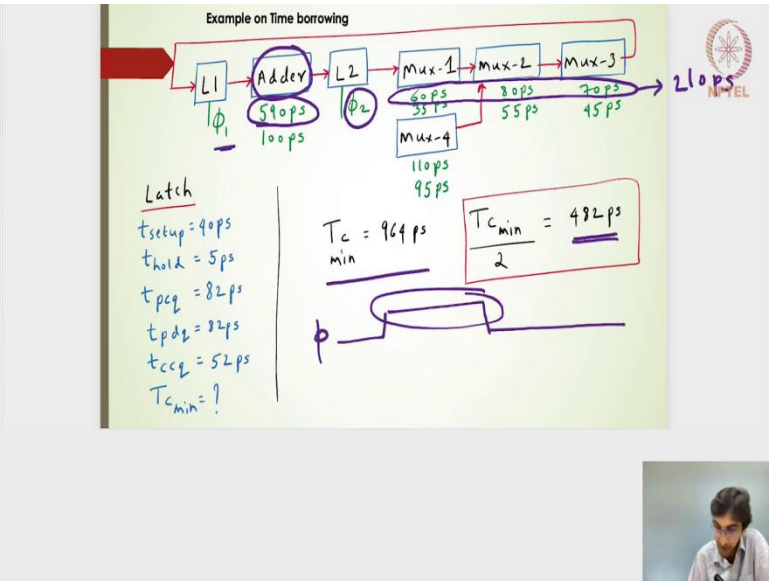

That is our clock time period that will be designed for this particular subsystem block. If the clock time period if I choose to be 964ps then the,

$$\frac{T_{c_{min}}}{2} = 482\text{ps}$$

It is kind of very important to use this Tc/2 to understand how much of the maximum borrowing time is available for the adder circuit, because that is the combinatorial circuit number 1 and if I actually see this the adder circuit has 590ps.

Whereas the mux 1 mux 2 and mux 3 put together if I actually round it off and then make a cumulative assessment it will be 60 + 80 + 70 = 210pss. The 590 is much much higher than the 210ps. In fact what is likely to happen is the adder circuit is occupying more time or rather it is entering into the to the $\phi 2$ clock being high it is utilizing some part of that and then I think the L2 is kind of getting captured and then it is the input is supplied to the mux 1 mux 2 and mux 3.

The adder block is actually extending beyond the first level of the ϕ1 clock and then how much it is extending. For among this 590 we know that 482ps is only the level high which is there 482ps is the clock level high here, but the adder is going to take more than 482ps and then we need to understand how much of time it is kind of borrowing.

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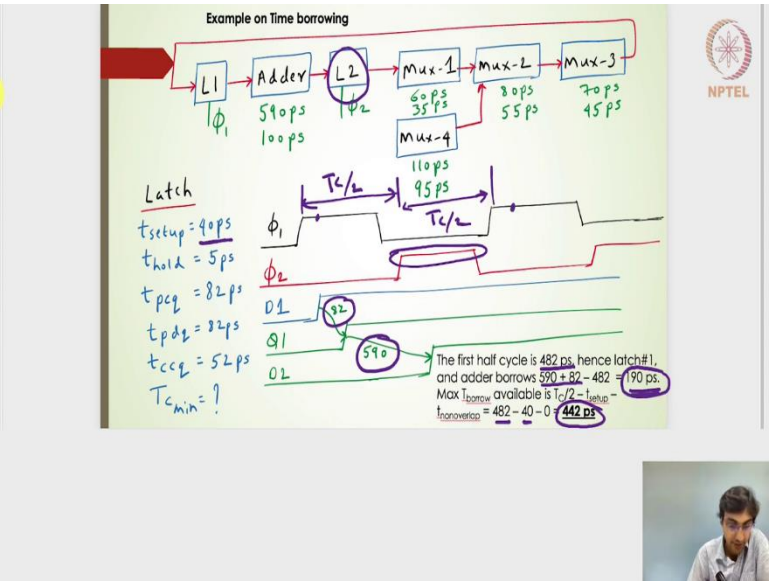

If I draw the timing diagram here of ϕ1 signal and then the ϕ2 signal and then we know that from here to here it is Tc/2 and then from here to here it is Tc/2. This will be Tc/2 and Tc/2. The Tc/2 is nothing but 480 whatever we have calculated 482ps, that is what the value is.

Now, if I draw the timing diagram of D1 signal Q1 signal and D2 signal here this is very interesting it takes 590ps and then it is made available in this ϕ2 being high.

After 590ps the D2 signal is now available and this clock level being high. The first half cycle is what is written as 482ps hence the latch 1 and the adder latch 1 which is taking it generates the output after 82ps and the adder generates the output after 590ps.

What it is saying is the latch 1 and the adder borrows $590 + 82 - 482 = 190$ps. It extends 82 + 590 it is more than 482ps, it extends beyond 482ps and how much time it is borrowing it is borrowing around 190ps.

Whereas the maximum borrow time that is been available is nothing, but 482ps - $t_{nonoverlap}$ - t_{setup}, that will be 482 - t_{setup} = 40ps -$t_{nonoverlap}$. Here the non overlap is

not at all characterized. We will assume it to be 0. The maximum borrowing time it has is 442ps, out of which it is actually borrowing 190pss.

$$t_{nonoverlap} = 482 + 40 - 0 = 442ps$$

It is very well placed and then once it reaches after the 590ps here and then we will have one more 82ps because of the latch 2 design. The latch 2 output the d propagation delay of d to q will take some time that will be 82ps and after that we will have 60 + 80 + 70 = 210ps. Overall, it will get captured again somewhere at this particular portion where it had started. That is how we are actually designing the clock time period, hope this is clear. The borrowing here it is actually borrowing 190ps.

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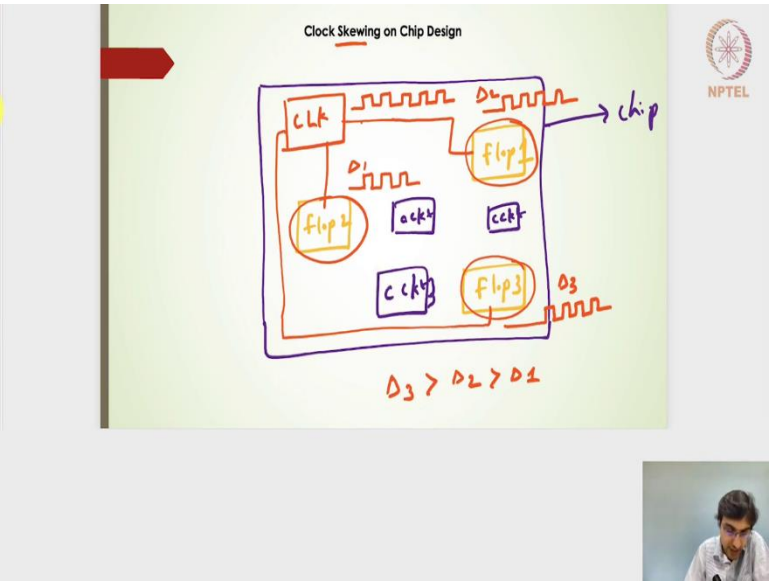

Let us continue with a new module called as clock skewing. Again a very important topic in the subsystem design and of course, the analysis of the subsystem design. Let me draw the chip level 2D diagram. Let us say that we have a chip here and I am going to put my clock circuit. I am going to say that the clock circuit is somewhere here. What it means is this is going to generate the clocks. This is going to generate the clock signal here and generally we will have minimum number of clocks we either have 2 or 3 clock generating circuits in the whole chip.

Let us say that we have our sequential elements and then followed by the combinatorial circuits and let us say that we have this flop designs here I will say that this is a flop 1 and then we will say that the flop 2 is here and we will say that the flop 3 is here.

We actually do not know where are the flops going to be placed in the whole footprint of the chip and the reason is very simple, we actually design the blocks the subsystem blocks and then it is being submitted to the placement and routing designers. They actually tend to place this flops as well as the combinatorial circuit in between them.

We will also have a combinatorial circuits in between combinatorial circuit here number 1 combinatorial circuit number 2 or wherever and that the placement and routing designers will then place this flops and then the combinatorial circuits such that it will optimize the area it will optimize the power and other things.

In that sense what we do not have is the placement of the flops designs and then the placement of these combinatorial circuit blocks, but what we know the flow of flop 1 goes to the flop 2 via the combinatorial circuit some particular combinatorial circuit number 1 or 2 and then flop 2 we will go to the flop 3 and via the another combinatorial circuits. In that sense we know how the flow is, but we do not know the placement of these flops and remember that the clock signal we generally have minimum number of clocks what it means is a clock circuit or a generating circuit is then distributed to the different sequential elements.

We have this particular clock segments which is going and connecting to the flop 1 it is also connecting to the flop number 2 and it is also connecting to the flop number 3 notice here that flop 3 has the maximum interconnects here flop 1 or rather flop 2 has the minimum interconnect length here and flop 1 has in between the interconnect length here. What it means is even though the clock is generated here by the time it reaches the flop 1 it will be delayed.

By the time it reaches flop 2 it will be delayed and by the time it reaches flop 3 it will be maximumly delayed. If the clock is generating this signal and by the time it reaches flop 2 there may be slight delay, I will write that the delay will be Δ 1 for the flop 2 here flop 1 it there will be a slight delay again.

Then I am going to write it as Δ 2 and in the flop 3 it will be the maximum delay. I will write it as Δ 3 and notice that the Δ 3 is actually very very large compare to Δ 2 compared to Δ 1 and if actually I do not know the placements of flop 1 2 and 3. In fact, it could be completely the other way also flop 3 can be very very close to the clock flop 1 kind can be very very far away from the clock. While I am actually designing at a stage before the routing and the placement what we really want to do is irrespective of the flops placement we have to ensure that even if I have a delayed clock even if I have a skewed clock.

Even if I have a skewed clock then also the circuit should be able to capture the output then also the flop designs or whatever the sequential element designs it could be a flop it could be a latch it could be a pulse latch it should be able to capture the input at that particular skewed clock. If we are expecting that it should be captured in the second clock it should be able to capture that, in that sense what we are saying is this delayed clock signal also called as skewed clock or a clock skewing and we should design the circuit in a way that it should be resilient to this particular skewed clock.

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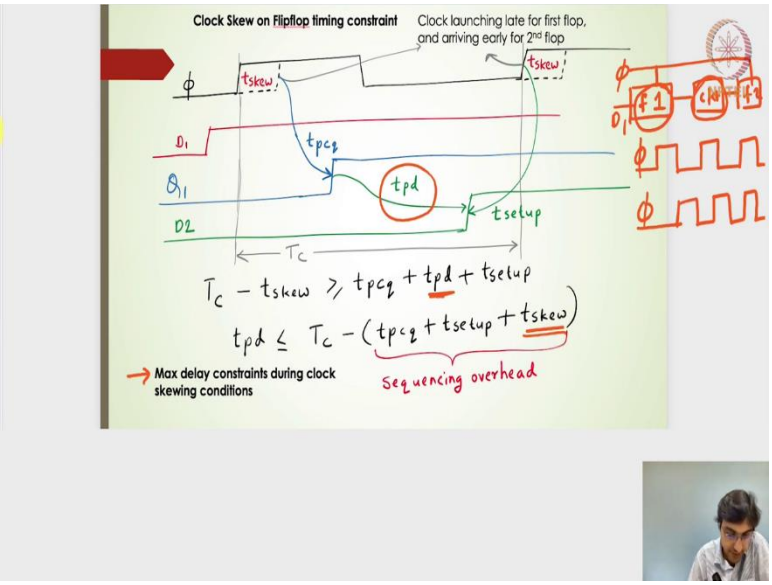

Moving ahead let us take a simple example of what you used to do. Let us say we have flop number 1 connected to the combinatorial circuit and then that goes to the flop number 2 and then we have the clock which is kind of generated.

Remember that flop number 1 has a delayed clock. Flop number 2 also has a delayed clock it could be very very near to the clock. What do we do? if we have the clock characteristics

of the clock over the chip design and that is something we can actually get it characterized by the clock designers. If I know the chip design area and then where the clock is going to be placed and then as a designers I need to know I already have the characteristics of the clock. I will have the clock with no delay and we can easily get the clock with the maximum delay.

Basically I am saying that the clock characteristics or the clock skewness the maximum skewness for a particular chip. We will be able to know from the clock designers and if that is provided then I can ensure consider the worst case and then try to design the combinatorial circuits t_{pd} or t_{cd} parameters.

What we are saying is in we have to consider the worst case of the clocks skewness and then design our combinatorial circuit. In this particular sequence of f1 and then the flop 1 going to the combinatorial circuit number 1 and then going to the flop number 2. This is the clock signal and we have the input to the flop number 1. The output of the flop number 1 goes to the combinatorial circuits and then the output of the combinatorial circuit is fed to the flop number 2. In this sequence of the data path alright. In this particular subsystem design what we need to take care is the worst case condition and in this particular sequence if I have let us say only 2 flops and then the clocks skewing is given to us.

Then, we can easily say that we can have a worst case where f1 is placed at a very far end of the clock and 2 is placed at the very near end of this flop. The f2 is placed at the very near to the clock generate source generating circuit and f1 is placed farthest to the clock source generating circuit.

In that sense what we are saying is the although the clock signal is shown in this particular black lines we can say that the f1 is actually getting the worst case the this skewed clock here annotated with the dotted lines and the flop number 2 it because it is placed very very close to the clock source generating circuit it is getting the clock which is arriving very very early.

The dotted lines because it is skewed or because it is delayed we can say that this particular clock is launching late for the first flip flop and then this particular black line is the clock which is arriving early for the second clock second flop, we are considering the worst case.

If it is the other case if it was the best case we can say that f1 to be placed very very near to the clock generating circuit and f2 to be the farthest from the clock generating circuit, but then that will give the best case and then there is nothing to be worried about this combinatorial circuit design.

But, if it is the opposite case that is where the worst case design comes in and then we have to ensure that the combinatorial circuit design is designed in such a way that it still becomes resilient to the skewing. If that is the worst case, we have this kind of a skewing effect. Even if the D signal is made available just before the skewed the t_{setup} with respect to the skewed. If it is made available we will have the q1 generated with respect to this skewed, the transition and then we will have the t_{pcq} propagation clock to q of course, this clock is nothing, but the skewed 1.

I will have the t_{pcq} which is the characteristics of the flop design. Which is output of the flop 1 goes to the combinatorial circuits and then we will have the output of the combinatorial circuit after the propagation delay of the combinatorial circuits and we have to ensure that is made available just before the clock which is arriving early for the second flop.

It has to be made available t set up time before the clock that is being provided to the second flop and in this case the clock is arriving early. For the first flop worst case condition we are saying that the clock is delayed its arriving late and in the second in the second flop it is arriving early for the worst case condition.

In this particular case the difference here is because of this skewness. In an ideal clock where I am saying that all the clocks to the flipflops are arriving at the same time we will not have this skewness at all.

Whereas, in this particular case where the clocks could be arriving at different particular time intervals for the flops although it is coming from the same clock source generating circuit, because of the interconnect delay there will be in the skewness and if it is a skewness what should be my t_{pd} or what should be the maximum t_{pd}. That I do not have it still does not violate the set of time failures.

Looking at this particular timing diagram we can easily say that if I consider this t time period from this black line to this particular black edge transition we know that this is,

$$T_c - t_{skew} \geq t_{pcq} + t_{pd} + t_{setup}$$

The maximum t_{pd} is,

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew})$$

This will be the sequencing overhead alright. The maximum delay constraints during the clocks skewing condition is this one. Remember that in an ideal clock where the clock arrival time is same for all the flops, this giving effect will not be there.

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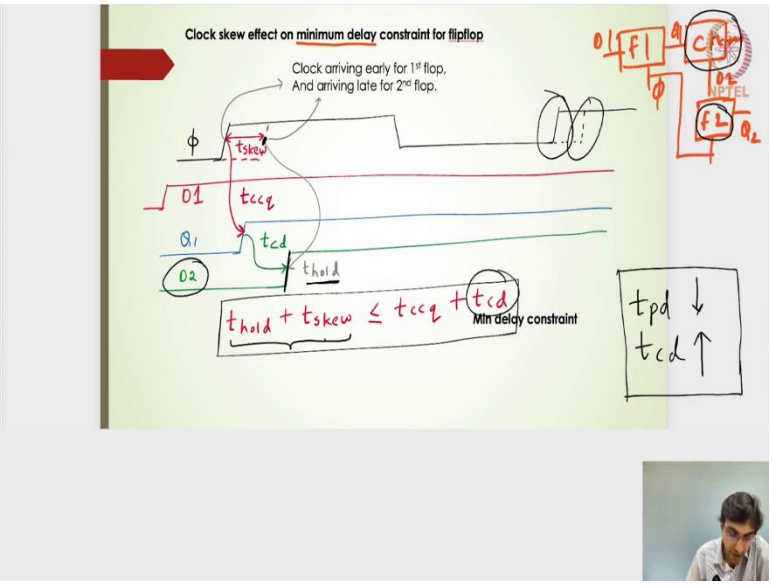

Now, let us see how the clock skewing effect will have it impact the minimum delay constraints. For a minimum delay constraints because, we do not know the placement of the flops. Let us say I am going to draw the flops flop 1 and then we have the combinatorial circuit and then we have the flop number 2. This is the sequence in our subsystem design and then we say that it has a clock here and then it has a clock here this is the output D1 Q1 combinatorial circuit output is D2 and then it gives the output of Q2.

This is the flow. In our previous data path system example what we have taken was the clock is arriving late here and early here for the minimum delay constraint it could be exactly the opposite way. It is the clock is arriving early for the flop 1 and it is arriving late for the flop 2 and in that case because it is the worst case condition for the minimum delay constraints.

We have to ensure that the combinatorial circuits t_{cd} the contamination delay should still not violate the hold time failures. If I have the clock here and then the dotted lines as the skewed clock. I am saying that the clock is arriving early for the first flop and clock is arriving late for the second flop.

What we really need to do is even if it is a skewed 1 we need to ensure that the f2 does not capture the signal the contaminated signal in the first clock itself. The f2 signal should actually capture in the second clock edge and it should not capture in the dotted lines here which is a clock which is actually skewed. It should get captured here in the dotted lines of the second clock.

What we need to do is the even if there is a contaminated output. We should ensure that it surpasses this hold time failure with respect to this skewed clock. In that sense if the D1 signal arrives early before this particular clock for the flop 1 just before the t setup time. Then the Q1 you can get the contaminated output coming from the t_{ccq} of the flop 1 designs and then the combinatorial circuit will pass a contaminated output after the contamination delay here and we will have a t_{cd} with respect to the Q1 signal and then we have the D2 signal here t_{cd}.

Now, this D2 signal should arrive it should make sure that the D2 signal arrives after the t hold time. The t_{hold} for the flop 2 is now with respect to the skewed clock and the skewed clock is designed by this dotted lines is given by this dotted line, the t_{hold} is with respect to this dotted line.

We need to ensure that the D2 signal arrives or surpasses after the t_{hold} for the flop t. That it does not sneak in the first clock edge of the skewed clock, but rather it should be made available in the second clock cycle of the for the flop 2 designs. By looking at this particular timing diagram. We can easily say that the,

$$t_{hold} + t_{skew} \leq t_{ccq} + t_{cd}$$

The t_{cd} the minimum delay constraints should be for designing the combinatorial circuit is a,

$$t_{cd} \geq t_{hold} + t_{skew} + t_{ccq}$$

Remember that with the t_{clock} skewing this hold time effectively increases. Earlier we we are having the same ideal clock arrival time for the all the flops we did not have this t_{skew} parameter at all and my $t_{cd} \geq t_{hold} - t_{ccq}$ which is much more easier to design.

But now because of the addition of the clock skewing the t_{cd} value has a kind of further increased. Remember for any kind of a combinatorial circuits we have to ensure that it is characterized by the t_{pd} parameters and t_{cd} parameters. In this case the t_{cd} increases because of the t_{skew} and then in the earlier slide we have seen that the t_{pd} decreases.

The more and more this t_{cd} and t_{pd} comes closer it becomes difficult you as a designer it becomes difficult to design the circuit. If there is a more margin here t_{pd} and t_{cd} is it is much much easier to design the combinatorial circuits.

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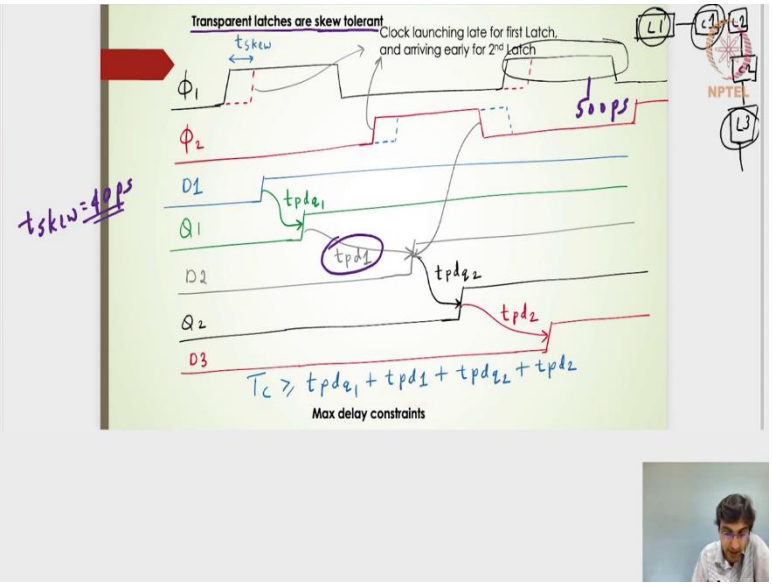

Moving on let us take a look at the clocks skewing effect for the latch designs, again here is I am directly giving the timing diagram for the latch design, but the latch design here it is pretty similar to what we had seen L1 going to the combinatorial circuit here. Circuit number 1 and then that goes to the latch design L2 and then that goes to the combinatorial circuit number 2 and then that goes to the latch L3 and then so on.

This L1 L3 and all are operating at the clock 1 ϕ1 clock and then L2 L4 and all the even number of latches are operating at ϕ2 of the signal. Here in this ϕ1 of the signal because it

is a propagation delay what we are saying is for L1 and L3 and L5 and so on the clock is arriving late.

The clock is launching late for the first latch and arriving early for the second latch. That will be the worst case condition which will ensure that the t_{pd} value of that we will have to design for the combinatorial circuit 1 is actually because there is this skewing factor and it has to be slightly reduced.

What we have seen for the flip flop designs, but in this transparent latch notice that the t_{skew} factor will be around 40ps, but the clock level being high, it will be available for almost around 482 or 500ps.

The clock level being high or the $\phi 2$ clock level being high will be around close to 500ps whereas, the clock skewing will be somewhere around 40ps. With this particular parameter one can actually say that if the clock level high is around 500ps. Then there is a skewing effect the D1 signal although if it arrives during the clock level high. This skewing which is around one tenth of the 500ps. In fact, less than one tenth of the 500ps it will not have that much of an effect.

Even if the D1 signal arrives in between after the late clock Q1 will get easily captured there will not be any effect here whether the skewing is there or not and then the D2 signal will be nothing, but the output of the combinatorial circuit number 1. It produces after the tpd1 and then the latch number 2 will give the output after the t_{pdq} of the latch number 2 and then the combinatorial circuit number 2 will throw the output after the t_{pd} of the combinatorial circuit number 2.

$$T_c \geq t_{pdq1} + t_{pd1} + t_{pdq2} + t_{pd2}$$

In this case because the t_{skew} is actually very very minus in terms of the clock level being high which is around 500ps. We can easily in fact, this the latch designs are really skew tolerant. What the skew if the skewing is there then also it will not have any effect. The latches or the transparent latches designs are said to be skew tolerant. Even if the skew is there it will not get reflected at the output. The maximum delay constraints, does not have especially for the transparent latches it does not take into account this skewing effect.

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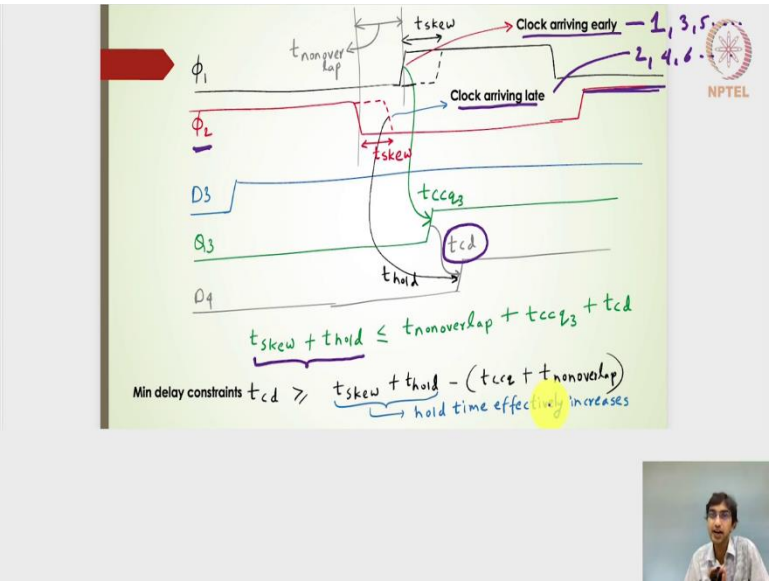

Hope this is clear, but it will have an effect in the minimum delay constraints especially for the transparent latches. Even if I have a transparent latches in the same data path sequence of latch 1 followed by combinatorial circuit number 1 followed by latch number 2 followed by combinatorial circuit number 2 and then latch 3 and then so on.

Then I will have this as a clock designed and then for the minimum delay constraints we will take the opposite as a worst case for the latch number 1 3 and 5 we will say that the clock is arriving early and latch number 2 4 and 6 we will say that the clock is arriving late. In that sense I will have this skewed clock determining the output of the latch number 2 4 and 6 or the even number of latches whereas, the clock arriving early we will consider it for the latch 1 3 5 all the odd number of latches.

This is what the clock is designed and then the ϕ2 clock will also have the similar the clock skewing circuit. Here is the clock skewed which is arriving late and then the clock arriving early clock arriving early is for the first third fifth and so on. The clock arriving late is for second 4 and 6 and then so on.

In that sense if the D3 signal is available then D3 signal is going to the latch number 3. I should consider this particular clock, that output of Q3 the output of the latch number 3 with respect to this clock it will produce after the ccq3 which is contamination clock to Q3.

Then the contaminated output then goes to the combinatorial circuit number 3 the output of that will be given to the latch number 4. That D4 signal is the output of the combinatorial circuit number 3 and it is going to produce after the t_{cd} time the contaminated output.

We need to ensure that this contaminated output should surpass the first high level or the rather the delayed or the clock arriving late signal and then the first level of the clock arriving late signal and a with respect to its t_{hold}. That it will be captured in the clock skewed clock for the high level of the $\phi 2$ signal. It will be captured in the second high level of the $\phi 2$ signal although it is skewed that is perfectly fine, but it should surpass the t skew and the high level of the $\phi 2$ signal clock signal. In that sense the clock skew is there and then this t hold time is there. What we need to do is this,

$$t_{skew} + t_{hold} \leq t_{nonoverlap} + t_{ccq3} + t_{cd}$$

$$t_{cd} \geq t_{skew} + t_{hold} - (t_{ccq} + t_{nonoverlap})$$

What we are saying is the hold time effectively increases because of this skewing effect although this is a worst case.

What we are saying is we consider the worst case because we really do not know the placement of the flops. We consider it to be a worst case because we know the characteristics of the flops. If it is placed farthest we know what is the t skew time and we will utilize that to make sure that the combinatorial circuit that is placed in between the flops or in between the latches it is still able to surpass the hold time failures.