Design and Analysis of VLSI Subsystems
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Lecture - 75
Static Timing Analysis

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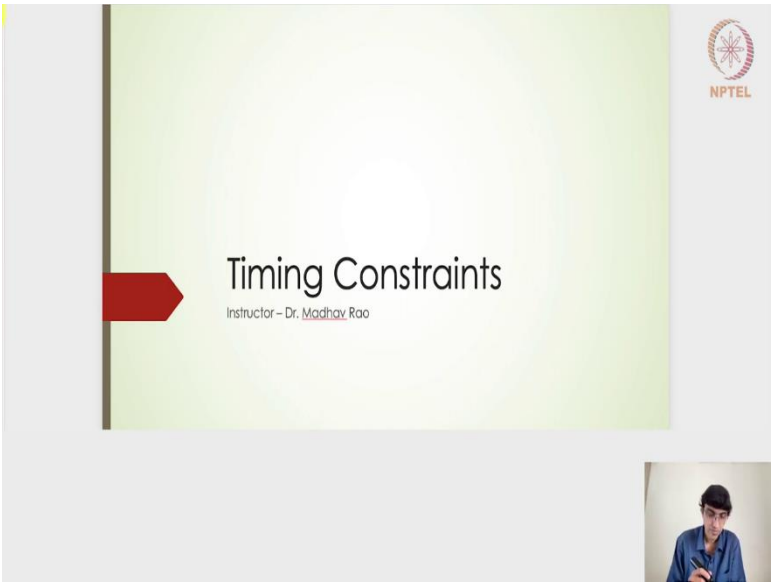

Hello students. Welcome to this lecture on the Timing Constraints. In this particular lecture, we will look into some of the static timing analysis the parameters especially the setup and the hold time and for two different circuits, one is the CMOS latch design, another one is the flip flop designs. What we are going to do is try to evaluate or try to express to some extent what is the setup and hold time with respect to the propagation delay of the circuits of the digital blocks which we have been using in the latch and the flip flop designs.

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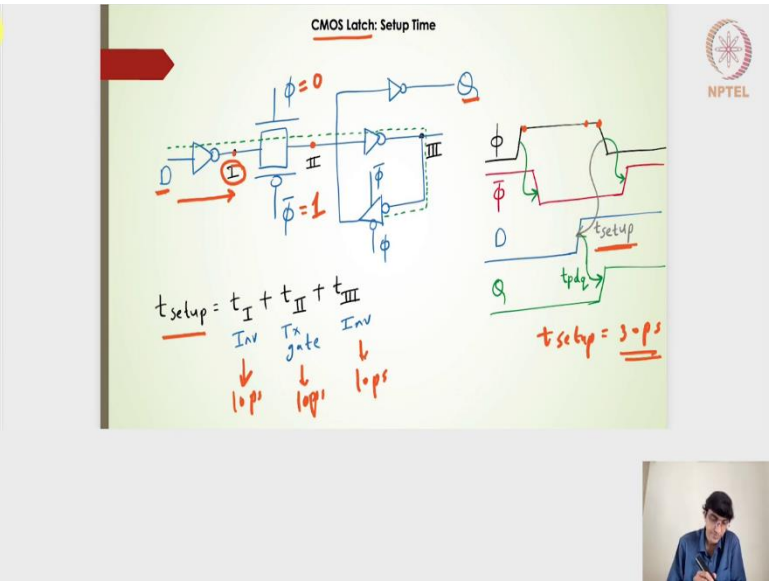

This is the CMOS latch design which we had seen, I think this is the circuit number 7 which we had seen in the previous lectures, where we had the inverters and then the transmission gates.

Followed by the inverters and in the feedback path we had the tri-state inverter to ensure that this particular node is statisized. The output node getting isolated from the X node, we bring in the inverter here and then the inverter here is to ensure that the input noise is not passed into the circuit and this particular inverter is to ensure that the output is isolated from any kind of a noise and getting it back into the X node or to the latch circuit. This forms the complete design which takes care of all the problems associated with the their latch design.

Now let us look at this particular timing diagram here. I have a clock here the high level of the clock that is when we should be able to get into the transparent mode that means, the output Q should reflect to the changes made at the input side. Based on the clock here, the high level of the clock, I have whatever is the input that is been passed, I will get it at the output side. Now, the question is how far or how late the input can be passed, the input changes can be passed within this clock level high? The output will be able to capture it properly.

How late in the sense whether the question is, while the clock level is high in this particular time period or rather in this particular duration, can I send the changes at the input side at

the D side somewhere here. Whether the output will be captured properly or should I need to send it somewhere at this particular portion, that I will have some amount of time, that the output will be able to capture.

Here you know that is kind of defined by the t_{setup} time for the CMOS latch design. The t setup time says that the input should be passed at least before the t setup time of the of falling edge of the clock, so that the output will be captured properly. Thus, this tsetup time ensures that the input should be passed at least before the t_{setup} time with respect to the falling edge of the clock for a high level of a latch design. If it is a low level of a latch design, this t_{setup} time should be for the rising edge. The t_{setup} time is defined, such that the input if it is passed before the t_{setup} time of the falling edge of the clock in this particular case I will get the output to be nicely captured by the latch design.

Now, how do we characterize this t setup time? here I have said that t_{setup} time is nothing, but the delays that is passing through this digital blocks or that this digital gates, the inverter here, the transmission gate here, and this particular inverter here. I have written the output 1, of the output 1 represents the output of the first inverter second represents the output of the second stage, which is nothing but the transmission gate.

Third represents the output of this inverter which is the third stage. I have drawn the dotted lines showing that it should have the D should be made available before the falling edge. This particular dotted line says that the signal should have enough time, the signal that is passed with the D input should have enough time to propagate till it reaches here before the clock going low.

The t_{setup} time is actually characterized as the propagation delay of this particular inverter, the propagation delay of this particular transmission gate, and then the propagation delay of this particular inverter, it is made available till here.

$$t_{setup} = t_{\substack{I \\ inv}} + t_{\substack{II \\ Tx \\ gate}} + t_{\substack{III \\ inv}}$$

Now, let us take some cases to validate this particular definition of the t_{setup}. Let us say what happens let us bring in some example of this being 10ps and this being 10ps and this also being 10ps. I have just taken it for the simpler understanding.

All of them are 10ps. The total t_{setup} time should be 30ps. That means, the input should be passed atleast 30ps before the clock going low. That is when the output we can say that we can confirm that the output will capture the changes in the D signal.

For example, let us say that the t_{setup} time is set to 30ps. But my clock comes in only just before 10ps of the input comes in only 10ps just before the clock going low. The input comes in only at 10ps before the clock going low. If that is the case, if the input comes in, it takes 10ps to reach to the first portion or rather to the first stage and after that the clock is going low.

After that the clock goes low. That means, this will be 0 and this will be 1, the transmission gate will be off. That means, this particular whatever the signal it has reached here due to the changes in the D is not propagating or it is not passing to the other side because the clock is low that means, that the transmission gate is off now, it is not going to capture whatever is provided at D. Q will not capture whatever is provided at the D signal.

Now, what happens if t setup time is 30ps, but the D signal is passed instead of 10ps, let us increase it to 20ps? It is not 30ps yet. What happens if it is 20ps?

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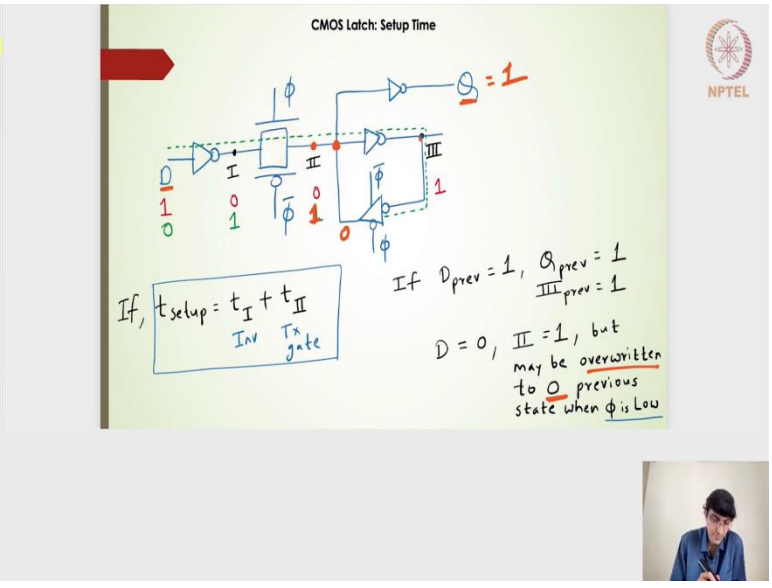

The input signal is passed 20s just before the clock going low. That means, if the input signal is passed only 20ps. It is able to pass this particular inverter. It is the signal will be

propagating to this particular portion, and after that the clock is going low, the transmission gate will be off.

After that it goes low, but by the time it goes low or this particular transmission gate is off we have anyways have the signal here. Then in that sense the Q should be able to get or capture the valid D signal. But does not happen because it still needs to propagate to this particular inverter and then through this tri-state inverter and then push this Q signal.

What really happens is if it is only 20ps, but the setup time is 30ps then in that case, if the signal whatever is the D signal is been propagated into the node number 2 and then this transmission gate is off. That means, that it does not have any kind of a driving capability coming from this particular inverter because this is off. This inverter will actually ensure that the two node is driven to either by the V_{dd} rail or to the ground rail, that does not happen. That particular channel is switched off.

Although this two, signal is high or low, the previous state signal is still here, this tri-state inverter is now getting activated because the clock has gone low. That means, that the tri-state inverter is now activated and then the previous state signal is going to switch on the transistors here. This particular tri-state inverters, the transistors there is going to be driven by the V_{dd} or the ground rail based on the input here which is nothing, but the previous state. I will get back the previous state output here and then thereby the Q will be reflecting the previous state output and not the one which is kind of recently updated by the D signal. Just to take an example. Let us say that if I say that t_{setup} which is kind of wrong here.

$$t_{setup} = t_{\substack{I \\ inv}} + t_{\substack{II \\ Tx \\ gate}}$$

I am not taking the inverters propagation delay at all here. What really happens? If that is the case, the D previous let us say the previous value is 1 and then here it was 0, it was 0 here, and then it was 1 here, this 1 was fed back to 0 here, and then the Q was nothing but 1, previously.

But now there is a change here, D is 0 now. That 0 is getting reflected into the 1 node as 1 here and that 1 is getting it is passed by the transmission gate as a 1 here. But after that the clock goes low, that means, that the clock goes low that means, this particular tri-state inverter is going to be driven by the input of 1 here and not 0 because it still not has passed

to this to this particular inverter because we are not accounted for this particular propagation delay.

Although this is 1 here, but it does not have time to make the 0 here and the previous state is 1 here. This is going to get driven the output will be 0 here, which is going to get driven by this tri-state inverter. Instead of 1, it still shows the previous state 0 and then the previous state of 1, that is what I have written here.

It may be overwritten to the 0 here because of the previous state because the clock goes low. The t setup time has to consider this particular inverter delay also. It has to consider this particular inverter delay. It has to consider this particular transmission gate delay as well. Hope this particular example makes it very clear.

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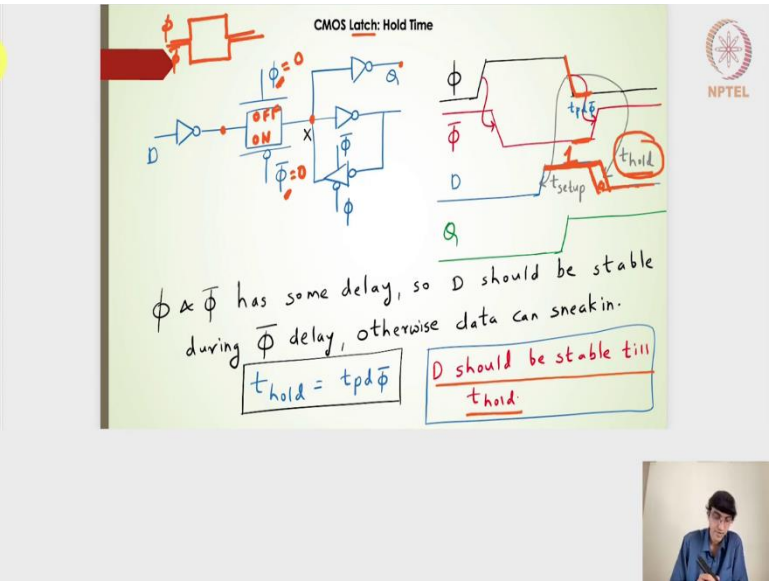

Now, the other significant static timing analysis parameter is the hold time. What is this really the hold time? this is again the latch design which we have been seeing, the most recommended latch design.

Now, remember that I have noticed that the ϕ and $\overline{\phi}$ here. One goes to the NMOS transistor, the other one goes to the PMOS transistor. We always up till now we have been considering the clock, whenever the clock changes from high to low and then low to high, we said that it will be ideal. The $\overline{clock}$ also changes at the same particular time which does not happen always.

There will always be a delay between the clock and then the $\overline{clock}$ signal because this $\overline{clock}$ signal is actually generated from the clock signal. Of course, there will be an inverter and then the inverter is going to drive that complementary output. The $\overline{clock}$ is always behind the clock. There will be a delay here. In this case, the designed the clock signal and then the clock power signal, there is some kind of a delay here. This particular delay I am calling it as propagation delay of the $\overline{clock}$ signal, that is why I have written t_{pd} and then the $\overline{clock}$ signal.

if I now consider the D input signal here. Let us say that it is coming it is satisfactory, it is satisfying the D setup time constraint. it is coming before the t setup time just before when the clock goes low before the D setup time and then it has to stay till the hold time of the clock going low.

If it does not stay there, if the D signal does not stay consistently for the t_{hold} time. That means, that the D is coming back low or it is kind of fluctuating or it is not staying at the signal we want to capture, it goes back to 0. There is a possibility that when the clock goes low here from 1 to 0. This NMOS transistor will be off, but this particular PMOS transistor because of the delay because of the delay, this is still 0. It takes some time to go from 0 to 1. In that sense this will still be on for some while during this particular portion where this is low and then this is also low and after that will going to be high.

The $\overline{\Phi}$ is low. Whatever changes happens at the D can get reflected here and can get passed to the X node and then can get reflected at the Q node. If it is really the contamination delay which is really fast which is very very low, its contaminated delay can go here, contaminated delay makes the signal go reach here and then reach to the Q output.

In fact, we will be capturing a wrong signal whereas, we the intention is to capture this change in 1 here. Whatever the fluctuations happens at the D side before that can get captured. What we really need to do is ensure that the D signal is staying, even after the clock goes low the D signal stays to the expected input to the expected input. So, that it will be able to capture the expected output signal. It stays low, it stays to that particular signal level till the t_{hold} after the clock goes low.

$$t_{hold} = t_{pd_{\bar{\Phi}}}$$

After this particular edge whatever is the t_{hold} time it has to retain, it has to stay there for that t_{hold} time after the clock going low, after the clock edge the negative clock edge for the positive latch design, ϕ and $\overline{\phi}$ has some delay. The D should be stable during the $\overline{\phi}$ delay otherwise the data can sneak in. Whatever is the changes here can directly get sneaked in into the Q. The t_{hold} this as per our definition it is nothing, but the delay that it takes for the $\overline{Q}$, the propagation delay for the $\overline{Q}$ signal, this D should be stable till the t_{hold} time.

In fact, whatever is the stable D it should be retained for $t_{setup} + t_{hold}$ time, so that we will get the proper output or an expected output at the output of the latch. It should be stable for the t_{hold} before the clock edge going low and t_{hold} after the clock edge going low, that we will get the expected output. Hope this is clear.

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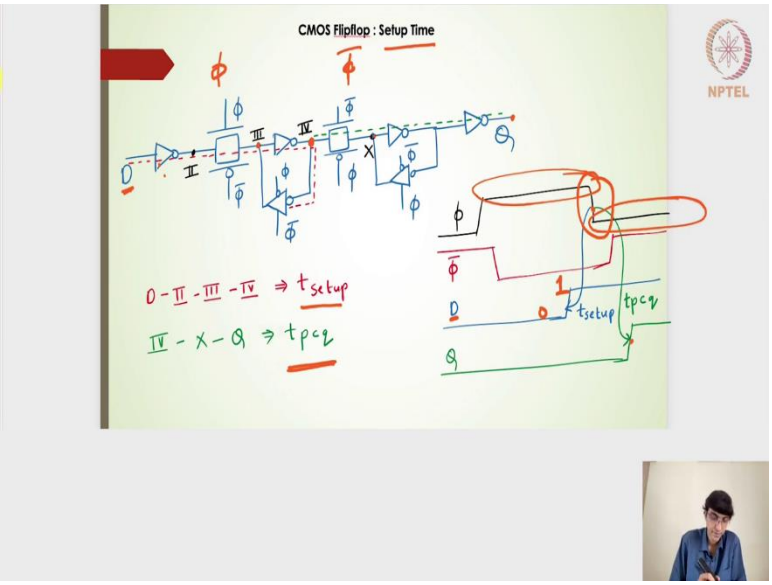

Let us try to understand what is the setup time for the flip flop designs. For the flip flop designs again if I am considering the negative edge flip flop, remember that for the latch design we had considered the positive level of the latch.

For this particular flip flop design, what I have considered is the positive level of the latch first followed by the negative level of the latch. It is a basically an, negative edge triggered flip flop and its definition of the setup time is also very very similar. I have drawn a clock signal here and then a $\overline{clock}$ signal here which will have some kind of a delay.

The D input, the question for the setup time is always what should be by far the most farthest signal that I can pass, that it will be able to capture the signal at the output of the flip flop. The answer is nothing, but it should be made available at least before the t_{setup} time of the clock going low for the negative edge flip flop. For a negative edge flip flop during this particular edge only whatever is the changes happens just before the t_{setup}, if the D has to go from 0 to 1, so that 0 to 1 has to happen now. At least before the t_{setup} time of the negative edge of the clock, that the output will be able to capture it properly.

The t_{setup} time again its definition, it says nothing, but the propagation delay of this particular inverter plus the propagation delay of this particular transmission gate plus this particular inverter. If we have then the signal whatever is the changes here will get propagated until this point nicely or properly or expectedly and then whenever the clock changes from high to low, this particular latch design will be on and then the changes here will be reflected into the Q output. We will be able to capture the output based on the changes of the D signal.

But if I do not do, if I have this the D signal arriving just after the t setup time requirement, even in the previous case where we had 10ns, 10ns and 10ns, but the D signal was arriving at 20ns, then it is able to pass up till here. But then because of this previous state, this signal will be overwritten by the previous state and then when the clock goes low we will have the previous state signal.

The similar things are expected even in the flip flop design. The t_{setup} for the flip flop as well as the negative level of the latch design remains the same. It is nothing, but this inverters propagation delay that is this particular transmission gate and then this particular inverters delay.

Now, what should be how much time it takes once the D is passed before the t_{setup} time, there is no setup violation. How much time it should be able to generate the output signal? That particular propagation delay from clock to Q is given by t_{pcq}.

The propagation delay of clock to Q it is nothing, but once the signal has reached here and it is waiting for the clock to go low. That is when it is doing the transition from high to low. During this particular high one the first latch will be on and then during this particular level the second latch will be on.

The output of the 4th node which is kind of made available because the D signal has arrived sufficiently before the t_{setup} time. The 4th node signal is available and it is just waiting for this latch to get activated. This latch whenever it becomes low this 4th node signal whatever is there it is getting reflected, it is getting passed to the output node. That particular propagation delay from 4th node to the Q is called as the propagation delay clock to Q.

Whenever the clock goes low here the transmission gate delay followed by this particular inverters delay plus this inverters delay will be nothing, but a t_{pcq}. Starting from 4th to the through the X node through the Q node is our propagation delay clock to Q. There is another parameter for characterizing the flip flop designs. We have now seen the setup time as well as the propagation delay clock to Q for the flip flop designs.

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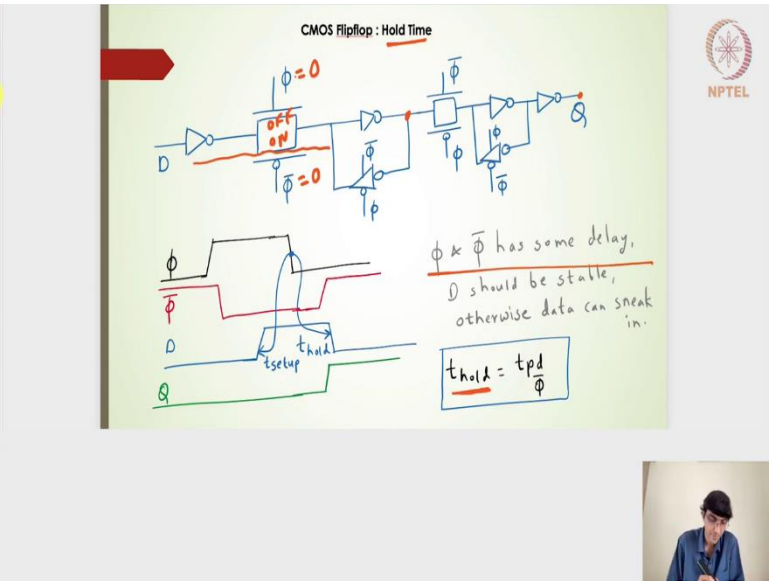

The flip flops again what is the hold time? Again, what we had seen in the latch design is that the D input should stay even after the clock edge going low for the hold time. It should stay at least for a hold time. Even in this case because the ϕ and $\overline{\phi}$ has some delay, D should be stable otherwise the data can sneak in. The D should be stable or till the hold time has reached and then we will get the expected output.

Otherwise, what happens is because of the delay in the Q and $\overline{Q}$, even if the Q is low $\overline{Q}$ will still be low for some duration. Even if the NMOS transistor is off we will have the PMOS transistor on for a certain duration and then the signal the changes here, even in

between the clock edge and then the t hold time if at all the D signal changes here is going to get sneaked into the output node here. Whenever it goes low this can get reflected into the output.

We should not change the D signal before the t hold time, it should be changed at least after the t hold time. It should be held, the D signal should be held for a particular duration that is the t hold duration even after the clock edge going low. The clock edge and the t hold are also defined as nothing, but the t_{pd} $\overline{clock}$. The propagation delay of the clock complements of the clock that is being generated from the clock signal, very very similar to that of the latch designs definition.

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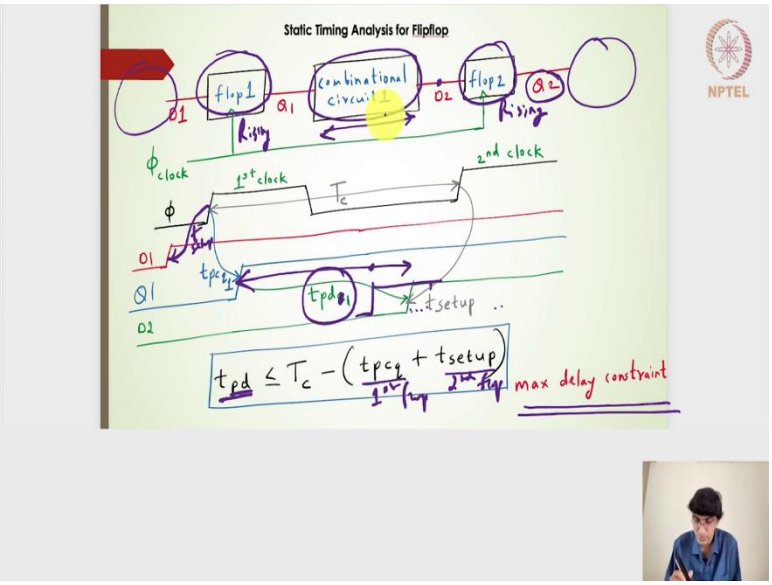

What we have seen is a flip flop in the latch designs and it is a setup time, hold time, and especially for the flip flop we also took into account the propagation delay, clock to Q. Now, let us try to put this and try to see how do we actually use that.

Let us say that in our combinational circuit design, especially in the system on chip where there is one particular computational block. I have written it as a combinatorial circuit, it could be a computational block, it could be a multiplier 8 bit, 16 bit or whatever it is. Then on the two other side we have set up the flop design, so that we can time the output and that the timed output can then be going into some other part of the circuits.

If it is a timed output I need the flop designs, I need the flop designs or the latch designs, in this case I have taken the flop designs. The flop 1 and flop 2 which is nothing, but the flip flop 1 and flip flop 2. The flip flop 1 and flip flop 2 is characterized by the setup and the hold time.

Let us say that both the designs are very very homogeneous that means, that the same transistor bits and everything is the same. In that sense, this t setup time and then the t setup time as well as the hold time as well as the t_{pcq} everything of both the flip flops are same. Then this is a combinational circuit and at this particular point of time, as a designer we are specified to ensure that there is no setup time failure. What I mean by the setup time failure is given this clock signal, which is the same for both the flip flop 1 and flip flop 2 and this is a clock signal of certain particular frequencies, this is the first clock, this is the second clock.

What are we supposed to do is make sure that the combinational circuit gives the output, takes the input in the first clock and gives the output in the closer to the second clock. But without the setup time violation, if I have the D1 signal whatever is the combinatorial circuit coming or the output is providing into this particular combinational circuit, that will be my D1 signal. If the D1 signal let us say it is available much before the t setup time of the flop 1, then it can get easily captured and of course, it stays after the t hold time also. But I have not drawn that.

The Q1 is going to give me a proper output based on the D1 signal. The Q1 is going high only after the clock and let us say that this is a rising edge. This is a rising edge of the clock, let me write it rising edge, and this is also a rising edge. Last previous examples or previous definitions was with respect to the falling edge. Here I have just to make it very simple I have done taken it as a rising edge of the clock. The rising edge of the clock what the setup time and hold time is with respect to the rising edge of the clock and the propagation clock to Q is also with respect to the rising edge of the clock.

Whenever the D1, let us say that it has arrived much before the t setup time. I will get a proper expected Q1 after the propagation clock to Q. Propagation clock to Q1 will be nothing, but the inverters the transmission gates and then the inverter and inverter. The delay of the transmission gate, the delay of the inverter and the inverter will be nothing but the propagation clock to Q.

Let us say that the combinatorial circuits takes its own propagation delay. It will have its own propagation delay t_{pdq} propagation delay for Q1 to generate the D2 signal. That is what we have t_{pd}. In fact, it should be written as t_{pd1}.

Now it is available for the flop 2 and we are saying that it reaches much earlier than the t setup time for the second clock, because we are making sure that the combinatorial circuit does the computation, and then it generates the output which is timed circuit. What it means is this particular computation the output of that will be made available in the second clock edge for the next combinatorial circuit.

Its input has come in the first clock and its output is available in the second clock. What it means is the combinatorial circuit is generating the signal and then making it available in the second clock for the next combinatorial circuit.

In that sense it should provide the output at least before the t_{setup} time. Now, what should be this tpd1 then? this is my clock time period Tc, this is the delay t_{pcq1} coming from the flop 1 design. The t_{setup} of this second flip flop, it should ensure that the output should reach before the t_{setup} time, so that my Q2 will be captured properly

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup})$$

T_c is the overall clock time period which can also be defined by the frequency of the clock. The t_{pd} this is the maximum delay that I can provide that I can use to design a combinatorial circuit, that is why it is called as a maximum delay constraints. If this t_{pd} goes beyond this particular maximum delay constraint. Let us say that the maximum delay constraint is 1000ps followed by this particular calculation on the right hand side.

The T_c minus the first flip flop plus the second flip flop t_{pcq} and t_{setup}, respectively. If it turns out to be 1000ps, but my t_{pd} the propagation delay of the combinatorial circuit is 2000ps, then what is likely to happen is this D2 signal is going to take more time, it is going to take more time. Either the second clock is not going to capture the Q2 signal at all or if it falls in between this setup time and then the clock rising edge, then the output is not going to capture it nicely.

In that sense the t_{pd} should be actually be designed less than or equal to this maximum delay constraint, which is nothing, but $T_c - t_{pcq} + t_{setup}$. In fact, have this T_c, t_{pcq} and then the t_{setup} and we have only this particular duration to design our combinational circuit.

The lower it is the better it is because lower means it will arrive at somewhere here it can arrive at somewhere here, but it cannot go beyond this t setup time. Remember that for normally in our designing, the digital blocks, the combinatorial circuit design is something which we will have to do it.

The other designs like the flops and the latches which we are anyways going to take it from the standard cell library design, those particular t_{setup} and then the t_{pcq} parameters are already defined. We do not have an allowance to change the properties of t_{pcq} in t_{setup} or the t_{setup} of the flip flop designs. The only thing we can change is change the combinatorial circuit, so that the propagation delay is adjusted, so that there is no setup time violation.