Design and Analysis of VLSI Subsystems
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Lecture - 73
CMOS Latch Design

Hello students, welcome to this lecture on the CMOS Latch Design Part 2. In this particular design we will have a look initially we will have a look into the tri-state inverter and how it is closely matching with that of the inverted buffer design. The tri-state inverter will use it in the feedback part of the latch design.

So, as to overcome the dynamic node output voltage, which was kind of which remained to be floating and during an opaque state it, due to the sub threshold leakage current it can get dropped and change the output node voltage. In that sense the tri-state inverter design is kind of very important to understand and then try to use that in the feedback path so that we can have a staticized output node, instead of a dynamic or a floating node output voltage.

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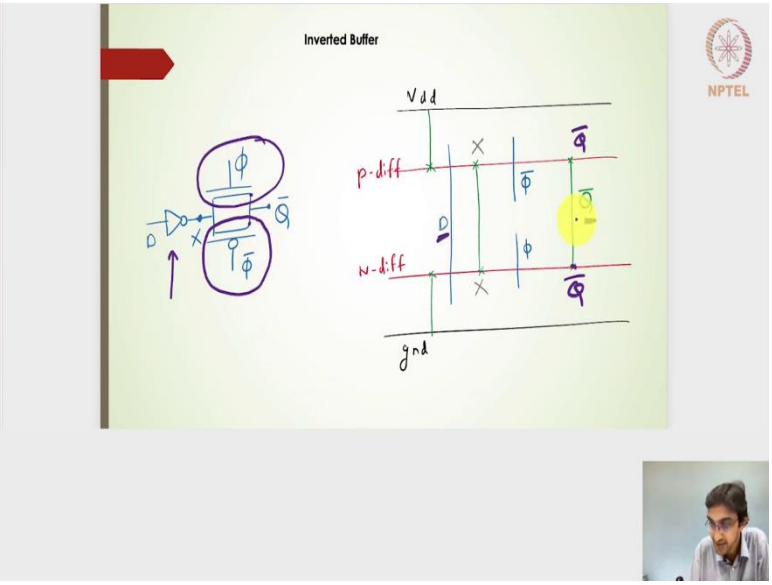

Moving ahead let us have a close look at the inverted buffer. The inverted buffer design, we have an inverter here followed by the transmission gates. The clock is provided to the NMOS gate and then complement of the clock signal is provided to the PMOS gate. To

understand the difference between the inverted buffer and that of a tri-state inverter design, we need to understand these stick diagrams.

In fact, to understand the differences or the similarities of the inverted buffer with that of the tri-state inverter, we will have to understand the stick diagrams and that is why the stick diagrams have drawn here on the right side. If I want to draw the stick diagram of this particular circuit, which is an inverter followed by the transmission gate we will try to do it in a sequence.

Try to draw the stick diagram of an inverter. The inverter stick diagram is given by the p diffusion line and an N diffusion line also I have a V_{dd} rail and then a ground rail. We will have the D input here, which is separating the 2-diffusions on the p diffusion line and then 2-diffusions on the N diffusion line.

The inverter one diffusion line goes to the V_{dd}, on the p diffusion line and then the another diffusion on the N diffusion line goes to the ground, the other side is the output node which is nothing but the X output of the inverter. This X output which gets connected by a metal line.

This completes my inverter stick diagram follow that with a transmission gate. The transmission gate we will have $\overline{\phi}$ given as a poly silicon gate onto the p diffusion line and ϕ as a poly silicon gate applied on the N diffusion line. I have a ϕ signal and then a $\overline{\phi}$ signal, separating the diffusion pockets of the transistor. For an NMOS transistor we will have the ϕ poly silicon gate and on one side it is the X node and the other side it is the $\overline{Q}$ signal.

This is the $\overline{Q}$ signal and then one side it is the X node. The PMOS transistor here of the transmission gate which sees a polysilicon gate of $\overline{\phi}$ and then separates out the diffusions of X and then the ϕ X in one side and then $\overline{Q}$ on the other side here. We will have this $\overline{Q}$. Remember that this $\overline{Q}$ the which is nothing but the diffusion of the NMOS side and then the diffusion on the PMOS side, has to be connected and that is been connected by a metal line in this stick diagram.

This is my input for this particular circuit design, which is nothing but an inverted buffer. This is the input and then this is the $\overline{Q}$ output, this is the overall stick diagram of the inverted buffer.

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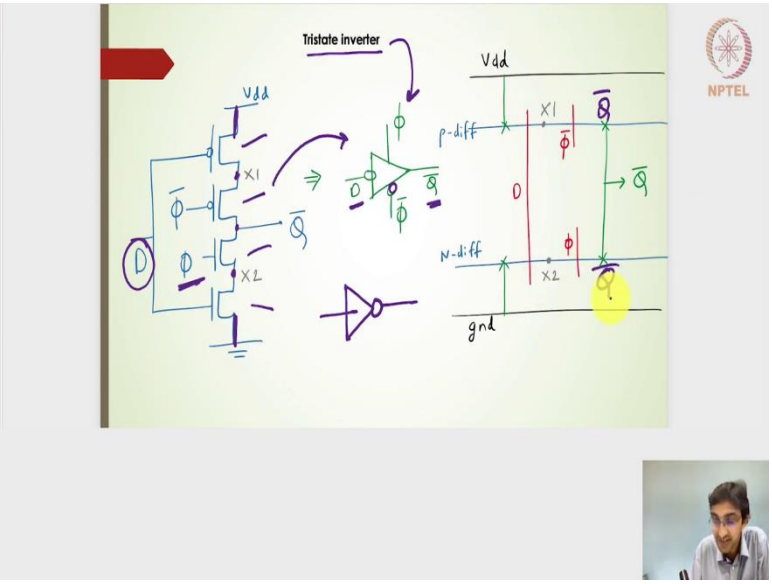

Let us have a look into the tri-state inverter, the tri-state inverter we should have the pull down circuit as well as the pull up circuit are nothing but the mirror image or a mirror topology, what we call or refer to. I will have the D input given to the transistors, which are closer to the V_{dd} and the ground rails. The other 2-transistors which are closer to the output node is supplied with the clock signal ϕ and $\overline{\phi}$.

In fact, it is kind of symbolized with the help of an inverter kind of a symbol, but inverter is nothing but we have an output here, which is bubbled instead of that for a tri-state inverter the bubble comes on to the input side and the clock signal, because it is a tri-state. We in fact, have 2 pair of signals, one is the input signal the other one is the clock signal. The clock signal ϕ and $\overline{\phi}$ is also inherited in the symbol design.

A tri-state inverter is kind of represented by this particular symbol, where we have the bubbled input and then the clock and then the output. Remember that the output is $\overline{Q}$, the input is D and the clock supplied to the NMOS is ϕ, the clock supplied to the PMOS is $\overline{\phi}$ and that is why we have this bubbled input, which is going to the $\overline{\phi}$ representing that this represents the PMOS transistor and this represents the NMOS transistor.

Coming back to this particular schematic in terms of the transistor level schematic and then trying to draw that on the stick diagram. We have four transistors, the four transistors have to come that means, I need to have 2 transistors, 2 transistors on the PMOS side and then 2 transistors on the NMOS side.

The 2-transistors has to be visualized on the stick diagram, on the p diffusion line and then 2 transistors has to be visualized on the NMOS diffusion line. If I consider this particular transistor and this particular transistor, I should have an input signal of D that means, a polysilicon gate of D which is cutting the p diffusion line into 2-diffusion pockets and cutting the N diffusion line, into 2-diffusion pockets. This particular diffusion pocket is going to the V_{dd} rail and then this particular diffusion pocket on the N diffusion should go to the ground and that is what is happening here and here.

The other one is this division pocket X1 and X2. I just left it as X1 and X2 here, $\overline{\phi}$ polysilicon gate applied on the p diffusion line will create 2-diffusion pockets X1 and $\overline{Q}$. The $\overline{\phi}$ is cutting the p diffusion line into X1 and $\overline{Q}$. This is $\overline{Q}$ and similarly ϕ poly-silicon gate is going to cut the NMOS or rather N diffusion line into 2diffusion pockets of $\overline{Q}$ and X2. The $\overline{Q}$ here and X2 here, this is the stick diagram of the tri state inverter.

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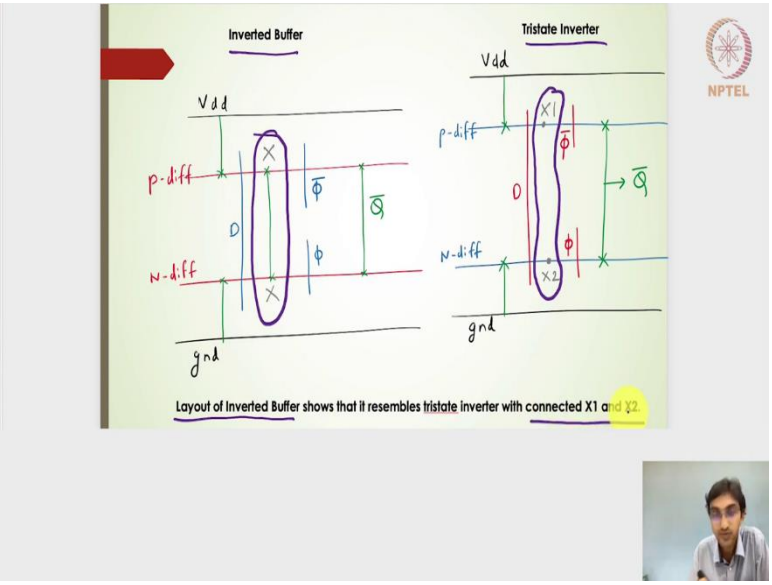

Looking at the inverted buffer and the tri-state inverter stick diagrams and if I actually put it nearby we can clearly see that there is only one metal line difference, everything else remains the same in the strict diagram, X and X are connected, here X1 and X2 are not connected.

If I connect this, this particular stick diagram, in fact if I draw the stick diagram of a tri-state inverter and then connect these two nodes or the diffusion lines, diffusion points into a metal through a metal line then I actually get the inverted buffer design. The layout of

the inverted buffer shows that it resembles very very closely to that of the tri-state inverter, with the connected X1 and X2 line.

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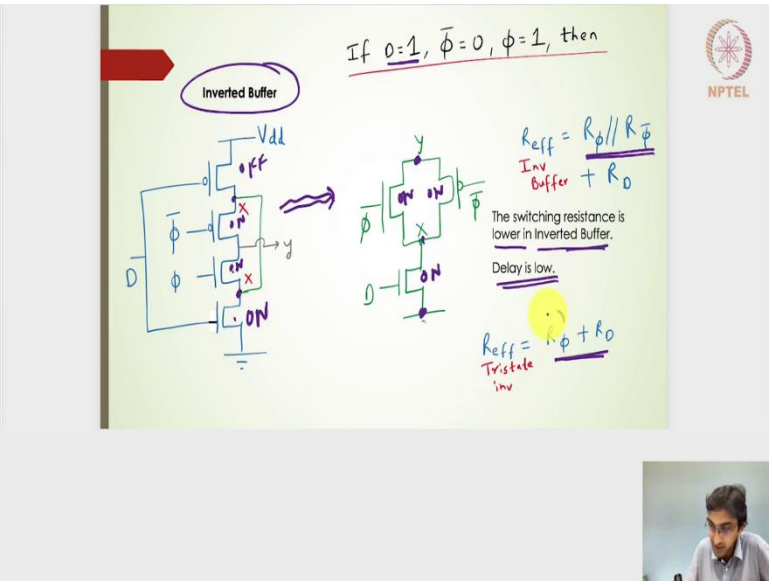

What it really means is, in terms of the stick diagram or rather in terms of the schematic the inverted buffer, I can actually draw the inverted buffer using the tri-state schematic by connecting this X1 and X2, by connecting or wiring or shorting it the X1 and X2 nodes and now after shorting it I am calling it as an X node.

The inverted buffer schematic is nothing but the tri-state inverter design with this two nodes shorted. Now, if I have these two nodes shorted what is the advantage we have? Now, whether we have an advantage in the inverted buffer with respect to the tri-state inverter and what is that? by adding an additional metal line in the layout of course, there will be some kind of, it will become a little bit costly in terms of fabricating the inverted buffer design. But with that what are we trying to gain?.

If we have this kind of a short circuit and let us say that the D = 1 here, D = 1 means I will have the NMOS to be on, PMOS to be off, $\bar{\phi}$ = 0 and ϕ = 1 that means, we have this to be on and on.

Then I will have this particular four transistors because this is an off transistor I can draw an equivalent circuit with only 3 transistors, where ϕ and $\bar{\phi}$ now are actually in parallel with respect to y node and X node, with respect to y and X it is in parallel. This X node

will be in series with that of the on transistor, that on transistor the NMOS on transistor which is connected to the ground.

This is an on transistor, this is an on transistor and then this is an on transistor and if I want to find out the switching resistance here and then eventually find out the logical effort. The switching resistance here is from the y to the ground here turns out to be nothing but this 2-resistance. This 2-transistor switching resistance in parallel with that of series of this particular transistor.

The switching resistance will be lower in the inverted buffer, than when we compare within the tri-state inverter because in the tri-state inverter I do not have this connection, I do not have this X1 and X2 node to be connected by a short circuit or a wire. I will not have these 2-transistors in parallel.

Having a parallel transistors, with a similar width is likely to reduce the switching resistance. Overall switching resistance from y to ground. If I have a switching resistance to be lower, then I will have the delay to be low. Whereas, in a R effective, the R effective switching resistance in a tri-state inverter it turns out to be nothing but one of them output node, one of them to be used for the switching resistance and then the other one this particular transistor.

For the falling down switching resistance, it will be this and then this switching resistance of this fall by switching resistance of this, that is what it will be. Here in the inverted buffer I will have a parallel component which will further reduce, than that of the R ϕ switching resistance.

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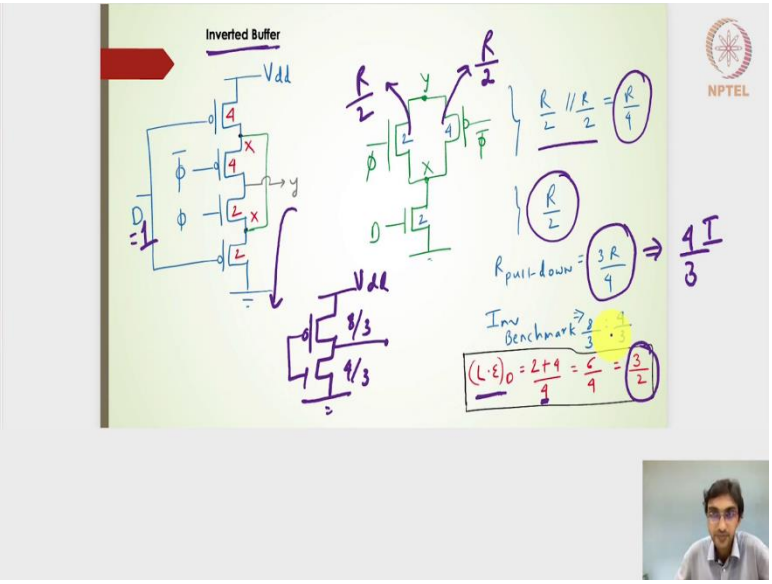

Let us try to quantify that effect. Let us have the width here a 4 4 2 2, that is what the width I have and if that is a width then for the inverted buffer design that means, that this nodes are connected. I am going to evaluate this overall switching resistance, especially if I am taking this particular case when D = 1 I will have the falling switching resistance.

The falling switching resistance turns out to be nothing but this resistance on the NMOS side, with the size of 2 in parallel with the PMOS transistor of size of 4 in series with that of the D transistor, which is on the NMOS side with the size of 2, and then connected to the ground. Here the size of 2 will give me a resistance of R/2. A size of 4 on the PMOS side is going to give me a resistance of R/2, I will have a R/2 and parallel with R/2 giving me R/4, in series with R/2, I will get,

$$R_{\text{pull down}} = 3R/4.$$

If I have a 3R/4, for this particular circuit design what should be my benchmark inverter? 3R/4 is going to give me a current of 4/3 I. I need a benchmark inverter which will give me 4/3 I. My benchmark inverter, just to find out the logical effort it will be nothing but an inverter. I am drawing an inverter, wherein the falling current should be 4/3 I and the rising should also be 4/3 I. My width of the benchmark inverter will be 8/3 and 4/3.

Now, if I have the benchmark inverter, I should be able to find out what is the logical effort for the D input. For the D input it turns out that the logical effort is

$$\text{L. E} = \frac{2+4}{4} = \frac{6}{4} = \frac{3}{2}$$

hope this is clear.

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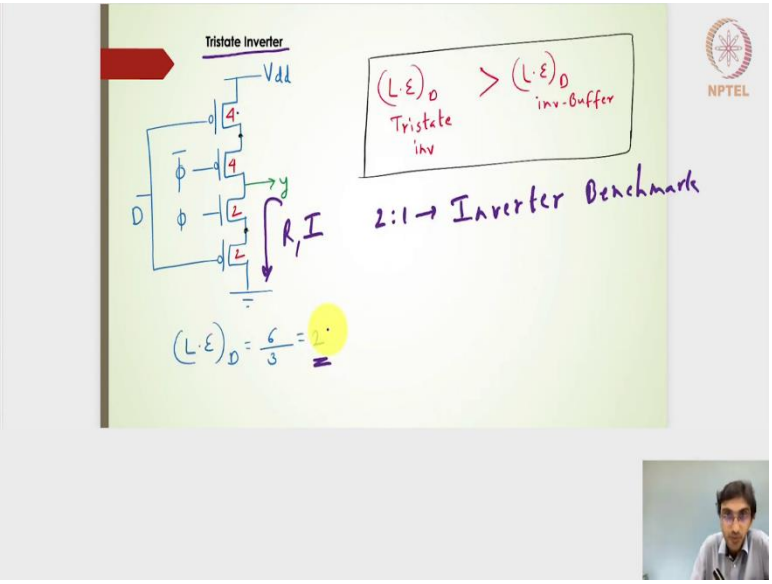

For the tri-state inverter having the same width of 4 4 2 and 2, the logical effort for the D signal turns out to be 4 and 2 and my inverted the buffer design is actually 2:1. The inverted or rather inverter benchmark inverter is actually 2:1, because my falling resistance is R, which will give me a current of I. I will have 2:1 inverter as the benchmark inverter. I will have the total logical effort of the D input is

$$\text{L. E} = \frac{6}{3} = 2$$

The logical effort of the tri-state inverter is greater than that of the logical effort of the inverted buffer. Inverted buffer just going to the previous slide, it is going to give me a logical effort of 1.5. Here the logical effort is 2.

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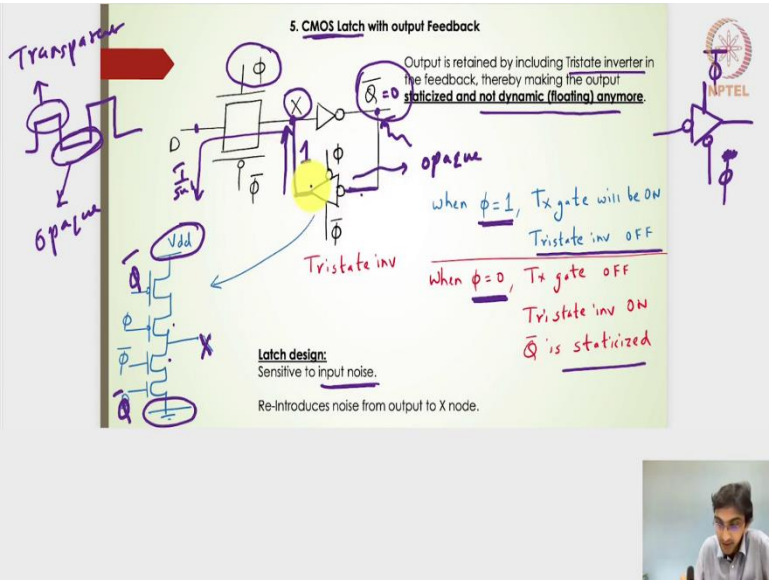

The logical effort is more, in the sense what happens is the overall delay will be higher for the tri-state inverter, but of course, I do not have to join the metal line in the layout and also that reduces to some extent the cost of the design alright. Let us use that particular tri-state inverter in our design and how do we use it? For a CMOS latch with the output feedback.

We have seen this particular transmission gate and then the inverter and then the disadvantage of this the transmission gate with that of the inverter was this output node was to be in a floating mode or a it was dynamic. Due to the sub threshold leakage current, it this X node will be dropped the node voltages at the X node will be dropped and it will have an effect on the $\overline{Q}$ signal. Now, what if I have a some kind of a feedback path wherein in the feedback path a tri-state inverter is applied and then connected to the X node.

Remember that in our previous case X was supposed to be floating node and X was floating and it used to you know this particular X node, the voltage of the X node used to get dropped due to the sub threshold leakage current, when it was in an opaque mode.

When it was supposed to retain the output node voltage for a longer duration, due to the sub threshold leakage current we analyzed or realized that the X node can get dropped. Now, what if I have to design a tri-state inverter such that it will drive the X node especially in an opaque state. Especially, when the latch is working in an opaque state. This part of the circuit should be operating in the opaque state that means, that I need to have a tri-state

inverter here, which will be working. Working in the sense, based on the input I will get the output to be driven by either by the V_{dd} rail or to the ground rail depending on the input here. But the clock at that level should ensure that the PMOS and NMOS transistor that is connected to the clock, that transistors of PMOS and NMOS that is connected to the clock will turn on those 2-transistors and that is possible in an opaque mode, especially if I design this latch with a clock level high. This high level clock is when the latch will be working in a transparent state that means, the output will follow the input, this particular low level of the clock is when we say that it is in opaque mode and output should retain whatever was the previous state.

In this design what we are saying is, this particular tri-state inverter with the clock should ensure that the, we supply the clock of the low level signal. A low level clock should be supplied such that the transistor will be on and an output here will be nothing but the inverted output of the input. That is the reason why for the tri-state inverter here, the inverted of the clock that is been supplied for the latch signal. For the latch signal I have a clock of ϕ that means, that the high level it should pass the signal.

The tri state inverter is there here which ensures that the low level clock signal is supplied to the tri-state inverter. So, that we will have the complement of this particular input at the output side during the low level of the clock and that is why a complement of the clock signal is provided to this particular tri-state inverter.

If you notice the tri state inverter, we had the input like this and output like this and then we had a NMOS and PMOS as $\overline{\phi}$, what it means is the NMOS side we are giving a clocks, we are giving a signal of ϕ and then on the PMOS side it is the signal of $\overline{\phi}$. But for our design of the CMOS latch and especially to staticize, especially to avoid that dynamic or the floating node voltage at the X node, what we are doing is we are providing the clock signal on the NMOS side, it should be $\overline{\phi}$ and on the PMOS side it should be the complement of $\overline{\phi}$ which will be nothing but ϕ. This is what the schematic looks like for the tri-state inverter. The tri-state inverter, this will be the $\overline{Q}$ signal and the clock is nothing but $\overline{\phi}$ given to the NMOS and then ϕ given to the PMOS and the output is nothing but the X node.

Now, what it does is based on the $\overline{Q}$ signal, if the $\overline{Q}$ is 0 here, the output of here it will be 1. Even if it wants to drop due to the sub threshold leakage current, this 0 will ensure that the V_{dd} is driving this particular X node or whatever is a capacitance at the X node.

Even if I will have some kind of a sub threshold leakage current in terms of nano amperes, the Vdd is going to provide pump in more current and it is going to stay at a logic level of 1. Similarly, if $\overline{Q}$ is actually 1 instead of 0. I will have an output of 0 and then this X node will be driven by the ground rail. The ground rail is this and then the V_{dd} rail is this, that is the advantage of having a feedback path, wherein a tri-state inverter is used in the feedback.

Thereby making the output node staticized or rather it is driven to either a logic 1 or 0 even if there is a drop or rather the sub threshold leakage current, it is likely to have its likely to discharge or charge this output node. But, because of this tri-state inverter the real voltages are going to dominate or drive this X node, it is no longer a dynamic or a floating node anymore.

This particular design technique helps to overcome the dynamic node voltage at the X node, the dynamic node voltage problem. Just to summarize when ϕ is equal to 1, we will have the transmission gate, which will be passing or which will be on and which will be passing the input to the X node and then to the $\overline{Q}$ output.

It works like a transparent mode or a transparent operation and the tri-state inverter will be off. During the transparent stage, the transmission gate is going to pass the signal. Whereas, the tri-state because the ϕ is equal to 1 that means, ϕ is equal to 1 means $\overline{\phi}$ is equal to 0, this NMOS and PMOS transistor will be off, the tri-state inverter will not be on, or it will be off.

The tri-state inverter is required only in the opaque state. When ϕ is equal to 0, that is when the opaque state starts and then the transmission gate, it will not pass, because this will be 0. We will have the tri-state inverter passing the signal of the previous output and with ensuring that the x is retained to the previous X value. The tri-state inverter will be on and $\overline{Q}$ is staticized.

This particular latch design at the input side there is no inverter. It is still sensitive to the input noise and the one more disadvantage is which this particular feedback path will bring

in is it reintroduces. This is the output node and any kind of coupling, noise coupled to the output node is kind of reintroduced back to the X node especially, when this tri-state inverter is on that is when the opaque operation of the latch is on, it reintroduces the noise from the output to the X node.

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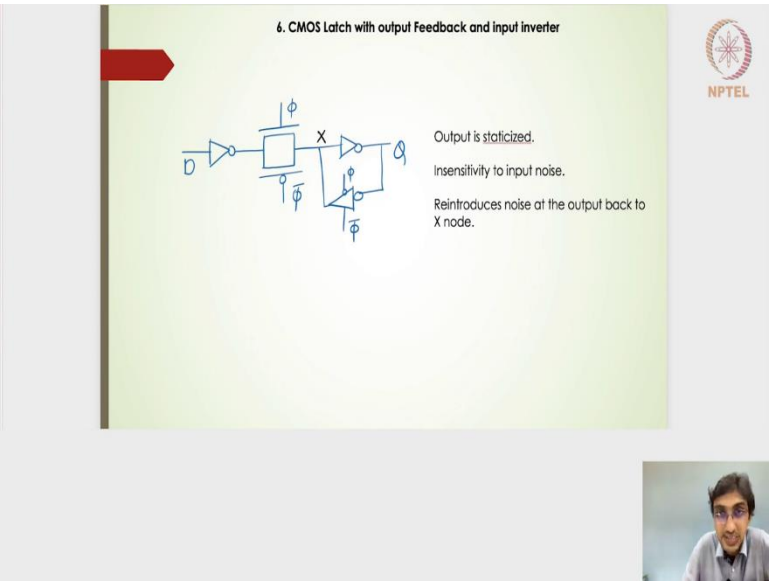

That is the one disadvantages this particular design brings in, CMOS latch with the output feedback and the input inverter, that if I bring in an inverter at the input side, then it becomes insensitive to the input noise.

The output is staticized because of the feedback tri-state inverter. Insensitive to the input noise because of this particular inverter, but it reintroduces the noise which is coupled at the output node, back to the X node especially when the tri-state inverter is on during the opaque node, during the clock level going low.

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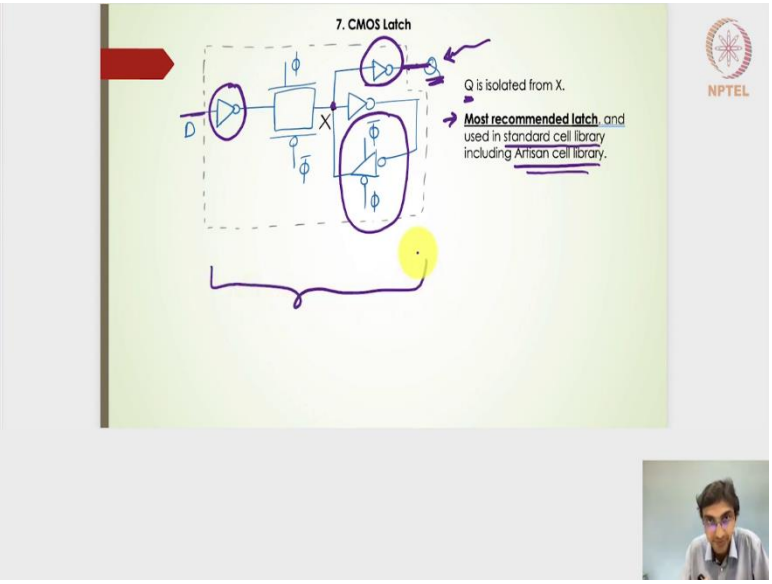

What to do that, here is the design. There is an inverter here, there is an inverter here, there is a tri-state inverter in the feedback path and then there is one more inverter here, which says that this is the output node and everything else apart from the output and then the input everything else is encapsulated or insulated completely.

Even if the Q is getting isolated from the X node. Even if there is an a noise at the Q point, because it is freely available to the outside chip design, even if there is a noise signal that is gets coupled into this particular node, it does not get reintroduced into the X node because of this particular inverter.

The input noise does not get coupled because of this particular inverter and because of this feedback path the tri-state inverter, during the opaque state or during the clocks level low, this X node is maintaining the previous X value. This particular design is considered to be the most recommended latch design, especially it is used in a standard cell library including the artisan cell library. This is the most standard cell library one can see for a latch design. Once you go into any kind of a design suite and if you want to pick a latch design, most often you will come across this particular latch design.