Design and Analysis of VLSI Subsystems
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Lecture - 70
Subthreshold leakage current and Gate leakage current

Hello students welcome to this lecture on the static power and in this particular lecture we will continue with the Subthreshold leakage current and also subsequently see or look into the Gate leakage current and then try to analyze the subthreshold leakage power and then the gate leakage power or the currents for a given circuit. Let me pick up my pointer and proceed further to the next slide.

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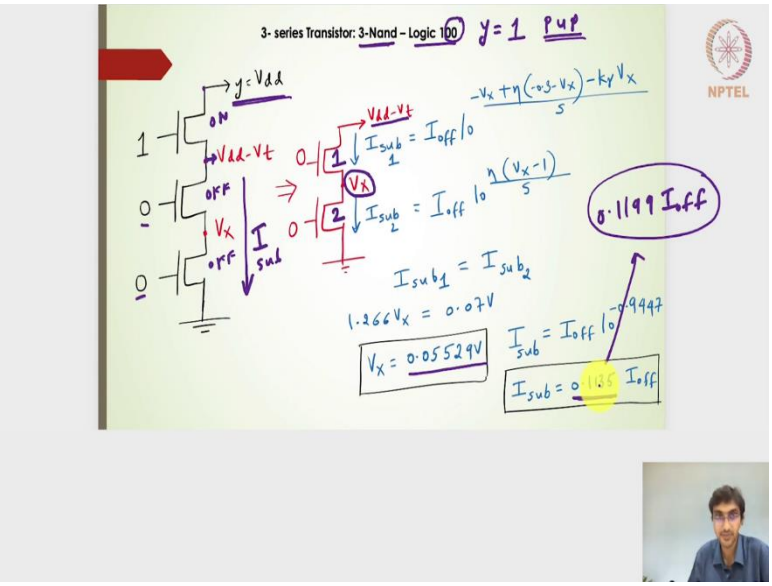

We were looking into the 3-series or transistors especially for the 3 input NAND gates and we were looking into the logic of 1 0 0 in the previous lecture. Remember that for a 3 input NAND gate the logic of 1 0 0 will yield an output logic of 1 here. That means, that the pull up circuit is likely to make sure that the output voltage is retained at V_{dd} because the pull up side we will have the two of the transistors where the input is 0 0 is going to make the transistors PMOS transistors both the PMOS transistors to be ON. The PMOS transistors are going to drive the current to ensure that the output voltage is starts to V_{dd} value.

Now, we are interested in finding out the static power or the subthreshold leakage power in this particular case. We know that when the transistors are getting an input of 0 0

especially for the NMOS transistor. We know that these two transistors will be OFF and the transistor with the logic of 1 this will be ON and if I consider this particular transistor. The ON transistor to be working as a pass transistor ON one side of the diffusions or one side or rather the drain terminal here is connected to the all is being charged to V_{dd} rail. Then the other side it can charge or it can drive till $V_{dd} - V_t$. If I have this particular node voltage as $V_{dd} - V_t$ and these two are OFF transistors ON the other side it is connected to the ground then I should be able to estimate or evaluate the subthreshold leakage current.

Then that is what we had done $V_{dd} - V_t$ and then ground the subthreshold leakage current of 1. Using that particular, the approximate equation of the subthreshold leakage current, we estimated or we arrived at the expression of subthreshold leakage current for the transistor number 1 and then the subthreshold leakage current for the transistor number 2. Equate both this subthreshold leakage currents we should be able to find out V_x value which was 0.05529 volts. Then find out the subthreshold leakage current turned out to be $0.1135I_{off}$ current, which is actually and if I compare that with $0.1199I_{off}$ which is for the two stacked transistors with on one side it is V_{dd} and the other side it is ground. This particular value is higher than this particular 0.1135. Intuitively we can say that is correct because this $V_{dd} - V_t$ which is a slight drop and the voltage as compared to the V_{dd} value.

If I have it three transistors stack transistors with one of them being ON, the two of them will give me the OFF transistor are likely to give the subthreshold leakage current, but this current will be $0.1135I_{off}$ current, hope this is clear.

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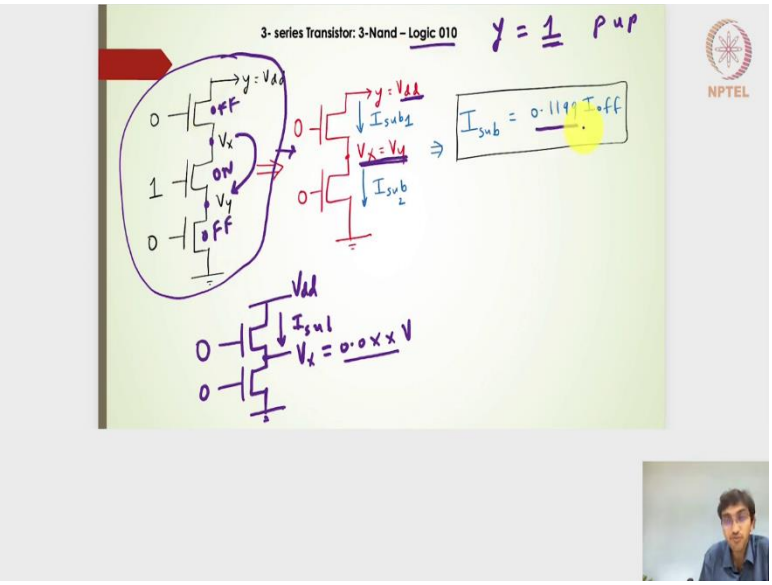

Now, let us say that if I have a logic of 010. If I have a logic of 0 1 and 0. This is OFF transistor of course the 010 will give me the output of the 3 input NAND gate to be nothing but 1. That means, that the pull up side it is active and it is driving the output node to value of V_{dd}.

In this 010 this both these transistors are OFF and then this particular transistor where the 1 is given or logic level high is provided to the gate of the second transistor that particular transistor will be ON. If I have that ON transistors and normally when we see the two stack transistors or the three stack transistors where the first transistor is OFF.

If I consider this particular transistor where both the transistors are OFF one has noticed that this particular node voltage. If this is an OFF transistor I will have the subthreshold leakage current. The subthreshold leakage current is low that it is in terms of the nano amperes for a 65nm technology node. This particular node voltages turns out to be very very low.

It is actually somewhere around 0.0 or 0 some value 6 5 value or 5 volts or something like that. The 0.05 or 0.06 volts in that sense this particular if I have an OFF transistor here this V_X value is going to be very really really low value and if I have a low value here the V_X value and this is an ON transistor.

It can work like a pass transistor and it can pass whatever is there on the other side. Even though I have written V_X and V_y as two different variables it turns out that because it is a OFF transistor here V_X value will be very very low. A low value here is going to reflect on the V_y value, we will have this V_x is equal to V_y. If I consider these two node voltages as the same then I can actually have these two transistors and this the three stack transistors in which one the middle transistor is ON I can actually make it an equivalent of two transistors taking out the ON transistors. Then having this node voltage of V_x equated to V_y and these two transistors will be stacked these 2 OFF. Now I think I should be able to find out the subthreshold leakage current quite easily.

I have the subthreshold leakage current of 1, I have the sub threshold leakage of 2 and then the ON one side it is V_{dd} the other side it is ground.

$$I_{sub} = 0.1199I_{off}$$

This is something which we are already seen earlier. For a logic of 010 I will have a subthreshold leakage current of $0.1199I_{off}$ current moving ahead.

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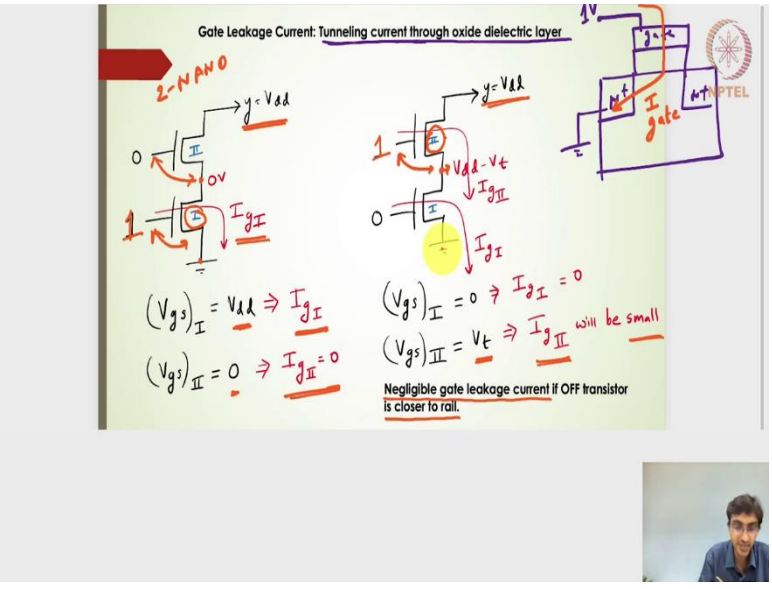

Now let us take a look at the gate leakage component. The gate leakage component is there for especially for an ON transistor. Now remember that the subthreshold leakage current we actually evaluate for a transistor where the V_{gs} value is less than or equal to 0.3 volts or the V_t value.

Generally, we take into account the V_{gs} value is actually less than 0.3 volts for the subthreshold leakage current and then subsequently the subs threshold leakage power estimation. For the gate leakage current and then estimating the gate leakage power, we need to ensure that the ON transistor is going to is likely to give us the gate leakage current. The gate leakage current is actually attributed to the tunneling effect the tunneling current through the oxide dielectric layer. Let me draw at cross section diagram of the NMOS transistor quickly, this is my N^+ diffusion pocket and this is the oxide and then this is the gate. What is likely to happen is based on the voltage applied here. If it is a 1 volts logic for a 65nm technology node and let us say the source is grounded, I will actually get a current that will be flowing or tunneling from the gate to the source side.

I will have a current and this particular current is called as the gate current. When I consider this particular circuit of two stack transistor with y is equal to V_{dd} this could be a part of a 2 input NAND gate where we have 0 and 1 as an input. My output will be nothing but 1 for a 2 input NAND gate. It will be active or driven by the pull up side. The pull up side is going to make sure that the output would no node voltage is set or configured at V_{dd}. In this case I have a 0 and 1. I will have some kind of a subthreshold leakage current, but more importantly when I am looking into the gate leakage current. This 1 is likely to give me a gate leakage current or a tunneling current across this oxide.

That is referred to as I current gate for the first transistor, this is the first transistor. For the second transistor this is an ON transistor, whatever is 0 here it is kind of passed into the other side of 0 volts. This V_{gs} turns out to be 0 that means, basically this is not likely to provide any gate leakage current. That is what I have written or indicated here V_{gs} of the first transistor is actually 1 volts or V_{dd} value. It is likely to give me a gate leakage current. That is represented by I_{gI} transistor V_{gs} of the second transistor is going to be 0. In fact, if it is actually less value it may be it is 0 or a V_t value, this is going to give me a very very low gate leakage current. If it is close to V_{dd} value I will get a gate leakage current. What it really means is to just to summarize the gate leakage current which will help in evaluating the gate leakage current and then subsequently the gate leakage power is we need to identify in a circuit which of the transistors are ON and then from then we should be able to find out the gate leakage current.

If I have another configuration here of the transistor here which is on and the transistor on the down transistor which is closer to the ground rail it is OFF and this is provided with a 0 logic and this is 1. This 0 is going to anyways an OFF transistor. There will would not be any gate leakage current, but having a 1 logic here although the transistor is on what happens is because on the other side it is V_{dd}. It is going to act like a pass transistor and in this particular node we will have $V_{dd} - V_t$. The V_{gs} for the transistor number 2 is going to be $V_{dd} - (V_{dd} - V_t)$ which is actually turning out to be V_t value.

If V_t value is actually closer to the 0 volt, the gate leakage current will be actually be very very small and we tend to ignore that. What we are saying is the negligible gate leakage current is evaluated, if the OFF transistor is closer to the rail. In this case I had a V_{gs} value of V_{dd}. I got the gate leakage current, but if we swap the logics here 0 1 onto the 0 to the transistor which is closer to the rail and 1 to the transistor which is closer to the output node.

Then I will have the V_{gs} value to be very very small and that will have a very reduced value of the gate leakage current. This particular configuration is better in terms of the gate leakage current just to minimize the gate leakage currents and overall minimize the gate leakage power, hope this is clear moving ahead.

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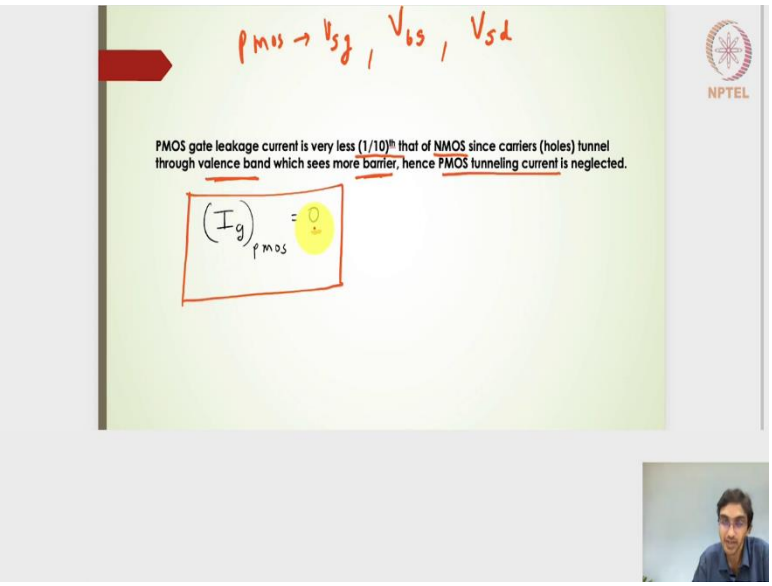

We have seen the subthreshold leakage current for the NMOS transistor we had seen the subthreshold the gate leakage current for the NMOS transistor. The sub threshold leakage

current for the PMOS transistor is also very very similar just that we will have to write those voltage in terms of V_{sg} for the PMOS transistor and we have to write the source to body we will be nothing but body to source.

We have to write V_{sd} instead of V_{ds} and our expression will remain the same. For the PMOS the gate leakage current of the PMOS it turns out to be very very less turns out to be 1 by 10th that of the NMOS transistors with the similar V_{gs} effect, if the V_{gs} for the NMOS transistor is 1 and if I have the V_{sd} for the PMOS transistor to be 1.

I will still get the gate leakage current to be 1 by 10th that of the NMOS the gate leakage current. The reason is actually very simple because for the NMOS while we get the tunneling current the majority carriers in the NMOS which is nothing but the electrons which actually tunnel from the body or the source side to that of the gate side. That kind of tunneling or on the flow of the majority carriers on the NMOS side is much easier as compared to that of the PMOS. Where the holes are the majority carriers that is lying in the channel or that is lying close to the source side and that has to tunnel to that OFF to the gate side and that sees a lot more barrier.

In that sense the PMOS the tunneling current is turns out to be very very low for the same amount of the V_{gs} value for the same magnitude of the voltage values. In that sense what we are going to do is just for our own analysis this current is turning out to be very very low, we will direct it to a value of 0. From here on while we are looking at the circuit it may be a NOR gate or a NAND gate or any other combinatorial circuits, the PMOS gate current we will approximate it to be 0 and we will try to evaluate the subthreshold leakage current for the PMOS.

We will also evaluate the subthreshold leakage current of an NMOS and then the gate leakage current of an NMOS. Finally, we will sum up all the leakage currents and including the gate leakage current and the subthreshold leakage currents and then try to evaluate or analyze what is the leakage power also referred as the static power, hope this is clear.

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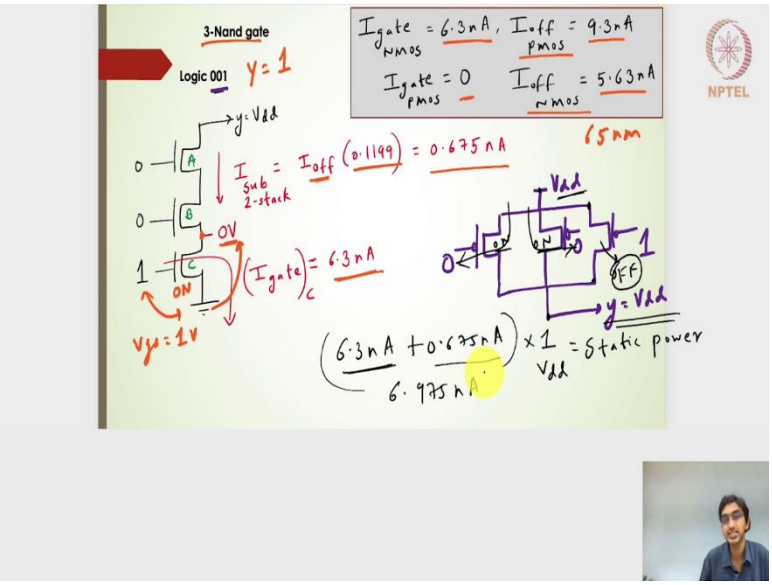

Let us take a look at the 3 input NAND gate which we have anyways taken and look at it, but with some values now. If suppose I have a logic of 001 that means, that the output is actually nothing but 1. That means, that the output is driven by the V_{dd} by the pull up side of the 3 input NAND gate, which is nothing but consists of three of the PMOS transistors in parallel. The values given here is the gate leakage current for an NMOS is 6.3nA the gate leakage current of the PMOS is 0 and these are the typical values for a 65nm technology node. The I_{off} current of the PMOS transistor that means, when the PMOS transistor is OFF, I will get a current of 9.3nA and if the NMOS transistor is OFF I will get a current of 5.63nA.

Remember that the I_{off} current the subthreshold leakage current of an NMOS is turning up is actually less than that of the I_{off} of the PMOS transistors. What it really means is if I apply the same magnitude of the voltages the PMOS is likely to give me slightly more subthreshold leakage current than that of the NMOS transistors. Looking at this particular pull down side because the pull up is going to be it is going to be active. The pull down side is where we will get the leakage current and if it is a logic of 001 that means, 0 0 and then 1. The 1 on the transistor which has a 1 which is on it is actually closer to the ground rail. This acts like a pass transistor and then provides this on the other terminal it is going to pass a 0 voltage.

My subthreshold leakage current because of these two stack transistors ON one side it is V_{dd} on the other side it is 0 volt. It will have $0.1199I_{off}$ current. The I_{off} current of the NMOS side is 5.63, it will be nothing but 0.675nA and if this we calculated for the subthreshold leakage current, we need to evaluate for the gate leakage current.

The gate leakage current if I consider you know the we need to identify the ON transistor and only this transistor is ON, where we get this V_{gs} value to be nothing but 1 volts. It is not close to V_t or close to 0. I will have some gate leakage current which is nothing but the 6.3nA which is given in this particular data sheet. This becomes the subthreshold and then the leakage current for the 001 logic. Now, if I look into the pull up side of this particular 3 input NAND gate I will have three of the parallel PMOS transistors. Let me draw that as well and see whether there are any kind of a leakage currents, on one side it is V_{dd} and on the other side also it is actually V_{dd} because this is a PMOS and or the pull up side and the logic here that has been imparted or given to the transistor is 001.

That means, this particular transistor is OFF on the pull up side that is on the PMOS side whereas, these two transistors are ON. It ensures that this is the output is charged to V_{dd}, there would not be any leakage currents here because this is anyways a non transistor there should be a subthreshold leakage current here. But if you look into the V_{ds} value turns out to be the same.

Whenever we have the same drain to source potentials to be the same there would not be any current. In fact, there would not be any subthreshold current, as well because on both the sides of this transistors we have the current of V_{dd}. There should be some kind of a potential difference then only we will have some kind of a subthreshold leakage current. But here because both the terminals of this transistor which is an OFF transistor sees the same potential. We will not have any subthreshold leakage current this particular ON transistor is like is was supposed to give us the gate leakage current, but because we know that the PMOS transistor is likely to give a very reduced gate leakage current.

Although it is a 0 what we are going to say is that the current here and then the current here that is tunneling to the gate side is going to be very very low. In fact, the gate leakage current of the PMOS side is going to be 0 and then 0 the subthreshold leakage current on the PMOS side is going to be 0.

The total leakage current for this particular logic of 001 turns out to be 6.3nA + 0.675nA and if I actually do a multiplication by 1 which is nothing but the V_{dd} value I should be able to find out the static power for this particular logic, because the $1V_{dd}$ value is there between the rail voltages of V_{dd} and then that of the ground.

It is likely to have a current consumption of 6.3 + 0.6795 = 6.975nA and if I have to multiply by and if I want to estimate the power it has to be multiplied by the real voltage which is configured to the V_{dd} value of 1 volts, hope this is clear moving ahead.

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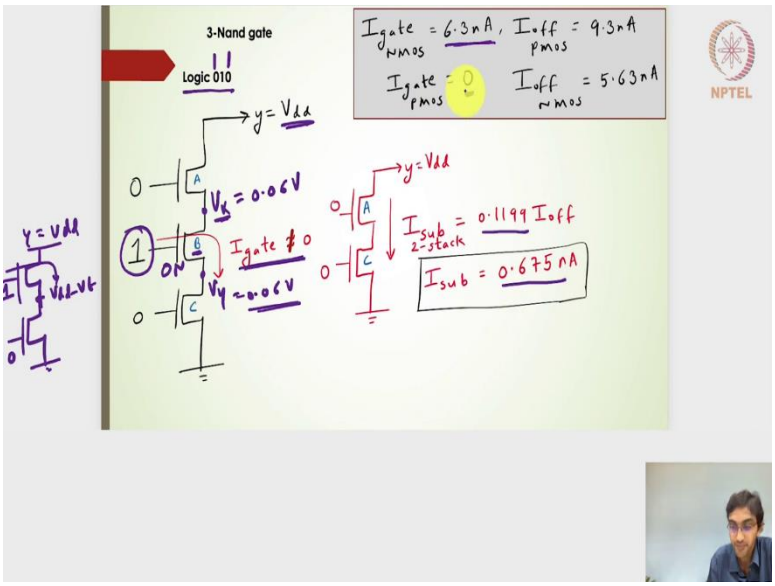

Let us say the logic is 010. For a logic of 010 and this is something we had already seen the previous lecture. For a logic of 010 here we know if I want to understand or estimate the subthreshold leakage current this value is going to be very very low and I can say that V_X and V_y were going to be same and one side it sees V_{dd} and the other side it is ground.

I can actually have two stacked transistors ON one side with V_{dd} the other side has V_y, because B transistor which is on is going to act like a pass transistor and make this V_x is equal to V_y. The subthreshold for the two-stack transistor will be $0.1199I_{off}$ current turns out to be 0.675nA. Now, if I want to find out the gate leakage current is applicable only for an ON transistor. Only the B transistor is ON here, I will have this transistor as an ON transistor. I should have a gate leakage current the value of V_X here and then the V_y here, I

should be able to find out from the subthreshold leakage current turns out to be very very low value 0.06 or 07 values.

In this case I will have the V_{gs} value to be almost close to the one value. I will get the gate leakage current not equal to 0. If you remember I have when we started with the gate leakage current if it was connected to V_{dd} right or rather it was connected to an output node which was at V_{dd} and then 2 of the stacked transistor where I had 1 this 1 and then 0 this 1. This one ON transistor is going to act like a pass transistor and then going to supply $V_{dd} - V_t$ and then we said that this the gate leakage current here will be very very low, because the voltage here V_{gs} value turned out to be closer to 0 because it is nothing but 1-$V_{dd} - V_t$ which will be nothing but V_t. My gate leakage current turned out to be 0, but in this particular case because of this OFF transistor I will have a V_x value which is not $V_{dd} - V_t$. In fact, this V_y value is not $V_{dd} - V_t$ it will be very very close to 0 volts. That is the reason why I will have a gate current and it will not be equal to 0. In fact, the gate current will be close to the gate NMOS side will be close to 6.3nA. On the pull up side we will have a similar effect as out of the logic in as out of the previous logic.

We will not have the subthreshold leakage current on the pull up side and the gate leakage current although there are two transistors which are ON. But still we will ignore it saying that the gate leakage of the PMOS is very very reduced value close to the 0 and then we will not take that into account Hope this is clear moving ahead.

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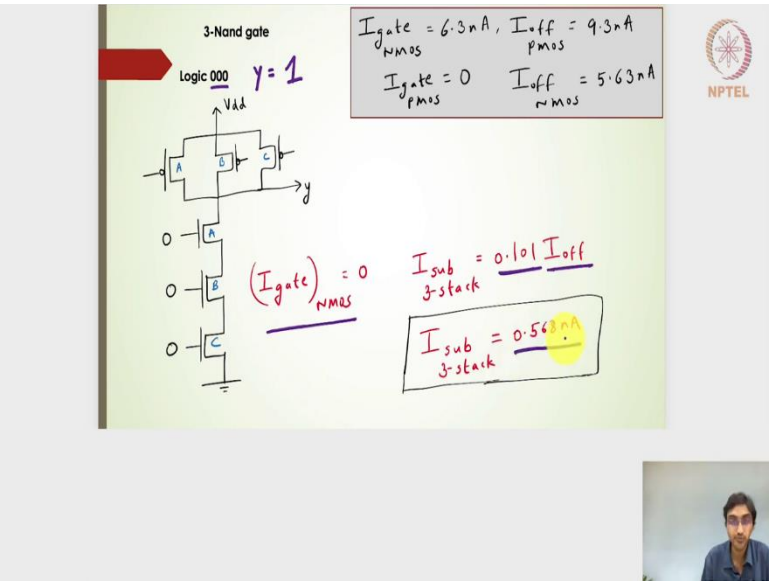

If my logic is 000 we know that the output in this particular case will be 1 that means, all the three transistors are ON. There would not be any subthreshold leakage current from the pull up side, there will be the three gate leakage current. But we know that the gate leakages of the PMOS transistors are very very negligible and then that we are going to ignore that.

For the 000 all the three transistors are OFF, the subthreshold leakage current will be nothing but $0.101I_{off}$ current as we have seen in the previous lecture, gate leakage current because although all the transistors are OFF. We will not have any gate leakage current. The subthreshold 3-stack current will be the total leakage current coming for this particular logic, it turns out to be 0.568nA moving ahead.

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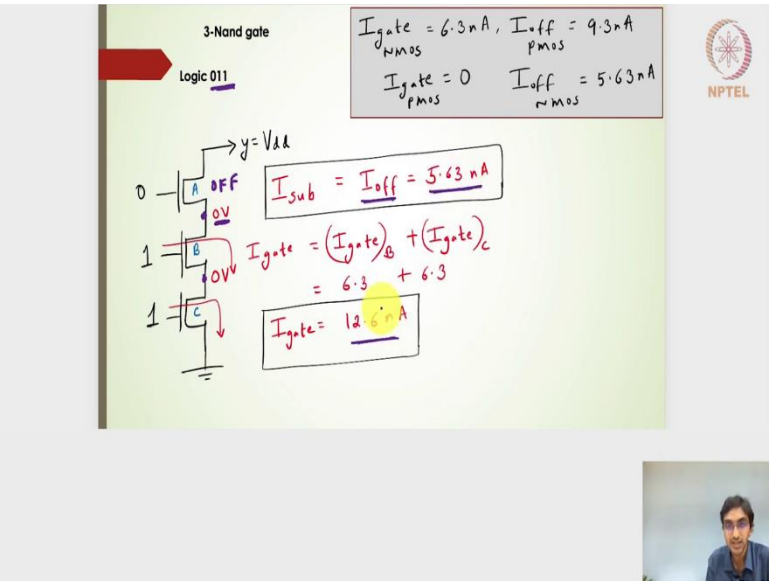

If the logic is 011. I have 1 and 1 here and then 0 here. I can consider these two ON transistors to work like a pass transistor. The potential of 0 can be passed here the potential of 0 can be passed here. I will have a gate leakage current coming from this ON transistor gate leakage current coming from this ON transistor.

The total gate leakage current is actually nothing but the twice that of the gate leakage current or for an NMOS transistor. The gate leakage current will be for the transistor B and C, 6.3 + 6.3 = 12.6nA, will be the total gate leakage current for this particular 3 input NAND gate for a logic of 011.

Well if I want to find out the subthreshold leakage current we know that only one transistor is OFF here, the other two are ON. We will have the 0 volts here on one side the other side it is V_{dd}. I will have an V_{off} current for this particular A transistor which is nothing but 5.63nA. The total leakage current will be 5.63 + 12.6nA x 1V will give us the static power moving ahead.

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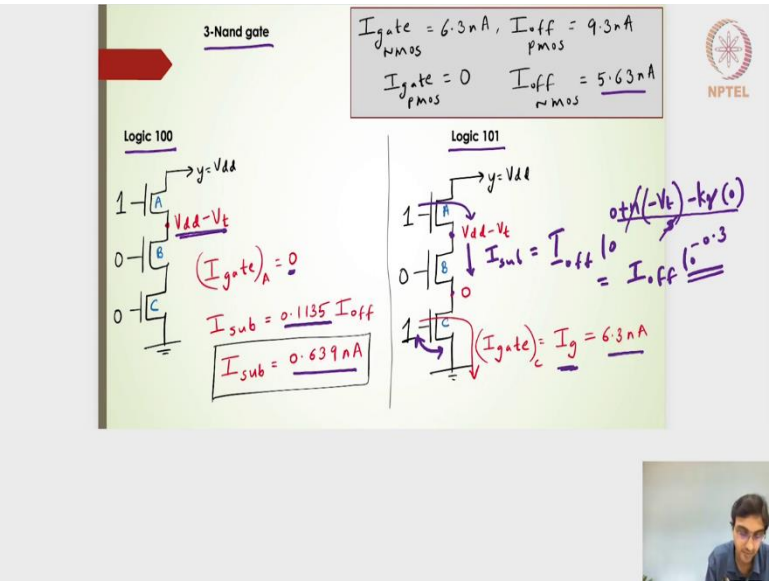

The 3 input NAND gate let us see for a logic of 1 0 0 and logic of 1 0 1. For a 1 0 0 if I have 1 and 0 0 these two will be OFF transistor this will be an ON transistor. I will have this transistor working like a pass transistor. I will get the voltage of $V_{dd} - V_t$ here. This two of transistor likely to give me the subthreshold leakage current this ON transistor will have a gate leakage current, but because this V_{gs} value turns out to be close to V_t, I will have the gate leakage current negligible or very low value and then I can equate it to 0.

The subthreshold leakage current we know that for a $V_{dd} - V_t$ and then the ground if there are two stack transistor it turns out to be 1 1 a $0.1135I_{off}$ current. Turns out to be I_{off} current is nothing but for an NMOS is 5.63, it will be 0.639nA. For logic of 1 0 1 here these two transistors will be ON, on one side it is working like a pass transistor, the ground of 0 will be passed or a 0 logic will be passed here. On this particular transistor which is also an ON transistor. It sees y is equal to V_{dd}. It will pass $V_{dd} - V_t$ the NMOS transistor, this OFF transistor is going to give me the subthreshold leakage current. The subthreshold leakage current will be nothing but the I_{off} and 10 raised to V_{gs}, V_{gs} in this particular case it is 0 +

η, V_{ds} is nothing but $V_{ds} - V_{dd}$. I will have $-V_t$ and -k_γ and then V_{sb}, V_{sb} is nothing but 0 divided by the slope of S. The S is 0.1 and η is 0.1, I can cancel that. It is nothing but I_{off} x $10^{-0.3}$. This turns out to be nothing but 0.5 value of the 5.63nA.

The gate leakage current because this is $V_{dd} - V_t$, I will have a negligible gate leakage current here from this particular transistor, the gate leakage current is 0 this is anyways an OFF transistor. I will have no gate leakage current. I will have a gate leakage current coming from here because the V_{gs} value here is actually 1 volt. I will have a gate leakage current of the one single NMOS transistor which is 6.3nA.

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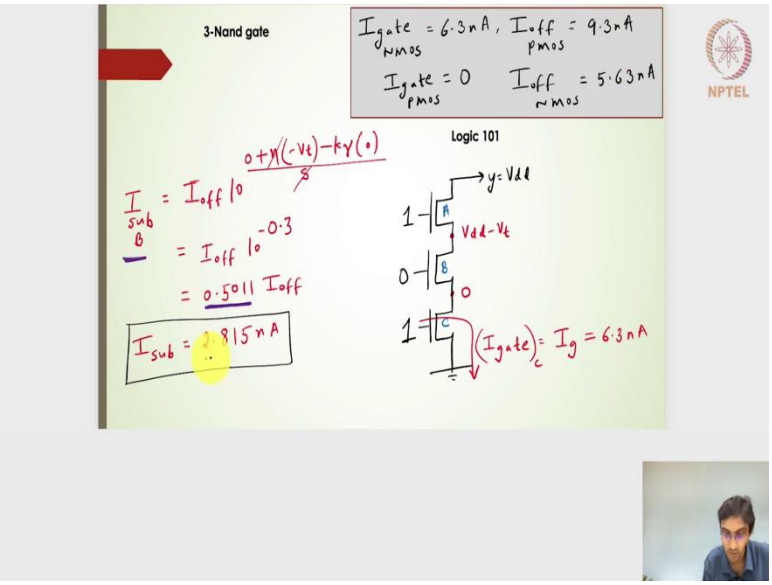

Moving ahead, this is what we had seen actually for the logic of 101. The I_{sub} for the leakage current is what is stated here $10^{-0.3}$, 0.5011I_{off} and I_{off} is 5.63, it will be 2.815nA.