Design and Analysis of VLSI Subsystems
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Lecture - 65
Energy estimation through driving factor

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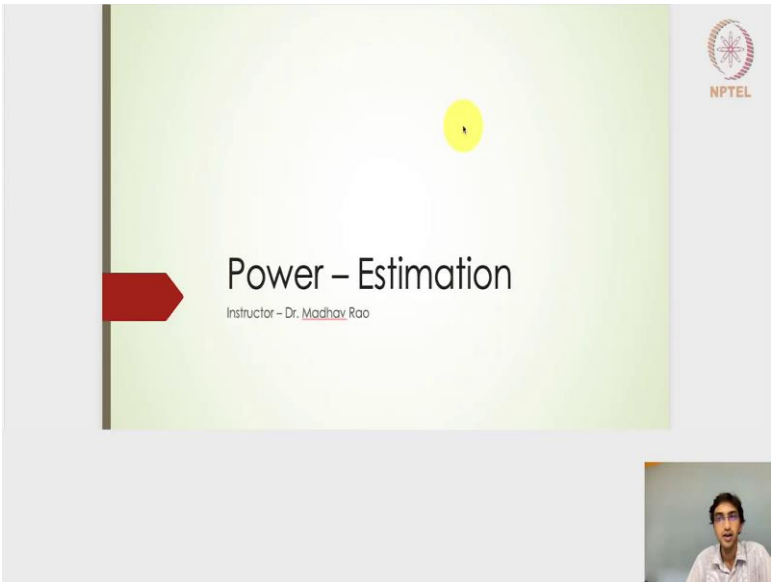

Hello students. Welcome to this lecture on the Power Estimation. Although it is a module is on power and I have written it as an estimation subsection for this particular module. It is basically trying to estimate the power using a driving factor expression.

What we will do is in the initial part of this lecture? We will quickly go to the definition of the driving factor or try to understand the driving factor first and then try to realize that or use the driving factor in our circuit design to estimate the overall power. Let us move on to the next slide.

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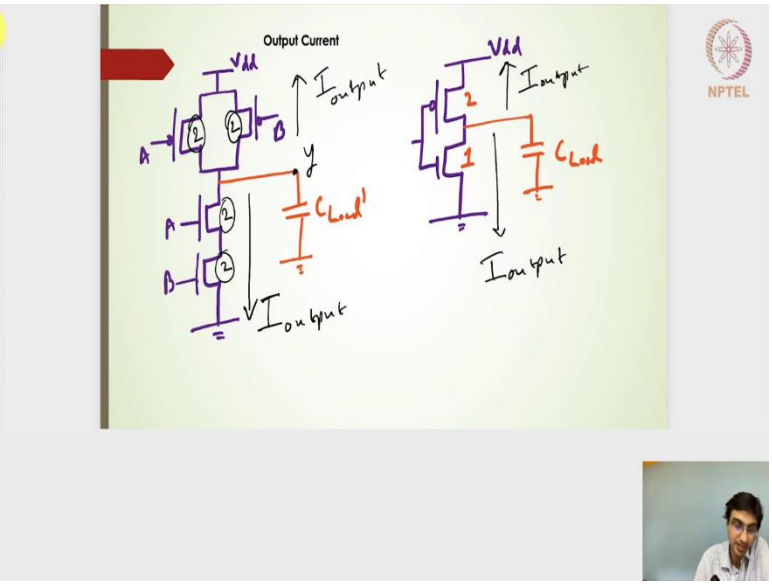

This is an empty slide which says the output current. What I want to do is just want to summarize how do we define the driving factor. Let me go back and then draw the two input NAND gate. I have a two input NAND gate, I have a PMOS transistor in parallel two of the PMOS transistors in parallel and we will have the V_{dd} rail and then we have the two of the NMOS transistors in series.

Here is my input A, B and let me also draw the inverter here as 2:1 benchmark inverter. I will have a PMOS transistor and then connect it to an NMOS one and then I will write the sizes here has 2:1 and then that I will also have a C_{load} capacitance here and then I will also have a C_{load} capacitances here.

In this particular case, if I have whatever the C_{load} capacitance could be different. I will have it as a C_{load} dash here. The capacitances are difference, but the way that we size this particular transistors is like 2:1, we wanted the size to be nothing but 2 and 2 here and then 2 and 2 here. While it is falling down the falling resistance should be equal to that of the falling resistance of the 2:1 inverter.

What it really implies is the current that is while the output node is doing the switching from 1 to 0, the output current here should be same as that of the output current of the 2:1 inverter, while it is falling down and similarly we have sized it 2 and 2 here. In the worst case condition if one of the transistor is on, the rising current of the output should be similar to that of the rising current of the 2:1 inverter.

What we have done previously size this up accordingly 2 and 2 and then 2 and 2 here. So, that we will get the output current of the capacitor being charged or discharged, that is output current equal to that of the output current of that 2:1 inverter.

With this particular understanding of the sizing of the gates especially for the two input NAND gate and the two input NOR gate, let us try to redefine the driving factor another parameter or another factor which we can define the gate sizes, through which we can actually define the gate sizes.

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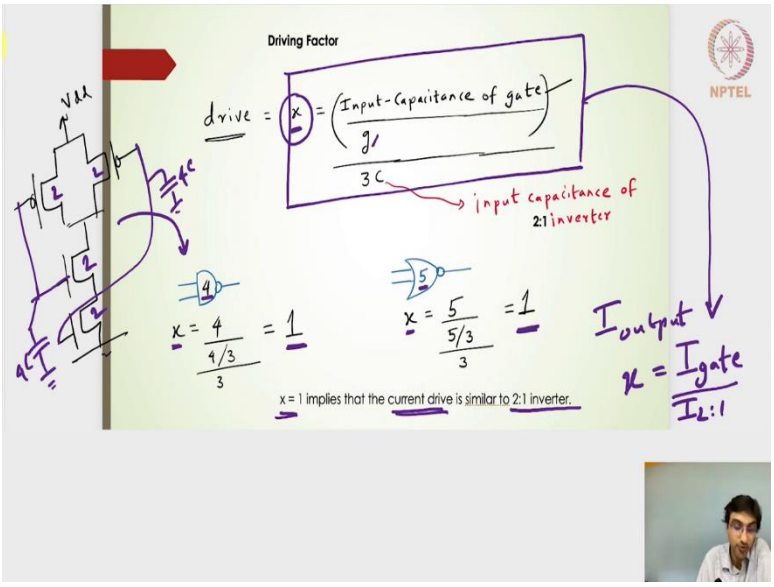

Here is a definition the driving factor - the driving factor here is defined as,

$$\text{drive} = x = \frac{\dfrac{\text{Input capacitance of gate}}{g}}{3C}$$

It is the basically the ratio of the input capacitance of the gate whatever we have and then the input capacitance of the 2:1 inverter and also in the denominator we have the logical effort of this particular gate.

Remember that in our previous slide we had the two input NAND gate to be of size 2:2 the NMOS transistor was of the size 2, the PMOS transistor was of the size 2. So, that we will get the outward current similar to the current I as similar as that of the 2:1 inverter.

Now, this is what the definition I have here. Let us say if I have the two input NAND gate. I am drawing the two input NAND gate, two of the PMOS transistors in parallel and two of the transistors in series. Let us say that the size is 2 and 2 and then 2 and 2. That means, that this particular gate is of having an input capacitance of 4. That is what we know the gate with the size of 4 indicates that in the individual input to this particular gate sees a capacitance of 4C.

In this particular case the input capacitance here which is connected to this sees a capacitance of 4C. This is what we have already learnt and this is by definition we write it as the gate size as four indicates the input capacitance to this particular gate, whatever the number of the inputs that we give each in input sees a gate capacitance of 4C.

As per the driving factory definition, if I have this particular two input NAND gate of size 4, I know that the gate capacitance will be 4C. It will be,

$$x = \frac{\frac{4}{4/3}}{3} = 1$$

Similarly, if I have a two input NOR gate, if the gate size is 5 that means, that each of the input sees a capacitance of 5C.

$$x = \frac{\frac{5}{5/3}}{3} = 1$$

In the previous slide we had seen the output current. The output current of the two input NAND gate should be equal to that of the output current of the inverter. The current drive in this case is very similar or actually same as that of the 2:1 inverter, that is why we will get the value x as 1.

In fact, if I try to find out what we are trying to see is the x value which is nothing but the output current of this particular gate divided by the output current of the 2:1 inverter. At this particular definition of the driving factor is actually rendering this the gate output current whatever gate we have two input NAND gate or a four input NAND gate or a whatever combinatorial circuit gates, its output current divided by the benchmark inverter 2:1 inverters output current that is what defines that driving factor.

But because of all this characteristic parameter like the logical efforts and we are known to design our gates or characterize our gates, with this the input gate the gate sizes has nothing but the input capacitances. We consider these input capacitances, we consider the logical efforts and then define our driving factor.

But driving factor actually implies it is nothing but how much time the gate current is actually more than that of the benchmark inverters 2:1 inverters output current. If I have a size of 4 here, what it implies is actually the output current size of 4 here the x driving factor turns out to be 1 for a two input NAND gate which implies that the output current of this particular two input NAND gate is very very similar to that of the 2:1 inverter.

Similarly, if I have a size of 5, the driving factor turns out to be 1 which means that the output current of the two input nor gate is similar to that of the 2:1 inverter. Hope this particular definition is clear to everyone.

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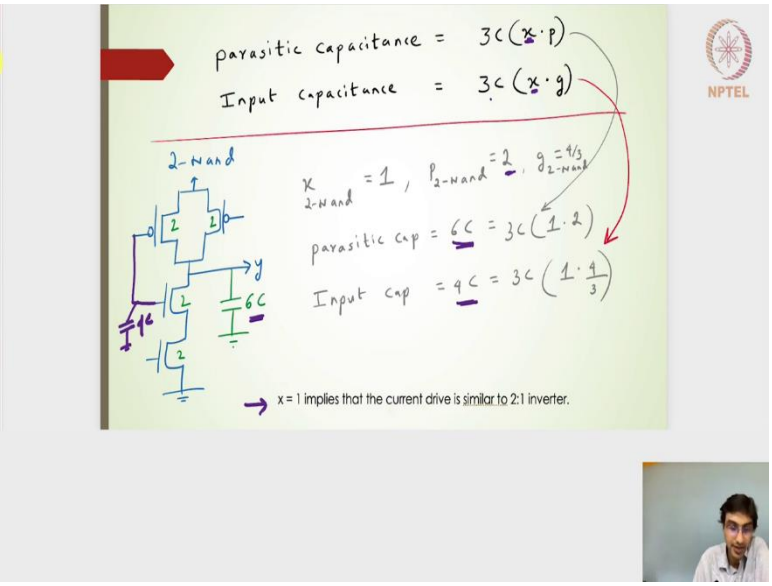

Moving ahead, if I know the parasitic or rather if I know the driving factor here, can I now establish what is the overall input capacitance and then the parasitic capacitance? if I know the driving factor and if I multiply that with the normalized parasitic factor and if I multiply with that of the logical effort and then multiply with the 3C, then I should be able to establish the parasitic capacitance and then the input capacitance subsequently.

$$\text{Parasitic Capacitance} = 3C(x.\,p)$$

$$\text{Input Capacitance} = 3C\ (x.g)$$

Now, to understand this lets take an example and then try to understand. Let us take a two input NAND gate which we had seen from the start of this particular lecture the size of 2 and 2, the size of 2 and 2 in the NMOS and in the PMOS side. The output parasitic capacitance of 6C here because this 2 this 2 and this 2 will contribute to have a capacitance of 6C.

The driving factor of this two input NAND gate is nothing but one here the parasitic factor for a two input NAND gate is nothing but two here. I have the normalized parasitic of a two input NAND gate is nothing but $\frac{6}{3} = 2$, the logical effort of the two input NAND gate is $\frac{4}{3}$.

With this particular x values and then g values and then the p values, can I now try to validate what is the overall parasitic capacitance and then the input capacitance? The overall parasitic capacitance is nothing but,

$$\text{Parasitic Cap} = 3C\ (1.2) = 6C$$

So, it does validate the parasitic capacitance.

$$\text{Input Capacitance} = 3C\left(1.\frac{4}{3}\right) = 4C$$

If I consider these two inputs coming from the NMOS and PMOS, I will actually have the 4C capacitance. Again I have just reiterated here x = 1 implies that the output current of the two input NAND gate here is same as that of the 2:1 inverters output current.

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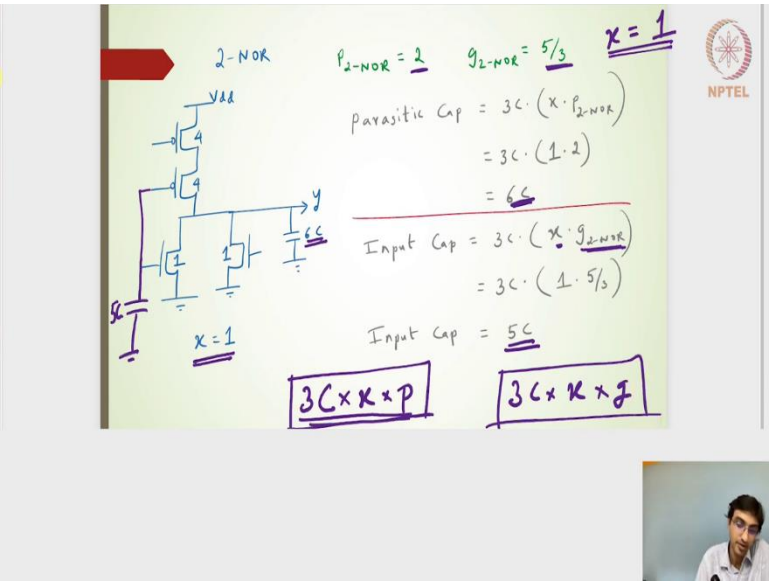

Moving ahead. Let us take another example of a two input NOR gate.

$$P_{2-NOR} = 2$$

$$g_{2-NOR} = \frac{5}{3}$$

Let us say that the x value is 1 here and the reason x value is 1 here because I know that the 4:1 size for a two input NOR gate or rather the gate size of 5 will actually give me the output current same as that of the output current will be 2:1 inverter. I will have the x value as nothing but 1.

If I consider this x value, g value and p value for a two input NOR gate, I should be able to find out or validate the parasitic capacitance which is nothing but,

$$\text{Parasitic Cap} = 3C\,(x\,.\,P_{2-NOR})$$

$$= 3C\,(1\,.\,2) = 6C$$

$$\text{Input Cap} = 3C\,(x\,.\,g_{2-NOR})$$

$$= 3C\left(1\,.\,\frac{5}{3}\right) = 5C$$

The overall it will give me the parasitic of 6C, and if I connect these two inputs I will actually get the input capacitance as 5C. That is also validated. So, 6C and then 5C capacitance is validated. Going forward what we can actually use is we can use this particular definition of 3C x X x P, if the gates are defined with the help of the driving factors multiplied by the parasitic of that particular gate should give me the parasitic of that particular gate.

Similarly 3C x X x g of that particular gate should be able to give me the input capacitance of that particular gate. Now, this capacitances becomes our absolute capacitance. Now, this absolute value of the capacitance is very useful, while we are estimating the energy or while we are estimating the power, the switching power or the dynamic power and similarly the switching energy or the energy delivered by the V_{dd} or the dynamic energy that is being delivered by the V_{dd}.

In that sense this particular driving factor or using the driving factor in our gate designs in our logical you know in a higher order digital logic circuit designs is very very useful.

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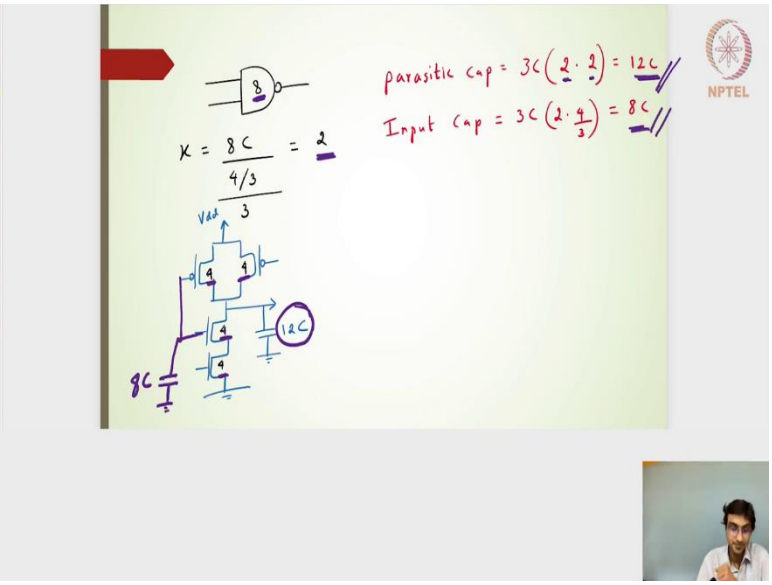

Just one more example. Let us say what happens if I have a size of 8 for a two input NAND gate. Remember that the size of 4, the 2:2 PMOS transistor 2 and NMOS transistor of the size of 2 will give me the output current similar to that of the 2:1 inverter.

My x factor or the x driving factor turns out to be 1, if I have a gate size of 4. Here the gate size is 8 that means,

$$x = \frac{\frac{8C}{4/3}}{3} = 2$$

Which means that I will have the size of 8 here will give me the output current to be twice higher than that of the 2:1 inverter. It is actually driving a stronger current and the reason is very simple, I will have eventually I will have the size of 8 will give me 4 and 4 here on the PMOS side and on the NMOS side will have 4 and 4. I will have a larger width here compared to my 2:2 two input NAND gate. That means, that the width is higher that means, the current is higher.

That is why I will have a driving factor of 2. The parasitic capacitance here just to validate it, it will be nothing but,

$$\text{Parasitic Cap} = 3C\ (2\ .\ 2) = 12C$$

$$\text{Input Cap} = 3C\left(2\ .\frac{4}{3}\right) = 8C$$

If I want to validate that in my gate size of 8, this is what 4 plus 4 plus 4 will give me 12C as a parasitic capacitance which is what validated here and the input capacitance of 8C, if I can actually connect this to inputs the gate size will be nothing but 4 and 4 or rather the transistor size is 4 and 4, will give me an input gate capacitance over all input gate capacitance as 8C.

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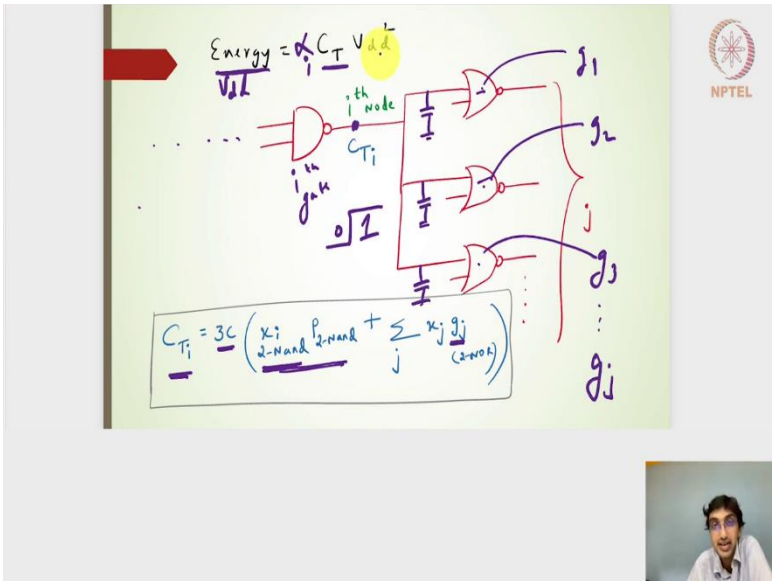

This is also validated, at this particular point of time what I had told earlier was, I can actually redefine my overall capacitance in terms of the driving factor. Actually redefine the capacitance in terms of the driving factor. The 3C multiplied by the driving factor multiplied by the parasitic will give me the parasitic capacitance and the input capacitance can be redefined as the driving factor multiplied by 3C multiplied by the logical efforts.

The energy at any point at any node in this particular at any node in a circuit. For example, if I have this particular circuit and if I choose to consider this particular i^{th} node because let us say that I have lot of nodes here and then let us say this is the i^{th} gate. Before that I will have I minus 1 gate and so on and then subsequently it follows the other side of gates.

Let us say that this is getting branched j number of times, the i^{th} node output and we need to find out what is the overall capacity here, because I should be able to evaluate the $C_T V_{dd}^2$.

If I want to find out the overall total capacitance here at the i^{th} node and if I have the driving factor because of this particular i^{th} gate which is a two input NAND gate. I should be able to estimate what is the overall parasitic capacitance at this particular i^{th} node. If I know what is the logical effort of this particular subsequent gates which are kind of branched.

It turns out to be its nothing but a two input nor gate. I should be able to know what is the logical effort, from the logical effort, from the driving factor of this particular gates I

should be able to estimate what is overall capacitance is been loaded into this particular i^{th} node.

My total capacitance of the i^{th} node will be nothing but,

$$C_{T_i} = 3C(x_{i,2-Nand}P_{2-Nand} + \sum_j x_j g_{j(2-NOR)})$$

If I consider this will be one particular logical effort, this will be another logical effort, this will be another logical efforts and then so on till we hit the last gate. That is why this is a summation of the overall capacitance. There will be an input capacitance here, there will be an input capacitance here, there will be an input capacitance here, and all this capacitance will get loaded into this particular i^{th} node.

I will have a parasitic node 3C into the driving factor into the parasitic of this particular two input NAND gate plus 3C multiplied by the summation of the input capacity or rather the input capacitance of this gate, this gate, this gate, that is the submission. That is why I have taken the 3C outside and then submission of $x_j g_j$.

Remember that this is the absolute energy for doing the transition of 0 to 1 at this i^{th} node. If I really want to estimate what is the average energy that is been delivered by the V_{dd} at this particular i^{th} node, I should be able to estimate $\alpha_i C_T V_{dd}^2$ and that should be able to give me the energy that is been delivered by the V_{dd} for 1 clock cycle.