Design and Analysis of VLSI Subsystems
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Lecture - 06
Non Ideal MOS model

The long channel ideal I-V characteristics shown in figure 6.1 shows the current I_{ds} versus V_{ds} is plotted in which the current is constant in saturation region. But in short channel non-ideal I-V characteristics the current in saturation region as linear slope shown in figure 6.2.

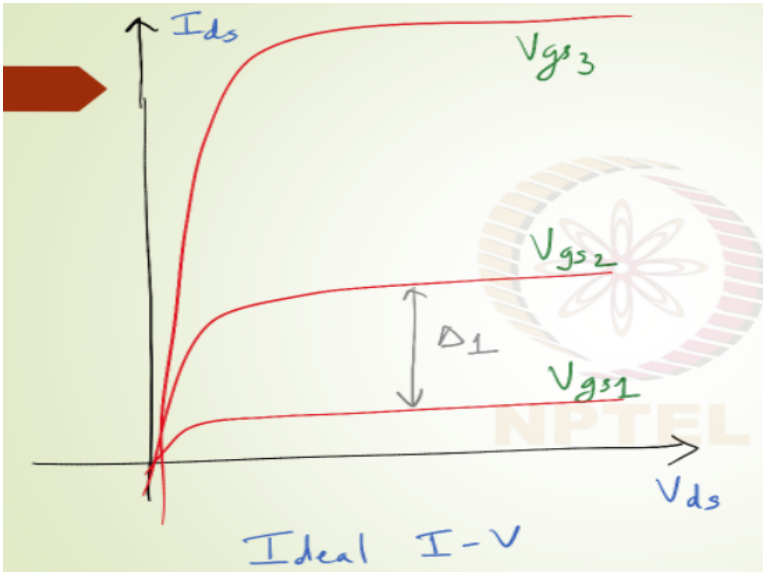

Figure 6.1: Long channel I-V characteristics

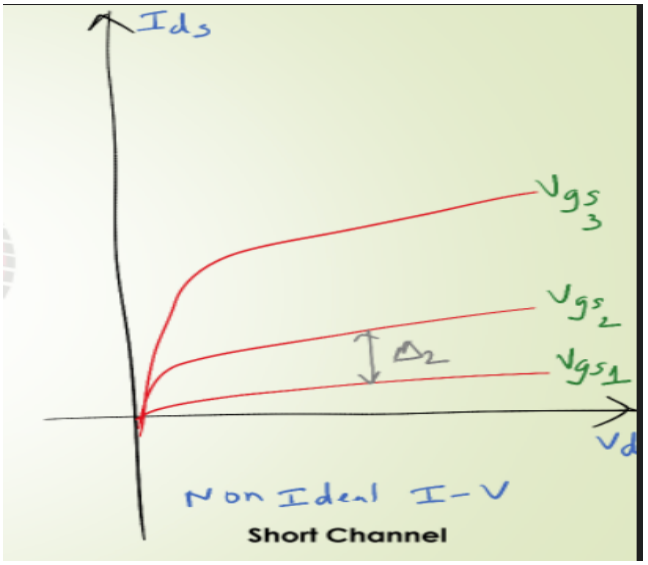

Figure 6.2: Short channel I-V characteristics

By comparing long channel and short channel I-V characteristic, the value of V_{ds} with respect to current I_{ds} is less in short channel. The value of V_{gs1} and V_{gs2} is less for short channel and then an increase in the current is denoted as Δ_2. Whereas for long channel the current is denoted as Δ_1. An increase in the V_{gs} is going to give a proportional to the square of the increase in the V_{gs}.

In non-ideal behavior the saturation current increases less than quadratically with increasing V_{gs}. This is caused by three effects that is velocity saturation, mobility degradation and channel length modulation.

Velocity saturation: In ideal characteristics the velocity is directly proportional to electric field E_{ds} and mobility will be constant. An increase in V_{ds}, I_{ds} current increases. whereas in non-ideal characteristics velocity ceases to increase with E_{ds}. This is called velocity saturation and results in lower I_{ds} than expected at high V_{ds}.

Mobility degradation: At high vertical field strengths (V_{gs}/t_{ox}), the carriers scatter off the oxide interface. This further slows the progress for majority carriers started from source to drain. Hence lower I_{ds} than expected for higher V_{gs}. A high voltage at the gate of the transistor attracts the carriers to the edge of the channel, causing collisions with the oxide interface that slow the carriers. This is called mobility degradation.

Channel length modulation: At higher V_{ds}, $I_{ds,sat}$ increases slowly (not constant as in ideal case) because of short channel at higher V_{ds}. The depletion region near drain starts increasing and shortens the effective channel length.

The mobility degradation of PMOS and NMOS for empirical model is represented as

$$\mu_{eff-n} = \frac{540cm^2/v-sec}{1+\left[\frac{V_{gs}+V_t}{0.54\frac{v}{nm}t_{ox}}\right]^{1.85}} \tag{6.1}$$

and

$$\mu_{eff-p} = \frac{185cm^2/v-sec}{1+\left[\frac{V_{gs}+1.5V_t}{0.338\frac{v}{nm}t_{ox}}\right]} \tag{6.2}$$

Example 6.1: Compute effective mobilities when the transistor is ON, given $V_{gs} = 1V,\ V_t = 0.3V, t_{ox} = 1.05nm$ for 65nm technology node.

Solution: $\mu_{eff-p} = \frac{185}{1+\left[\frac{1+1.5x0.3}{0.338\frac{v}{nm}1.05nm}\right]} = 36.37cm^2/v - sec$

$$\mu_{eff-n} = \frac{540}{1+\left[\frac{1+0.3}{0.54\frac{v}{nm}1.05nm}\right]} = 95.7cm^2/v - sec$$

As increase in electric field for a short channel transistor, the velocity ceases to increase. Also, an increase in electric field at drain to source end, velocity increases linearly initially and after a critical point it reaches to a saturation value. The velocity of the electrons ($V_{sat,N}$) in the NMOS is given as $10^7 cm/sec$ and the velocity of the holes ($V_{sat,P}$) in the PMOS is given as $8x10^6 cm/sec$ shown in figure 6.3.

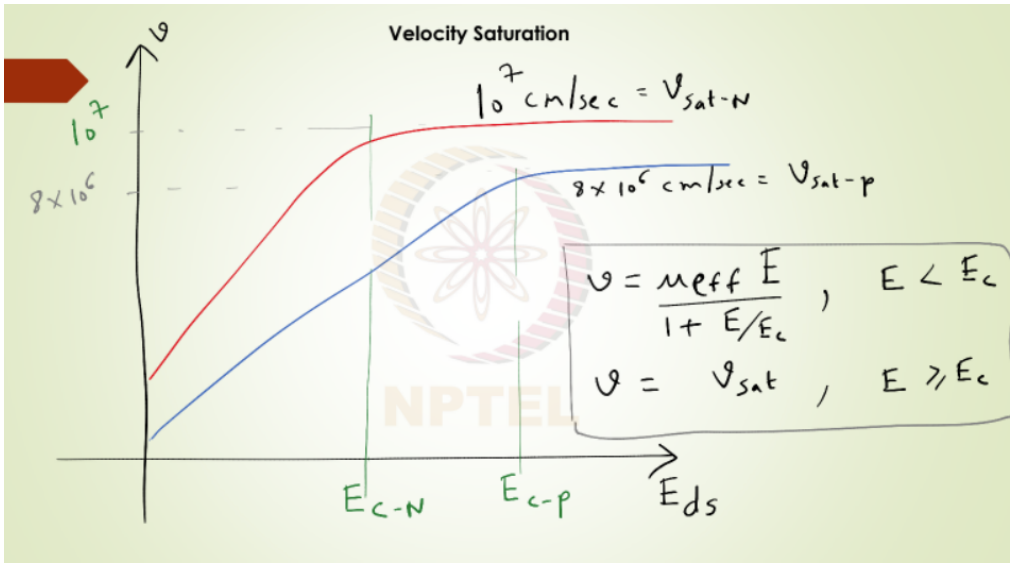

Figure 6.3: Velocity Saturation

the velocity can be approximated is written as

$$v = \frac{\mu_{eff} E}{1+\frac{E}{E_c}},\ E < E_c$$

(6.3)

$$v = v_{sat},\ E \geq E_c \tag{6.4}$$

V_{gs} for electrons reaches earlier than hole.

For low E, $\frac{E}{E_c} \approx 0,\ v = \mu_{eff} E$

For $E = E_c,\ V_{sat} = \frac{\mu_{eff} E_c}{2}$

$$E_c = \frac{2v_{sat}}{\mu_{eff}}$$

Where, $E_c = \frac{V_c}{L}$

Example 6.2: Determine $v_{c-n}\ and\ v_{c-p}$ for 65nm technology node, where L = 50nm.

Solution:

$$E_c = \frac{2v_{sat}}{\mu_{eff}}$$

$$E_c = \frac{2x10^7}{95.71} = \frac{V_{c-n}}{L}$$

$$V_{c-n} = 1.044V$$

$$V_{c-p} = 2.1996V$$

PMOS is not as badly velocity saturated as NMOS. NMOS reaches saturation velocity at earlier velocity than PMOS.