Design and Analysis of VLSI Subsystems
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Lecture - 49
Introduction to Stick Diagram

Hello students welcome to this lecture on Stick Diagrams. Stick diagram is kind of very essential in understanding the overall layout structure and it also helps in characterizing how much of footprint the design will require.

What we will do in this particular lecture is we will go through some of the simple gate structure we will start with an inverter primitive circuit and then we will go into 2 input NAND gates and then one more combinational circuit and then try to analyze or estimate the overall footprint that is required to design that on the chip.

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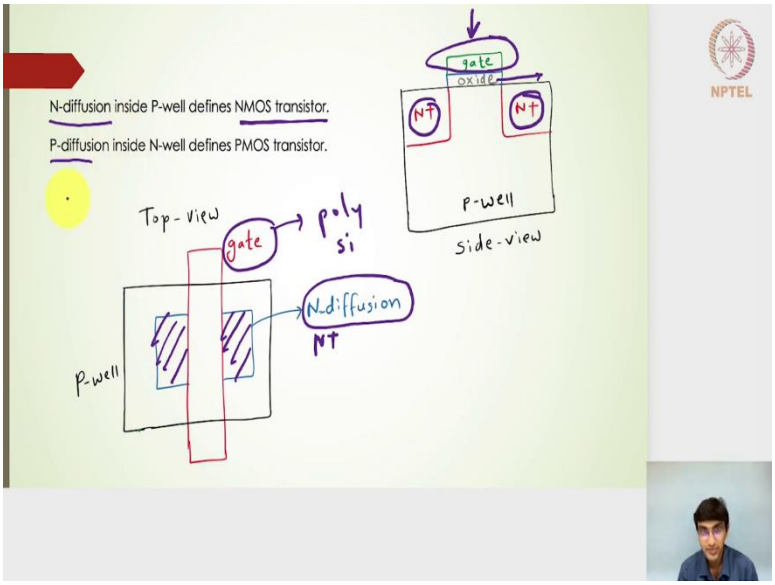

To run quickly to the basics of the stick diagram or rather to the basics of the fabrication process, this is what the slide I have. What we will do is in this particular lecture we will anyways learn the stick diagram, but stick diagram requires some kind of basic understanding or the top view of the overall fabrication process.

In this particular slide what I have done is I have shown the N diffusions. Let me pick up a pointer alright, here is our cross sectional view of the NMOS transistor. We have the P

well here and then on the side pockets we have done the diffusion of N^+ and N^+ and the oxide and then the gate and if we connect the power supplies onto the gate to the source and then drain to the source we will have the transistor operating.

This is a side view structure of the NMOS transistor and then here I have represented the top view structure of the NMOS transistor. If I actually look from this particular side what I will see is this particular gate and then on over or rather on top of this particular diffusion wells, this particular blue box here which is nothing but the N diffusion, it is nothing but our N^+ which I am seeing here on the side view or the cross sectional view.

Then there is this particular black boxes which is nothing but this particular P well. The gate is there this particular part on the top view side the red box here is nothing but the gate structure here represented on the cross sectional view. This is what defines the NMOS transistor, we have a gate and on either side we have the diffusions which is N^+ diffusion are also called as N diffusions and then we have the black box which is a P well.

What we actually say when we look this particular view the top view structure this gate or the polysilicon gate, the gate is generally made up of the polysilicon. I am going to rewrite it as polysilicon, that is the material, that is kind of deposited to form this particular gate structure. If I have this polysilicon gate running across the N diffusions then we get the NMOS structure.

From the top view it looks like this what it also says is I need this kind of a mask layout I need this kind of a masks for fabricating my NMOS structure. Masks in the sense this is. If I require a polysilicon, I require this kind of a polysilicon mask where we will have the deposition of the polysilicon only on this particular portion of the polysilicon box.

N diffusion this is the only the portion where I need to do the N diffusion. Only this particular portion is where I need the N diffusion again and then P well is of course, it will be there everywhere, but to talk about the N diffusion and then the polysilicon this is only the selective process, where I will require the N diffusion and this is where I will require only the polysilicon gate.

Although the polysilicon gate underlying the polysilicon gate there is an oxide here, which of course in the top view we will not be able to see. But that is something which is intuitive

in process or intuitive in understanding. Whenever I see a polysilicon gate beneath that we will have a silicon dioxide there alright.

This is how if we give this set of design to the manufacturers they will easily understand this is what the NMOS, the designer requires an NMOS transistor and this is the 3 masks are there. Which means that I need to follow some kind of a 3 fabrication process one is the P well diffusion the other is the N diffusion and plus diffusion and then we have the polysilicon gate deposition beneath that of course, I need to do the oxide deposition.

This is the basic understanding for developing or for designing the NMOS transistor on the silicon substrate. Just to summarize N diffusion inside a P well defines the NMOS transistors. N diffusion this is our blue box on the P well and if I have a polysilicon gate running across the N diffusion then we will get an NMOS transistor. Again the opposite is also true P diffusion inside an N well defines the PMOS transistors. Of course, what it means is the polysilicon gate running across the P diffusion will give me the PMOS transistor. Hope this is clear going forward.

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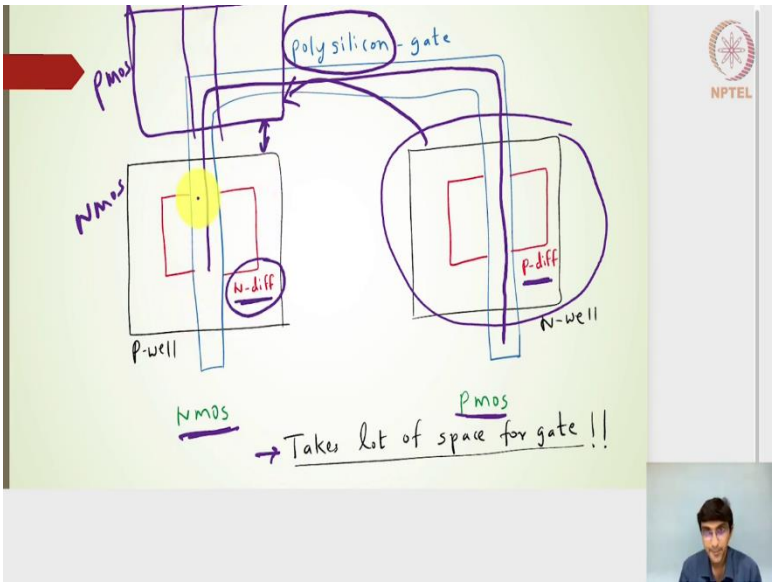

If I want an inverter I will require an NMOS transistor. This N diffusion and then the polysilicon gate running across it will give me an NMOS transistor and I will require a PMOS transistor. I will require a P diffusion and then a polysilicon gate running across the P diffusion will give me the PMOS transistor and I need the polysilicon gates to be

connected. We will just connect it the polysilicon gates and then this polysilicon gate I am connecting by a polysilicon gate and this is how my inverter will represent.

But, it is actually in terms of the layout it is a very bad design, the reason is the polysilicon gate is actually running across and then joining the PMOS transistor. It is better to have this you know put it somewhere here. This particular PMOS structure can be put here, so that I will have my polysilicon gate running like this.

What it means is the polysilicon gate should not actually run across and then connect here, remember that the polysilicon material as such has a little bit higher resistance than that of the copper metal or any kind of a metal.

In that sense if I have a longer polysilicon gate or a longer polysilicon line that is running to form the gate I will have more resistance and avoid that what normally we do is the transistors are designed or rather the inverters are designed such a way that I will have a the PMOS transistor and then the NMOS transistor vertically stacked. Vertically stacked in the sense in the 2 D dimensional footprint I will have the PMOS and then NMOS very close by. Of course, there will be some kind of a distance between these two diffusions and the polysilicon will be running cutting across, both the N diffusions as well as the P diffusions. Instead of doing it side by side we will have it vertically stacked.

That is what we will do. This particular design it is a very bad design, but just an understanding that this is a polysilicon and then they are connecting. But, this takes lot of space for the gate and thereby we have this kind in a 2 dimensional footprint we will place the PMOS and then we will place the NMOS and then we will have the polysilicon running across it.

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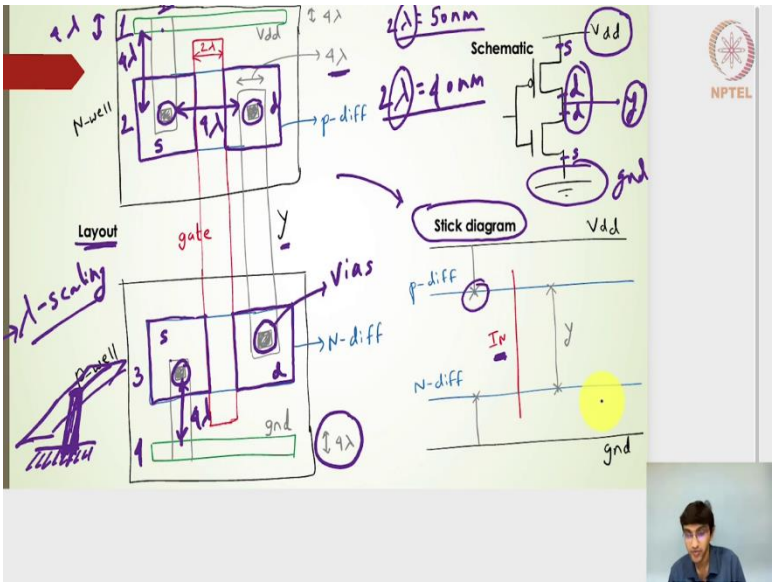

For an inverter this is the schematic of the inverter and this is the layout of the inverter circuit and then this is the stick diagram of the inverter circuit, what we are trying to learn is the stick diagram.

What we will do is schematic, anyways we understand we will have a look at this particular layout and from the layout we will try to find out the stick diagram alright. This is the schematic the PMOS and then the NMOS transistor connected by an input.

This the polysilicon of the PMOS and the polysilicon of the NMOS is actually indicated by the red box here so that is a gate. We have only one polysilicon line cutting across the N diffusion and cutting across the P diffusions. That means, that in the polysilicon gate which is cutting across the P diffusion should give me the PMOS transistor and then the same polysilicon gate which is running or running across the N diffusion should give me the NMOS transistor. We have the V_{dd} rail here and then of course the ground rail here. We have the ground metal line and then the V_{dd} metal line should get connected to the one diffusion here.

This is the particular diffusion. I am going to write it as the source of the PMOS and then the drain of the PMOS on the other side. This the polysilicon cutting across the P diffusion will form two diffusion pockets could be either of the source or the drain.

But, here because this is connected to the V_{dd} I am going to call this particular portion as the source and then this particular portion I am going to call this as the drain. Similarly we will have the source and then the drain for the NMOS. The source of the NMOS is connected to the ground, this is the metal line which gets connected to the ground this is the metal line of the PMOS from the source it is getting connected to the V_{dd} rail.

Let me complete this labeling of the NMOS the drain and the source. Remember that the drain and the drain are connected and then this is my output line. The drains are connected so there is a metal line that is running from the drain diffusions of the PMOS transistors and then connecting to the N diffusion of the NMOS transistor.

This particular metal line is my output node y, that is what is indicated in the schematic alright. We have completed the V_{dd} rail the diffusions getting connected and then the ground. The polysilicon as such the length of the polysilicon gate for any kind of technology node is actually 2 λ.

What it means is for a 65nm technology it will be actually be 50nm. 2 λ = 50 nm in our 65nm technology, λ = 25 nm. The metal line each of the metal lines which are there so indicating this particular metal line and then this particular metal line which is connecting the drain diffusion pockets of the PMOS as well as the NMOS transistors all of them have a length of 4λ they should have a length of 4λ alright.

This is 4λ they should have a minimum length of 4λ, the minimum polysilicon the gate length should be 2λ alright. The separation between this metal line or this particular metal contact or I will call this as a metal line and this particular as a metal line.

The separation between them should at least be 4λ again. I should have a 4λ here and then of course the separation between them should be 4λ. That these are some of the rules for designing the layout and these particular rules are called as the λ scaling rules. I mean there are different rules, but if you go to one of the particular technology vendors who will actually fabricate and give it to us.

They will try to follow some of the rules and most popular will be the λ scaling rule and that is what in the layout we are going to do and that is what we will go we will carry that forward to our stick diagram representation.

What is λ scaling rule represents is for any given technology node. If you actually specify the different features of the layout or the stick diagram alright different features of the layout features in the sense the metal dimensions the metal spacing the polysilicon lengths dimensions and then the metal line the V_{dd} line and then the ground rail ground line whatever is the dimensions.

If we can actually specify that in terms of λ and then we can get it manufactured, but tomorrow if I want to change from 65 nm technology node to 45 nm technology node nothing changes, because the λ is going to change of course.

If I give the same design of the inverter for a 65 nm technology node the 2 λ = 50 nm, but if I actually give this and if I want to design it for a 45 nm technology node, then in that sense 2 λ = 40 nm alright. Nothing is going to change because based on the λ the manufacturers can actually enter the what is the λ value right either 25 nm or 20 nm or if I want to do for 180 nm the λ = 90 nm they can configure or set it and then we can get the manufacturing done easily.

That is one advantage of doing the λ scaling and this is what we are going to follow for the layout as well as for the stick diagram representation alright. There is other things you know what in this particular sense what we are trying to address here is one important point and that is what we are going to follow the one most important point in this particular layout which we need to carry forward is the metal spacing and then the metal dimensions.

The metals are the regions where it occupies more of the footprint or the more of the area. Normally when we design the layout or when we draw the layout if I want to find out what is the footprint or the area of it we actually track the number of metals and then we know what should be the spacing of the metals and what should be the dimensions of the metals and then calculate the overall area.

Even in this particular design of an inverter which is a very simple 2 transistor design, what we will have this metal lines we will calculate the number of metal lines. In this particular case V_{dd} is one metal line and there is a contact here which represents that this particular contact, which ensures that there is a vertical contact running through the diffusions and then coming above and then connecting the metal lines.

These particular contacts are also called as vias, all this small boxes with the colored boxes is nothing but vias. What is the vias is nothing but if I have a diffusion underlying this particular layer is the diffusion and then I will have a metal line that is lining across it. I am trying to draw a design and this has to connect to this particular diffusion, so that I will get the current that will be running across it and then running across it. This particular portion is called as a vertical metal wiring.

What we do is there is some kind of an etching process and then the metal filling process it is very simple chemical process called as the plating process electrochemical plating will be done to fill those regions and then it will form the vias. But, anyways in the top view we will not see the vertical lines what we will see is a small square box, because this vertical line will be seen as a small square box in the top view and that is what is represented in the layout.

Coming back to the number of metal tracks, so what we will see is this V_{dd} is one metal track, round is another metal track and then this contacts which says that there should be a metal line that should start from the diffusions of the source and of course the drain of the PMOS gets connected to the V_{dd} the other one gets connected to the NMOS transistors diffusion.

Similarly, I will have one more metal contacts here which is on the source and the drain side of the NMOS transistor one side it gets connected to the ground the other side it get connected to the drain of the PMOS and then the 4th one is the ground rail. That is another metal line that is on the horizontal side. I have 1 2 3 4 and what we know that the dimensions of the metal, in this sense the width of the metal in this case should be at least 4 λ and then the spacing.

The spacing between this and this should at least be 4 λ. Again the spacing between this and this should be at least be 4 λ and then the spacing between this and this should at least be 4 λ and the width of this particular metal line should be at least be 4 λ. Similarly, on the vertical side we have one metal line. This is one metal line and then we have this particular one metal line, I am going to write it as 2.

The length of this particular metal line should be at least be 4 λ, 4 λ and then the spacing should be 4 λ that is what I have reiterated alright. This is what we have and then we will now draw the stick diagram we will try to understand the stick diagram representation.

We have the layout drawn for the inverter and that stick diagram is basically a very handy rough estimation of the footprint, it does not provide the details, but it just provides where does the polysilicon gate line is there where is the metal line going around and what is the overall footprint.

If I want to actually draw all these boxes instead of boxes, if I want to represent it by a line that becomes much much simpler for our rough estimation. Instead of the V_{dd} a metal box here that is been represented by a single line ground rail which is a box here which is represented by a single line and then the P diffusions here which is represented by again a blue box here and then the N diffusion blue box here is represented by a single straight line. P diffusion and the N diffusion and this vias or the contacts which connects the one diffusion to the V_{dd} rail and then one diffusion to the ground rail is actually represented by a cross and then gets connected to the V_{dd} represented by a cross and then gets connected to the ground. The polysilicon gate which is kind of a box is represented by a straight line again.

A red line with an input saying that this is the polysilicon line and the other side of the diffusion of the PMOS and then the diffusion of the NMOS gets connected by a metal line which will be also be indicated by a straight line.

All the boxes in the layout is actually now represented by a straight line and that forms a stick diagram. Of course, the vias or the metal contacts are actually indicated by a cross symbol just to say that there is a metal contact between the above rail V_{dd} and then the diffusion P diffusion.

Similarly there is a cross here which represents that there is a metal line that is running from the ground and connecting the N diffusions alright. This forms the stick diagram it looks pretty simple. Looking at this particular stick diagram there are not multiple boxes it is a single straight line and looking at it we can easily characterize the layout of any circuit what we have drawn.

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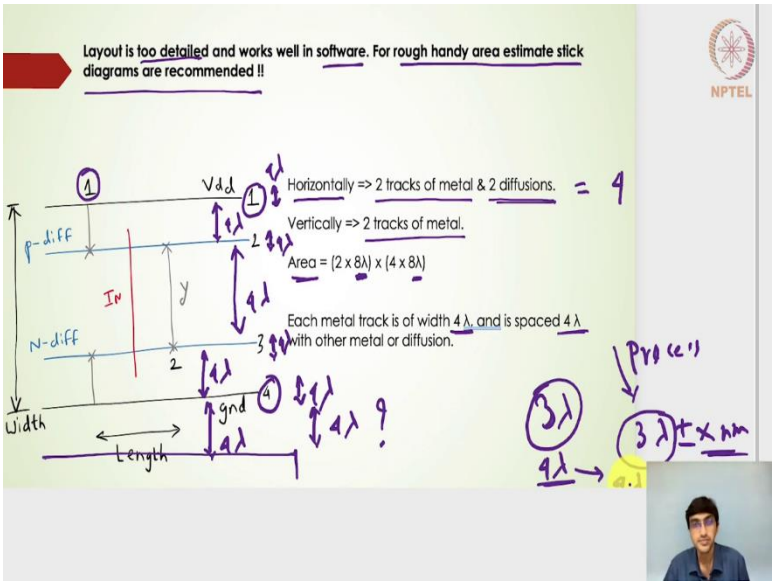

The layout as we as represented in the last slide it is too detailed and works well in the software. If we have a particularly good software I think we will be able to draw the layout very nicely, but for rough handy area estimates stick diagrams are recommended.

In terms of the paper design, if I can easily draw it on the paper and then give you a very rough estimate of the stick diagrams and if you want to optimize in terms of the area we can actually redesign our circuit. Then once again do a rough estimate in terms of the area on the paper and then find out which design is appropriate. This is what we have for the layout in the last slide what we had indicated the number of metal tracks horizontally and then vertically, the same thing I have represented in the stick diagram here.

In the stick diagram you know vertically you know this is the number of the horizontal tracks 1 the V_{dd} rail, 4 is the ground, 3 metal line which is nothing but the contacts 2nd is again the contacts here. I need to have each individual line of the metal line here is actually 4 λ. Each individual line the width of it is 4 λ and then the spacing between the metal contacts should be at least be 4 λ alright. Similarly the number of vertical tracks, here it is 1 because there is one metal line connecting the V_{dd} to the P diffusions and then the N diffusions to that of the ground.

Then there is one metal line which is connecting the diffusions of the NMOS and the PMOS making it the output node. That is what I have written,

$$\text{Horizontally} => 2 \text{ tracks of metal \& 2 diffusion}$$

Horizontally 1 2 3 4 although I have written this as 2 tracks of metal and 2 diffusions what is actually the diffusions are there. But, it is basically the metal contacts on the diffusion which gives me 2 additional metal tracks. Thereby making it the 4 tracks.

$$\text{Vertically} => 2 \text{ tracks of metal}$$

The 2 tracks of each of the metal line should have a minimum of width of 4 λ and then the spacing to the next one should be 4 λ. We can consider if I have one metal line in the stick diagram I can consider that it is to be occupied of 8 λ.

It occupies at least an area of a spacing of 4 λ plus the width of 4 λ, it will give me an occupation of 8 λ. The next metal line should come after 8 λ, in terms of area it is,

$$\text{Area} = (2x8\lambda)x(4x8\lambda)$$

Whatever is that λ will be nothing but 25 nm for a 65 nm technology node. Each metal track is of width 4 λ and then the spacing is 4 λ with the other metal or diffusions.

Now, one may always argue that this particular metal spacing will start from 4 λ. If I can actually do the calculation this is 4 λ spacing and then from here to here it is again 4 λ spacing and then from here to here 4 λ and then the 4 λ width here.

It is actually 4 λ of course the width here is 4 λ and then the width here is 4 λ. The 4 λ, 4 λ and then if I do it, it will be nothing but this 4 λ + 4 λ = 8 λ, this 4 λ + 4 λ = 8λ another 8 λ and then this 4 λ + 4 λ = 8 λ.

The 3 x 8 λ + 4 λ and then we do not require any more spacing of a 4 λ here, one may quite argue that why is this 4 λ is required the reason is normally a chip will not have only one inverter circuits. We will have one more circuit below this or on top of it. In that sense, if I want to start one more circuit here there will be one more diffusions or a metal line that will be running and the spacing of 4 λ is very much required.

In that sense to be very very conservative we will have this 8 λ for each of the metal lines and then whatever is the number of the metal tracks I will get it multiplied. Now, the other question is why is this 4 λ least that is required to design the metal track? I know this is

coming from the highly calibrated fabrication process. If I actually do not have the 4 λ and let us say that if I have a 3 λ the process itself has some kind of a deviations.

If I actually want to have let us say 3 λ of a metal line, we will design the process. The process is highly calibrated and highly characterized and after the process is done what we might actually get is a 3λ±xnm.

We cannot actually get thoroughly 3 λ, it will always be characterized with some small amount of deviations and it is been the process has been so much studied or investigated that with the 3 λ of metal spacing or a 3 λ of metal width it does not give the best results whatever we expect it to.

Hence we know the minimum width or the minimum length of the metal track should be at least be 4 λ and even if with the 4 λ we will have some kind of a deviations 4λ±x it is likely to give a better results, hope this is clear.

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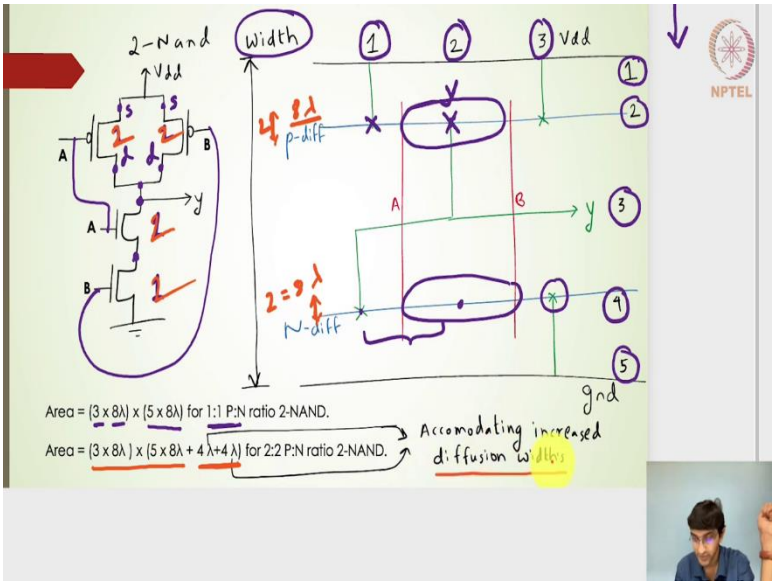

Moving forward this is the 2 input NAND gate circuit and then we want to draw the schematic of this and then try to identify what is the overall footprint. The schematic of the 2 input NAND gate as we know it is 2 of the transistors in series and then 2 of the transistors in parallel.

Now, A and B and if I want to draw the stick diagram, I will anyways have the V_{dd} rail, I will anyways have the ground rail and the P diffusion and N diffusions are there. The

polysilicons which will cut across the P diffusions and N diffusions forms the NMOS and the PMOS transistors.

Here we will have the A polysilicon, basically this A and then this A are connected in the schematic and then this B and then this B is connected in the schematic. I will have one polysilicon line which will cut across the P diffusions and N diffusions. That means, that the P diffusions on one side of the diffusion. On one side of the diffusion it gets connected to the V_{dd}, this is what is getting connected to the V_{dd} and then on the other side of the A polysilicon, this is this particular side I am talking about, this is this particular side and I have a cross here. Of course, there is a cross here also which says that this is connected there is a metal line that is connecting to the V_{dd} rail. This cross is this particular cross which is the output node. I can write it as the output y, this particular output node is a common node between the B transistors on the B PMOS transistors on one side of the B PMOS transistors you know this one.

In fact, I will write it as the drain and then the drain and then the source and then the source. The drain on the B and the drain of the A transistor and B PMOS transistors are both connected and that is the output node. That is what I have written here the output node.

The B polysilicon the other side is the source, one source diffusion which gets connected to the V_{dd}. In this particular case this particular diffusions is a merged diffusion and it is a contacted diffusions. This particular contact is our output contact which actually goes to the A transistor on the NMOS side.

A transistor N diffusion and then A polysilicon gate cutting across it will give me the A transistor on this particular side. On one side it is in the diffusions of the A transistor and then the diffusions of the B transistor are merged together, but there is no contact there.

That is this particular point, the B polysilicon and A polysilicon whatever is common here that becomes this particular point in the schematic and then we have the other side of the B transistor which is connected to the ground. The other side of the polysilicon of the B is this one which gets connected to the ground.

I have now the output node y which gets connected to the one side of the diffusion of the A transistor. The output y node gets connected to the one side of the diffusion of the A

transistor, that is this particular point. This completes the stick diagram, what are we interested in we are interested in the area or the footprint. Let me track the number of metal lines and of course the diffusion lines. Let me start in from this particular side the horizontal side and remember that this particular horizontal side or this particular dimensions is the width and then this particular dimensions is the length.

In terms of the width I will track number of metal tracks horizontally horizontal metal tracks. This will be the 1 metal line the V_{dd} 1, 5th one is the ground metal line and then we have the two diffusions 2 and 4 and in between there is an output node which is the 3rd metal line.

I will have 5 tracks x 8 λ. On the vertical side I will have the number of vertical tracks will be 1 and then you know there is one here which can be aligned with this one and then there is one here which can be aligned with this one and then there is one here which is the 2nd one. 3 metal tracks running vertically so that will be 3 x 8 λ.

For a P you know for a size of 1:1 P:N ratio. The 1:1 in the sense if I have a size of 1 here, a size of 1 here, a size of 1 here, a size of 1 here, ratio for a 2 input NAND gate then I will have this area,

$$\text{Area} = (3x8\lambda)x(5x8\lambda)$$

But, suppose I want to have an equal falling resistance and an equal rising resistance with that of the 2:1 inverter. In that sense instead of a size of 1 I need to have a size of 2 here, I need to have a size of 2 here, I need to have a size of 2 and I need to have a size of 2 what it implies is the N diffusion which we were considering it to be 4 λ, 4 λ = 100 nm in the 65 nm technology, that represents the scale of 1 alright.

For a scale of 2 it should be nothing but 8 λ and then similarly here the P diffusions the scale of 2 represents 8 λ. We were considering 4 λ and then we were calculating the number of metal tracks x 8 λ because 4 λ is the width and then additional spacing of the 4 λ. Here now because the scaling is 2 the width of the diffusion is 8 λ and additional spacing of 4 λ is required.

$$\text{Area} = (3x8\lambda)x(5x8\lambda + 4\lambda + 4\lambda)$$

What we have is an area which is a kind of increased by 4 λ on the PMOS side on the P diffusion side and then 4 λ on the N diffusion side, this is what I call it as a accommodating the increased diffusion widths.