Design and Analysis of VLSI Subsystems
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Lecture - 48
Domino gates

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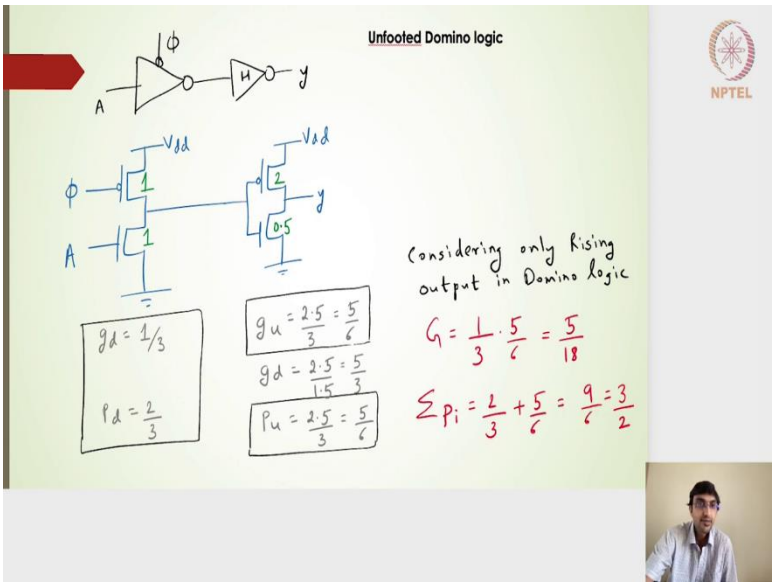

Hello students welcome to this lecture. We will continue with the Domino logic gates and in this particular lecture we will specifically look into one particular non inverting configured combinational gates and try to determine the best gate size so that we will get a minimum delay.

This is an unfooted domino logic, what it really means is we have the dynamic logic here, dynamic inverter and then followed by another inverter. The dynamic inverter and if it is unfooted we will have this kind of a schematic, unfooted means the foot transistor is not there. The logic A or the input A is given to this particular NMOS transistor.

On the PMOS transistor it is anyways clock, this represents our dynamic logic inverter followed by a regular inverter which makes it as the consolidated structure, now becomes a domino logic or the domino circuit. Notice that the domino logic or the domino circuit will always be applicable for a non inverting configuration or the non inverting output.

Based on the input here I will get an inverted output here and then y will be the non inverting output for the input A.

In this particular gate level structure the representation of the dynamic logic is nothing but a regular gate structure of an inverter, but because it is a dynamic logic we have associated or it is attached with a clock signal and it is bubbled which represents that this clock signal is going to the PMOS side of the transistor.

This particular structure is cascading to the next regular structured inverter and I have written a H here, H here represents the high skew inverter and let us talk about this high skew inverter. What we have seen in the dynamic logic, the dynamic logic has a problem when the output actually falls down.

We always need a rising output and that is why or rather the rising input, because if suppose I cascade this particular dynamic logic to another dynamic logic then if I have the falling output, this falling output will become an input to another dynamic inverter and that is where the problem arises.

What we do is we have an inverter here and the falling output is converted into a rising output here which then goes and feeds into the next dynamic circuit, it may be an inverter or it may be any other NAND or NOR gates. The falling output here is converted into a rising output here which is then fed as an input to the next dynamic logic circuit.

In that sense this particular dynamic logic output here or the dynamic inverter here we are interested only in the falling output. The reason is very simple if A = 1, I will get the output to be falling it will go to 0, if A = 0 in the evaluation mode, because this particular output node is anyways charged or precharged to V_{dd} it will stay at V_{dd}.

A whenever it is 1, then only this output of this dynamic inverter will go to 0 and thereby we will be interested only in the falling output because the rising output or the high level logic will be staying or will be retained in the evaluation mode. We do not have to worry about the delay of the rising output. We only have to worry about the delay for the falling output, for the rising output the delay will be actually be 0 because it is anyways retained. The precharge has this particular output node is precharged to V_{dd} or logic level high and it will be retained to the logic level high.

Only when A = 1 it will fall and that is what the delay, we are interested in. What we will do is in this particular dynamic part of the domino logic structure for this particular first stage we will be interested only in the falling down output that means, the logical effort for the falling down and then the parasitic for the falling down is what is interesting to us.

We calculate that the falling down one and then the parasitic down and anyways dynamic logic always has you know, when we represent the logical effort or the parasitic, we always represent for the logic the output going down signal. We have for an unfooted,

$$g_d = \frac{1}{3}$$

$$P_d = \frac{2}{3}$$

In this particular configuration, since the output is falling down we need the output here will be rising. In that sense if we are interested in the falling down signal here, why not make this rising up signal really fast and that is where the high skew inverter will be used.

A standard high skew inverter is 2 instead of 2:1, we make this 2, we retain this 2, the size of 2 in the PMOS side and on a NMOS side we make the strength of the NMOS less. Normally we will associate with making the strength to be half that of the 2:1 inverter and that is why we have the strength of 2 and 0.5.

The width of this PMOS remains to be 2, NMOS width is reduced to 0.5 and thereby we now have a high skew inverter. The advantage of the high skew inverter is this is going to really be faster in getting the signal to rise to a logic level high. Here we will get the output going down and here we will get the output going up and thereby if I make this high skew inverter, we will get a really fast output.

Now, what should be the logical effort and then the parasitic for the rising up signal? that is what g_u represents,

$$g_u = \frac{2 + 0.5}{3} = \frac{2.5}{3} = \frac{5}{6}$$

The parasitic for the rising up again it will be,

$$P_u = \frac{2.5}{3} = \frac{5}{6}$$

Going down logical effort I have just noted it here, but not really of any relevance for the domino logic. The g_d will be nothing but,

$$g_d = \frac{2.5}{1.5} = \frac{5}{3}$$

Considering only the rising output in the domino logic. Our overall G which is nothing but the product of all the g's which will be the g_u here and then the g_d here will be,

$$G = \frac{1}{3}\frac{5}{6} = \frac{5}{18}$$

I have taken the summation of all the parasitic just because we are interested in finding out the overall delay. The summation of the parasitic will be nothing but,

$$\sum P_i = \frac{2}{3} + \frac{5}{6} = \frac{9}{6} = \frac{3}{2}$$

Hope this is clear.

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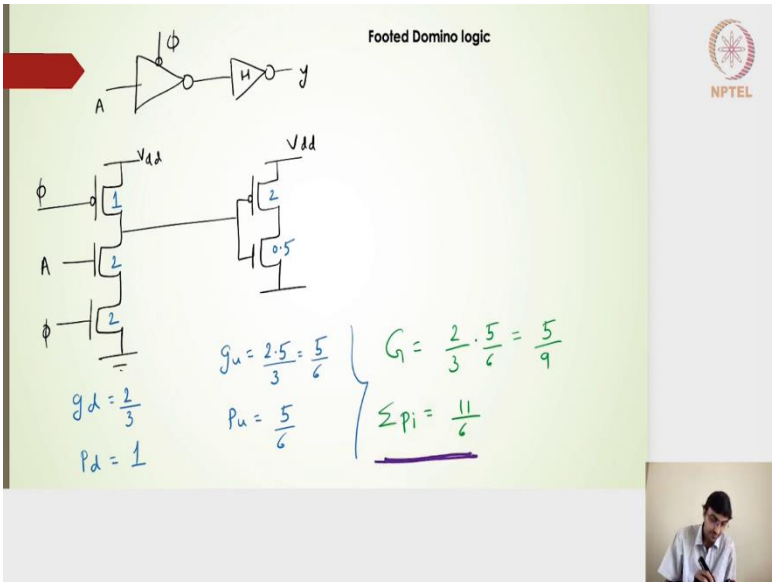

Moving ahead, let us look at a similar configuration, but we have an footed domino logic what it really means is we have instead of a unfooted dynamic logic here we have a footed dynamic logic put both of them together.

Footed one we will have a foot transistor and then this will be connected to the clock same as that of this clock which is getting connected to the PMOS transistor. During the pre-charge mode this will be on, this will be off, there will not be any contention. With this the output node of this dynamic logic will get precharged to V_{dd}, the size is 2 and 2, it becomes the total switching resistance turns out to be R which is very similar to that of the 2:1 inverter falling resistance.

Again, high skew inverter is been applied here in the next stage so that we will get a really fast rising output in the output of the inverter, in the output of the second stage. Let us try to evaluate the logical efforts, the logical effort here is gd for the falling output will be nothing but,

$$g_d = \frac{2}{3}$$

Parasitic will be,

$$P_d = 1$$

This remains the same as that of the previous case the logical effort of going up for an high skew inverter is,

$$g_u = \frac{2.5}{3} = \frac{5}{6}$$

The parasitic is also,

$$P_u = \frac{5}{6}$$

Again, the multiplication or the product of the logical efforts for both the stages put together will be,

$$G = \frac{2}{3}\frac{5}{6} = \frac{5}{9}$$

Then the summation of all the parasitic will be,

$$\sum P_i = \frac{11}{6}$$

What we have seen so far is the unfooted domino logic and then the footed domino logic and then we have evaluated the logical effort and then we have evaluated the parasitic, the total parasitic.

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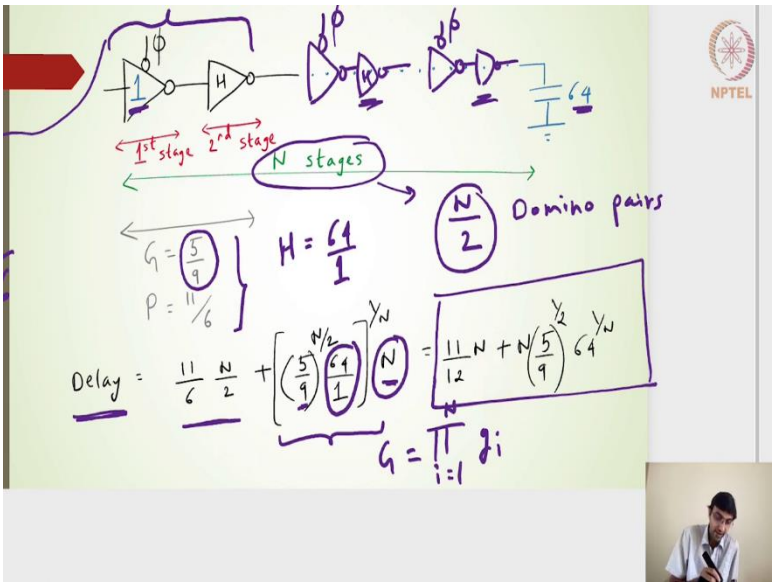

Let us try to see an example here and try to evaluate the best number of stages, we need to design for the domino logic equivalent circuit or a domino logic complied circuit which has a load capacitance of 64C, where 1C represents the unit NMOS transistors capacitance and here the first stage sees a input capacitance of 1.

Again we need to find out what is the number of stages in this particular circuit and what should be the best or what should be the sizes of those gates or the stages so that we will get the minimum delay. Earlier we had seen a similar kind of an example where we had the best number of stages, best number of inverters so that we will get the minimum delay and it was especially for the same or the exact load capacitance and then the exact input capacitance.

Now the example has been changed little bit and we are trying to see what is the best number of stages considering the domino logic. That is the difference and let us say that

this is I have taken this as $\frac{5}{9}$. If I go back $\frac{5}{9}$ is this particular logical effort, the product of this logical effort the product of both of them is the $\frac{5}{9}$, it is an or it is a footed domino logic.

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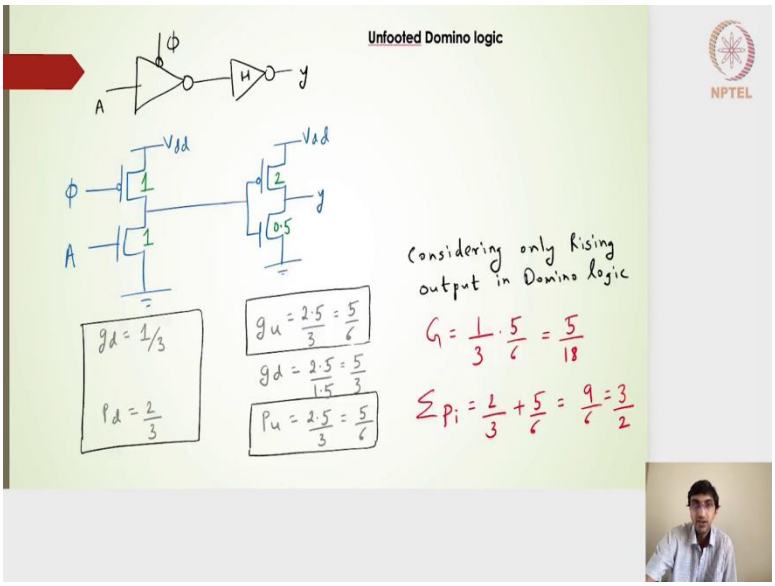

If I go back the previous slide the G here for an unfooted domino logic is $\frac{5}{18}$. Coming back to the current slide, what we will consider is put together these two stages. Let me get my pointer, this will be considered as one domino logic and let us say that we are interested in designing this whole stages in terms of a footed domino logic, its G value let me put it here should be $\frac{5}{9}$. I am considering this to be 1st stage and then this to be 2nd stage and then similarly we will have 3rd, 4th, 5th, 6th and 7th and 8th and all that we will get the minimum delay.

What you really need is an expression of the delay in terms of the N stages and then try to optimize it. If I consider this to be an N stages the dotted lines will be the N stages, and G is,

$$G = \frac{5}{9}$$

Then the total parasitic which we have calculated earlier in the previous slide was,

$$P = \frac{11}{6}$$

The summation of Pi for the first two stages, I will write it as I = 1 and 2 was $\frac{11}{6}$. I have considered these two for the first two stages and then we will keep on adding the domino logic and then similarly we will keep on adding the domino logic and the number of domino logics we will add that we will get the minimum delay that is the first thing. The second thing is we need to estimate what should be the size of this high skew inverter, what should be the size of the dynamic inverter here and dynamic inverter here and then what should be the size of the high skew inverter. Let me write the delay expression considering N stages.

If it is N stages, note that this N stages will have $\frac{N}{2}$ pairs of domino logic. $\frac{N}{2}$ pairs, let us say that if the number of stages is 10 that means, that a total number of stages is 10. The domino pair will be 5 that means, that we will have 1 dynamic inverter and followed by another regular inverter and that will be one pair and similarly 5 such pairs will be there alright. $\frac{N}{2}$ is what I am considering for the domino pairs. Let us try to write the delay expression and the summation of the parasitic is $\frac{11}{6}$ for one domino pair.

$$Delay = \frac{11}{6}\frac{N}{2} + \left[\left(\frac{5}{9}\right)^{\frac{N}{2}}\frac{64}{1}\right]^{1/N} N = \frac{11}{12}N + N\left(\frac{5}{9}\right)^{1/2} 64^{1/N}$$

If I have $\frac{N}{2}$ pairs the overall parasitic will be $\frac{11}{6}\frac{N}{2}$ and then the overall path effort and multiplied by the N stages is what will give me the overall delay. The parasitic plus the total path effort in the sense the total stage effort the individual stage effort multiplied by the N stages should give me the overall delay.

Here the number of stages is N, that is fine and this particular portion what I have done here is this is the individual stage effort that is what I have represented or I have written. If I closely look into this, this G value is $\frac{5}{9}$, we will come to that later $\frac{64}{1}$ will be our capital H which is nothing but the product of all the electrical effort or the fan outs.

Starting from the last stage to the first stage, it will be nothing but $\frac{64}{1}$, this portion is hopefully this is understood, if I am considering the G here for N stages it will be nothing but,

$$G = \prod_{i=1}^{N} g_i$$

But, here we know that for the two stages the 1st and 2nd stage and similarly 3rd and 4th stage and so on for one domino pair consisting of two stages it is actually $\frac{5}{9}$. For N such stages what we will do is $\sqrt{\frac{5}{9}^N}$, it becomes $\frac{5}{9}^{N/2}$. That becomes my overall $GxH^{1/N}$ will give me the best stage efforts so that we will get the minimum delay again hope this is clear.

Finally, we will get this particular expression for the delay and we know what to get the minimum delay, we can differentiate this delay expression with respect to N, that we will get the best of the optimal N value.

$$--= 0 => \frac{11}{12} + \sqrt{\frac{5}{9}}\left[64^{\frac{1}{N}} + \frac{N\, 64^{\frac{1}{N}} \ln(64)}{-N^2}\right]$$

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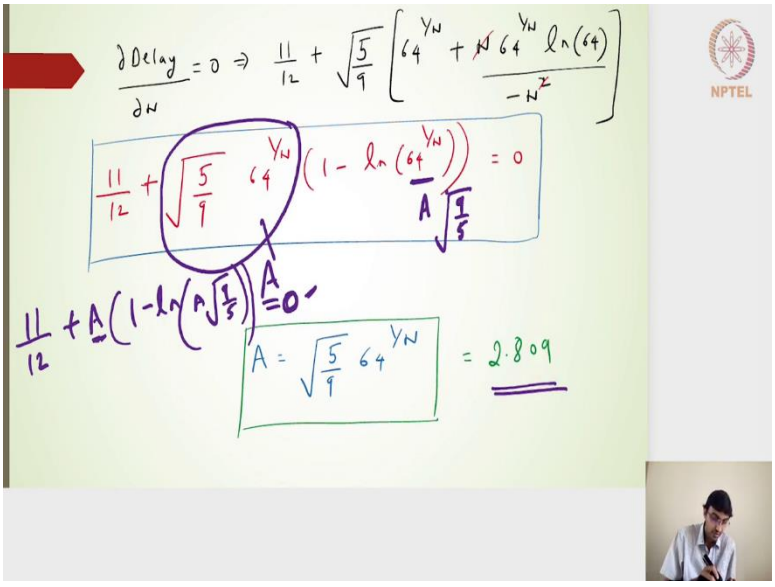

$$\frac{11}{12} + \sqrt{\frac{5}{9}} 64^{\frac{1}{N}} \left(1 - \ln\left(64^{\frac{1}{N}}\right)\right) = 0$$

$$A = \sqrt{\frac{5}{9}}64^{\frac{1}{N}} = 2.809$$

Heuristically means I will have this particular equation, I will have this particular equation written like this

$$\frac{11}{12} + A\left(1 - \ln\left(A\sqrt{\frac{9}{5}}\right)\right) = 0$$

I keep plugging in the values of A as 1 or 2 or 3 and then in between that 2.5, 2.8, 2.9 and then it should equate it to 0 or whatever the closest value that A can accommodate, that I will get closer to the 0 value that will be the solution and the solution turns out to be 2.809, hope that is clear.

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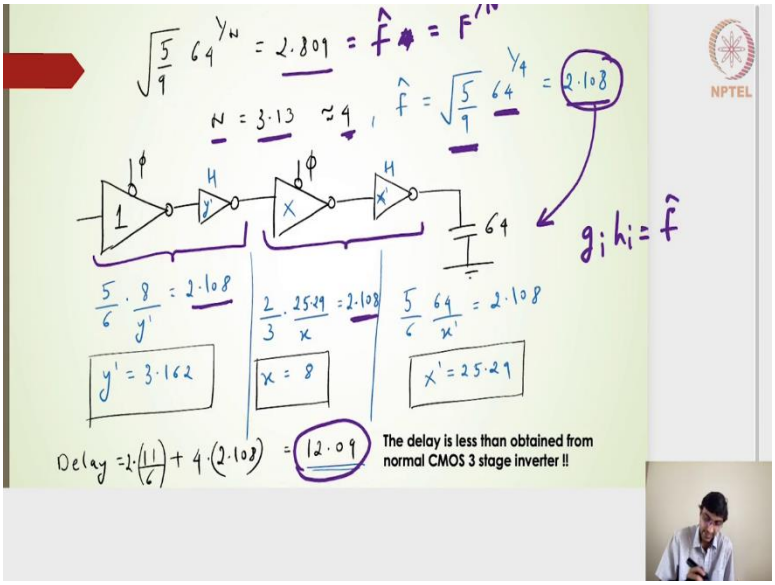

Once I have this 2.809 and if you remember,

$$\sqrt{\frac{5}{9}}64^{1/N} = \hat{f}$$

This is the best stage effort we want. Using this particular $\hat{f}$ let us try to see what should be the best stage, best number of stages we have to get so as to get the minimum delay.

Now, the $\hat{f}$ = 2.809 and which will be nothing but $F^{1/N}$ or rather I will write it as an $\hat{N}$. For getting 2.809 alright what should be that $\hat{N}$? that $\hat{N}$ = 3.13. The $\hat{N}$ = 3.13 and we cannot have 3.13 as a number of stages.

We always want the number of stages in a domino logic to be the even numbers. Instead of 3 we will have to go for 4 as a number of stages. If the number of stages is 4 actually then what should be this individual stage efforts? Which will be nothing but,

$$\hat{f} = \sqrt{\frac{5}{9}}64^{1/4}$$

Each of the stage will see $\sqrt{\frac{5}{9}}$ and because the load is 64 and then the input capacitance is 1, we will have the $64^{1/4}$. The $\hat{f}$ the best stage effort for the individual stages turns out to be 2.108 instead of 2.809, this will be the best stage effort we can see for a domino logic.

If I use this on the individual stages, then I should be able to find out what is the best gate size and from the gate size we can easily find out what is the transistor size. The best gate size I can find it out by equating this $g_i h_i = \hat{f}$, which is 2.108. The $g_i h_i$ for this particular inverter is nothing but,

$$\frac{5}{6}\frac{64}{x'} = 2.108$$

$$x' = 25.29$$

This is the gate size or its the basically the input capacitance for this particular regular inverter which is a high skew inverter. Similarly, if I want to find out the X value which is something, but the gate size of this dynamic inverter, I now know the x' value and its $g_d = \frac{2}{3}$,

$$\frac{2}{3}\frac{25.29}{x} = 2.108$$

$$x = 8$$

For this dynamic inverter the x or the gate size is 8. We have to appropriately design the transistor sizing for this dynamic inverter as well. This particular high skewed inverter again I have given the size of y' and we need to find out y'

$$\frac{5}{6}\frac{8}{y'} = 2.108$$

$$y' = 3.162$$

Again, it is a high skewed gate size, the overall delay in this case will be nothing but,

$$\text{Delay} = 2\frac{11}{6} + 4\,(2.108) = 12.09$$

The overall delays turns out to be 12.09 and if I closely look into the regular structured inverter we had the minimum delay as 15. Here the minimum delay turns out to be 12.09.

There we obtain the minimum delay of 15 using 3-stages here with the 4-stages in fact, two pairs of dominic logic family we are getting a delay of 12.09 < 15 value which is a normalized delay value not an absolute one. If I want to find out an absolute value of the delay I have to multiply by 3RC value and if we have the RC value as 1 picoseconds we can calculate the absolute delay, hope this is clear.

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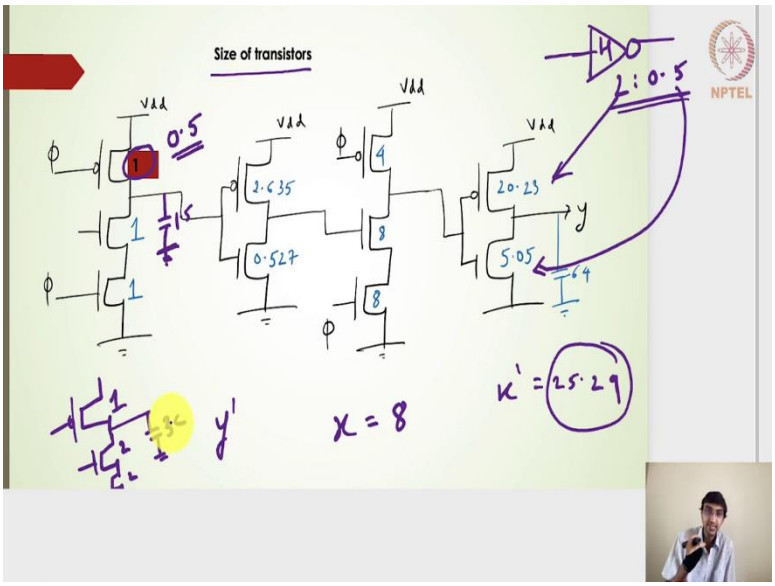

The sizes of the transistors because we have the sizes of $x' = 25.29$. What we will do is this is a high skew inverter, what I had written was a high skew inverter and if you remember the sizes was 2:0.5. What we are going to do is this particular 25.29 we are going to divide it into 2.5 parts, where 2 parts will go here and then 0.5 parts will go here and that is why we get 20.23 and 5.05.

Similarly, the x value for the dynamic inverter which is nothing but the gate size of the dynamic inverter was nothing but 8. The 8 will be put in here where the input is connected and for the foot transistor it should be similar to that and then, for the PMOS side we will take half of it. This one also we will have whatever is the value we obtain of y' we will do 2.5 parts 0.5 parts will go here on the NMOS side and then 2 parts will go into the PMOS side.

Lastly, the gate size is anyways 1 here, we will have 1 1. This particular size of the dynamic inverter here in the first stage if it is the size of 1, the clocked PMOS transistor should have a size of 0.5 so that we will have this particular parasitic to be 1.5 and that will give me the 1.5 will be considered appropriate.

If you remember we had a size of 1 here and then the size of 1 here 2 and 2 which gave us the parasitic of 3 capacitance, and then divided by the parasitic of the 3 capacitance gave us the normalize parasitic as 1, here it should be 0.5 instead of 1.