Design and Analysis of VLSI Subsystems
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Lecture - 35
Optimizing Gate Sizes Example

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Here the optimization is the first part of the lecture, we will do the optimization with respect to the sizes keeping in mind for the circuit, which has multiple branches and later on we will introduce into the number of stages.

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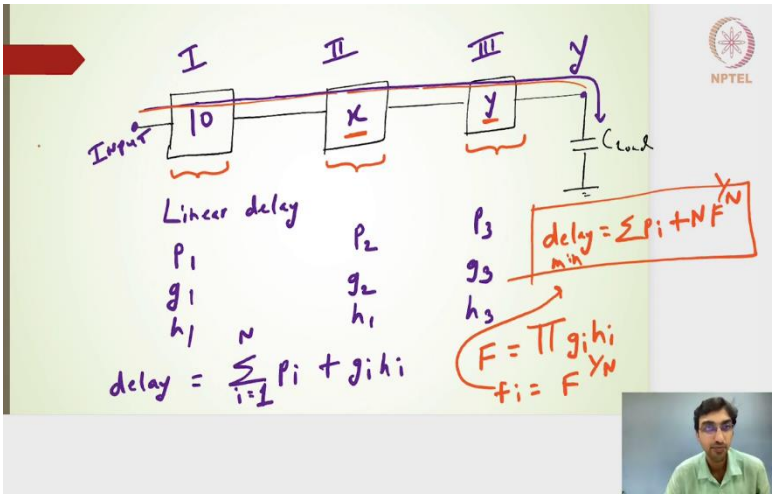

Let me create a single branch circuit and a single path circuit. Let us say that the initial I have one gate it could be an inverter or a NAND gate or a NOR gate or any other gates and then we have one more gates here and then we have one more gates here and then finally we have some kind of a load here and this is the input. What we are saying is we were using the linear delay model whether we can estimate the propagation delay from this to this particular point.

I will call this point as a y point and then this particular point as an input point. To make it simpler we have used a linear delay model method and we identified the p_1 value, the g_1 value, the h_1 values and similarly for the next stage. This is the first stage, this is the second stage and this is the third stage.

The third stage is loaded with some external capacitance or it could be considered as load coming from the another part of the circuit and then similarly the second stage we will have the normalized parasitic, the logical effort and then the electrical effort and then similarly p_3, g_3, and h_3. The linear delay model method says that the overall delay for the normalized delay is nothing but,

$$\text{delay} = \sum p_i + g_i h_i$$

Where i is for this particular case it is 1 to N, where N is nothing but the three stages.

Now based on this particular delay, if suppose we have some kind of a constant value here let us say we assume we have some given gate size as 10, but the second and then the third stage is unknown we should be able to find out what is the x value here what is the y value here so as to attain the minimum delay.

If I want to find out the minimum delay we know that there are three stages, one is this stage, the another one is this one, the another one is this one. There are three stage we will find out what is the overall path effort for this particular path what is the overall effect effort, that we can calculate it using $g_i h_i$ and then the product of all the three stages based on that we should be able to find out the best individual stage effort. So, that we will get the minimum delay which in turns out to be nothing but $F_i = F^{1/N}$.

1 by Nth root of the path effort should give me the individual stage effort being the best, so that we will get the minimum delay. If we can calculate this one then the minimum delay will be nothing but,

$$\text{delay}_{\text{min}} = \sum p_i + NF^{1/N}$$

Hope you know this is something you have understood up till this particular point of time.

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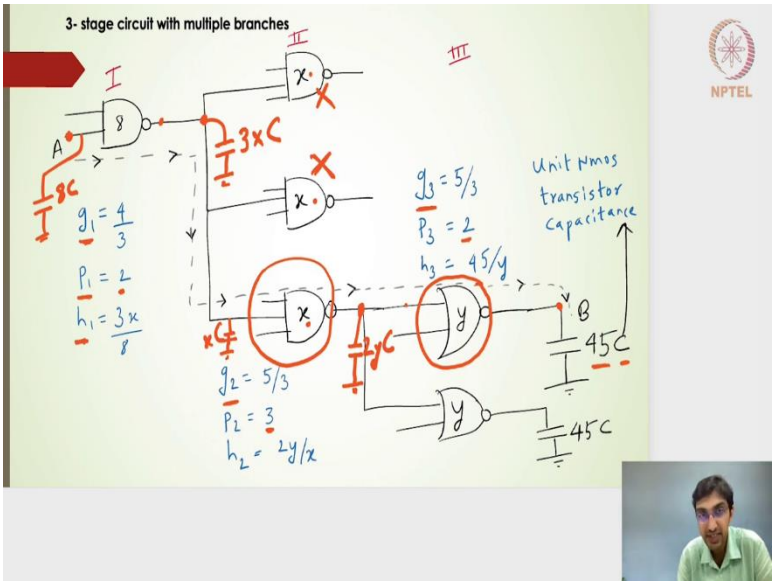

Moving forward, let us say I have another circuit here. I have in the first stage here and then the second stage and then the third stage and here it is slightly different in the sense that the first stage we see a 2-input NAND gate the second stage there are three branches. The first stage output gets branched into three times and then the second stage, in the second stage we choose one of the 3-input NAND gates. In the second stage there are three such 3-input NAND gates and one of them is connected to the first stage output. In fact, all the three 3-input NAND gates are connected to the first stage output, but here I have made a arrow direction saying that this is the path we are interested in.

I am going to consider this particular 3-input NAND gate and output of this is going to the two such 2-input NOR gates. The second stage sizes and all of them whatever gates we have here in the second stage 3- input NAND gate all of them have a size of x and in the third stage all the 2-input NOR gates have a size of y and the output is connected to some external capacitance which is normalized to 45C.

That means 45 times the unit NMOS transistor capacitance is what is the effective load which is seen at the output B here. The dotted arrows implies that we are interested to find out the propagation delay starting from the point A to the point B. We are not interested in any other paths from point A to somewhere this particular path we do not know what exists after this.

We are not interested in that, we are not interested in this you know the second output of the second 3-input NAND gate, what we are interested in is this particular path where in the first stage is the 2-input NAND gate, the second stage it is the third out of the three such NAND gates the third one 3- input NAND gate and an output of that which will go to the first 2-input NOR gate and then that goes to the 45C external load capacitance.

It is slightly different in the sense that there is a branching at the output of the first stage there is a branching at the output of the second stage here. Let me try to know if we are using the linear delay model let us try to identify what are the individual p, g and h values.

The individual p values is nothing but the normalized parasitic for the 2-input NAND gate or the 3-input NAND gates or the n-input NAND gate is nothing but the number of inputs. $p_1 = 2$ here for the first stage, for the second stage $p_2 = 3$ here and I have written $p_2 = 3$ here which means I am considering this particular individual 3-input NAND gate.

I really do not care about this particular one although this will be included in some form, but for finding out the g and p values it does not really matter because this is the three input NAND gate which is going to drive the parasitic which is going to drive the current to charge the capacitance at this particular node anyway.

$p_2 = 3$ here and then we are interested in this particular 2-input NOR gate, $p_3 = 2$ here, logical effort for a 2-input NAND gate is nothing but 4/3 for a 3- input NAND gate, it is 5/3 and for a 2-input NOR gate, that is what is estimated here.

Electrical effort, now we have to account for the three branching. The electrical effort here h1 in this particular stage the outward is getting a branch to three such 3-input NAND gates, that means if I find out the input capacitance at this particular node the output of the first stage the input capacitance that is coming from this particular branched 3-input NAND gate from this particular branch 3-input NAND gate and then from this particular 3-input NAND gates overall I see 3C.

The input capacitance for this particular first stage 2-input NAND gate, if I consider the input capacitance here it will be nothing but 8C. My electrical effort or the fan out in this case will be nothing but $\frac{3x}{8}$ or whatever $\frac{3xC}{8C}$, the C and C gets canceled and then finally we have the electrical effort or the fan out as $\frac{3x}{8}$, hope this is clear.

For the second stage, there are two branches. The overall capacitance that is seen input capacitance coming from the third stage at the output of the second stage will be nothing but 2yC The overall electrical effort or the fan out is nothing but $\frac{2yc}{xc}$.

It will be nothing but $\frac{2yC}{xC}$. We will get $\frac{2y}{x}$, the electrical effort for the third stage will be nothing but $\frac{45C}{yC}$, the input capacitance here for this particular input I am taking about is nothing but yC, this $\frac{45}{y}$ will be the electrical effort for the third stage, hope this is clear, moving forward.

Now I have a g value, p value and h value. The overall normalized delay will be nothing but,

$$\text{delay} = \sum_{i}^{N} p_i + g_i h_i$$

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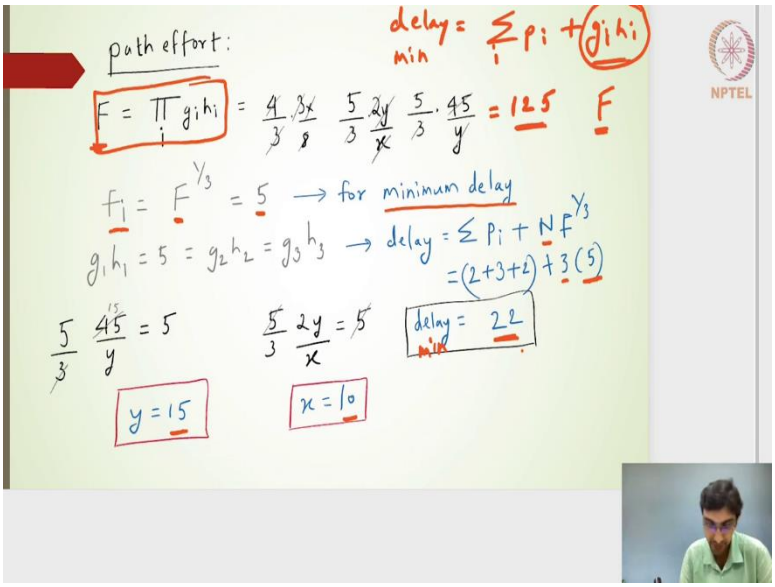

That will be the overall delay, that is something I might have written somewhere if not I will write it down here. The overall normalized delay I am going to write it down as the summation pi and then $g_i h_i$.

For estimating the minimum delay here what we had identified is, if I can find out a value of the product of $g_i h_i$. If I do not have the variables x and y that is something we need to calculate so that we will get the minimum delay, but if I somehow find out the product of $g_i h_i$ which is nothing but the path effort here F value and then the product of $g_i h_i$ without having any variables x or y.

If I can find out the value which turns out to be,

$$F = \prod_{i}^{N} g_i h_i = \frac{4}{3}\frac{3x}{8}\ \frac{5}{3}\frac{2y}{x}\ \frac{5}{3}\frac{45}{y} = 125$$

The individual stage efforts which will be,

$$F_i = F^{1/3} = 5$$

We are estimating the individual stage efforts for the minimum delay. If I have the individual stage efforts, the best stage efforts for the minimum delay I can now find out what are the variables x and y.

What are the gate sizes x and y, the optimum x and y values that we will get the minimum delay,

$$g_1 h_1 = 5 = g_2 h_2 = g_3 h_3$$

What it could have is all the individual stage efforts will be equal to the value 5. In that way if I calculate this particular value I should be able to find out what is y, y = 15 and similarly once I have the y value I should be able to find out what is the x value, x = 10, a y of 15 and an x of 10 in that particular three stage circuit we will notice that is going to achieve the minimum delay.

What is the minimum delay we can find out using this particular formula expression which is nothing but

$$\text{delay} = \sum p_i + NF^{1/N}$$

$$= (2 + 3 + 2) + 3(5) = 22$$

The lowest minimum delay we have calculated is 22 and this does not need the values of x and y. We actually need the path effort which is the F here, we actually need this particular value if we know this particular value without the variables x and y then we should be able to estimate the minimum delay.

For the minimum delay calculations if I know the input stage what is the gate size and then the output load capacitance, I should be able to find out the minimum delay without even calculating the variables x and y values. The x and y values we can estimate it and turns out to be 15 and 10 for achieving the minimum delay, hope this is clear.

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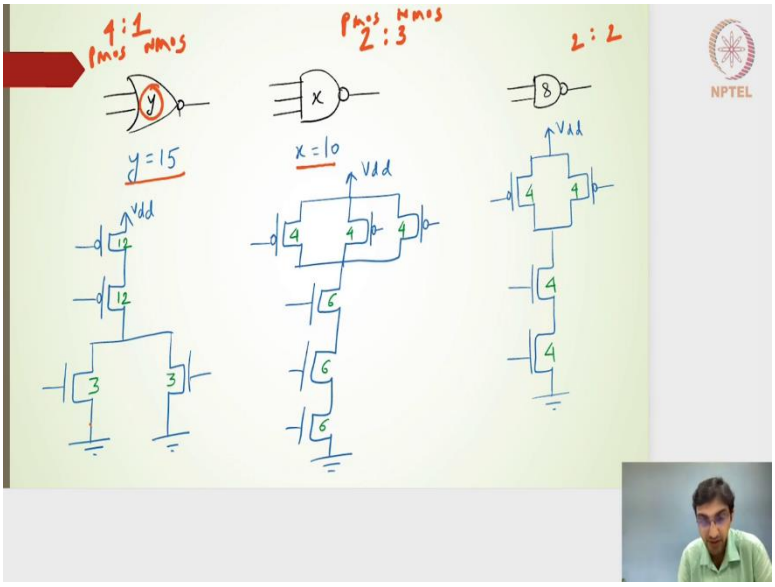

If I know the values of x and y, x =10, y = 15 and then the first stage is nothing but 8. In that case if the first stage is 8 what should be its transistor width? For a 2-input NAND gate we know that the size of the PMOS and NMOS should be nothing but two is to two. That is the gate size of 8 we will divide it equally into two parts make it 4 and 4, 4 will go to the PMOS side and then 4 will go to the NMOS side.

Both the inputs for this particular gate are symmetric, that means that both the inputs are seeing the same capacitance. Both the transistors on the PMOS and both the transistors on

the NMOS we will see the same width of 4. For a three input NAND gate the x value turns out to be 10 and remember for a three input NAND gate we have the size of two is to three on the PMOS side, we have the size of 2 for a 3-input NAND gate and on the NMOS side we have the size of 3.

What we will do is, whatever is the x value we have attained or we have achieved we will divide it into five parts, three parts of that will go to the three of that parts. 3/5 of the x value will go into the NMOS side and 2/5 of the x value will go into the PMOS side. We will get 4 and 6 on the PMOS and NMOS respectively.

If we have the value of y = 15 for a 2-input NOR gate, remember that for a 2-input NOR gate I should have four is to one ratio. The 4 being for the PMOS and 1 being for the NMOS. I will have, I will make it into five parts. 4/5 multiplied by whatever is the y value should be given to the PMOS side which turns out to be 12 and 1/5 of the y value will go towards the NMOS which turns out to be 3. Hope, this is clear.

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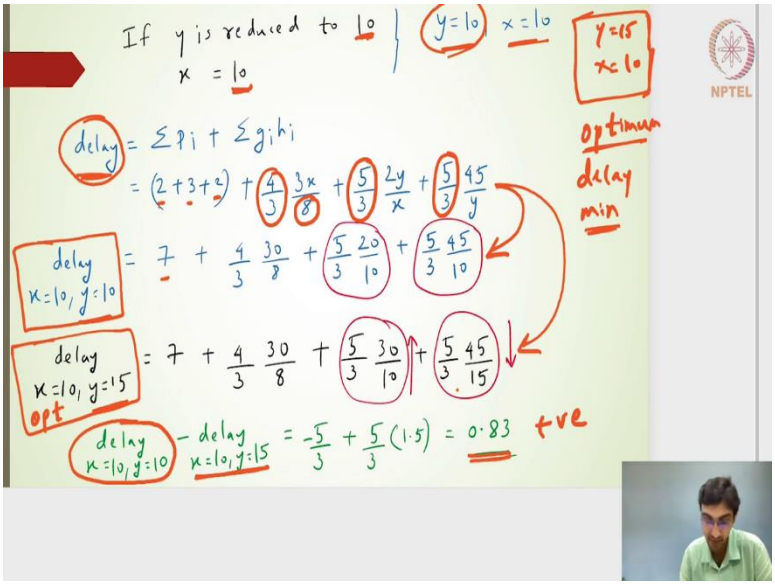

Moving forward, just for the curiosity if my y = 15 and x = 10, we are saying that this is the optimum value, that means that my delay is minimum giving optimum value of y and x is giving me the minimum delay.

What if my y value is reduced to 10. Let us pick a y value and just for a simpler calculation I am just picking a value of 10 one can pick any value like y =12 or y = 20 or whatever

just for a simple calculation I have just reduced the value of 10x, I have written it as 10. Now, for y = 10 and x = 10 what is the delay, with our claim we are saying that y = 15 and x = 10 is going to achieve with the minimum delay. Just to verify that our claim of optimum gate sizes is going to give me a minimum delay I am going to verify it using a different y values using a different gate sizes, what happens?

If I have a different gate sizes let us try to calculate the delay from our expression of pi and then the $g_i h_i$. The normalized parasitic values does not change with respect to the gate sizes, it will remain the same, the first one is the 2-input NAND gate the second one is a three input NAND gate and then the last one is nothing but the 2-input NOR gate. I will have the parasitic normalized parasitic as 2+3+2 which is nothing but 7. In fact, the 7 value will remain constant even if I change for a different x or a different y values.

$$\text{delay} = \sum p_i + \sum g_i h_i$$

$$= (2 + 3 + 2) + \frac{4}{3}\frac{3x}{8} + \frac{5}{3}\frac{2y}{x} + \frac{5}{3}\frac{45}{y}$$

$$\text{delay}_{x=10,y=10} = 7 + \frac{4}{3}\frac{30}{8} + \frac{5}{3}\frac{20}{10} + \frac{5}{3}\frac{45}{10}$$

$$\text{delay}_{x=10,y=15} = 7 + \frac{4}{3}\frac{30}{8} + \frac{5}{3}\frac{20}{10} + \frac{5}{3}\frac{45}{15}$$

I have calculated the delay or I have expressed the delay using this delay function using this particular delay function in terms of x and y. I plugged in the value of x and y and then try to evaluate the expression.

In this particular x = 10 and y = 10. So, y =10. I put in here x = 10 and then y = 10 here and x = 10 here, this is what I will get and then in this particular expression I have put x = 10 and y = 15 which we are claiming it is the optimum size giving the minimum delay.

I have rewritten that particular expression, but it is the same expression here, but the values of x = 10 and y = 15 and this particular is nothing but the same expression here by substituting the value of x = 10 and y = 10, if I calculated delay value for x = 10 and y = 10 and delay of x = 10 and y = 15, if I do the difference here turns out to be positive.

This difference is positive what it means is x = 10 and y = 10 size the gate sizes are giving me a delay more than the size that we had got the delay for x = 10 and y = 15. Y = 15 and x = 10 which we were claiming that is an optimum size, which we were claiming that that is the minimum delay it turns out to be true if I use a different gate size. If I use y = 10, it turns out to be giving a slightly more delay.

Hope you have understood this.

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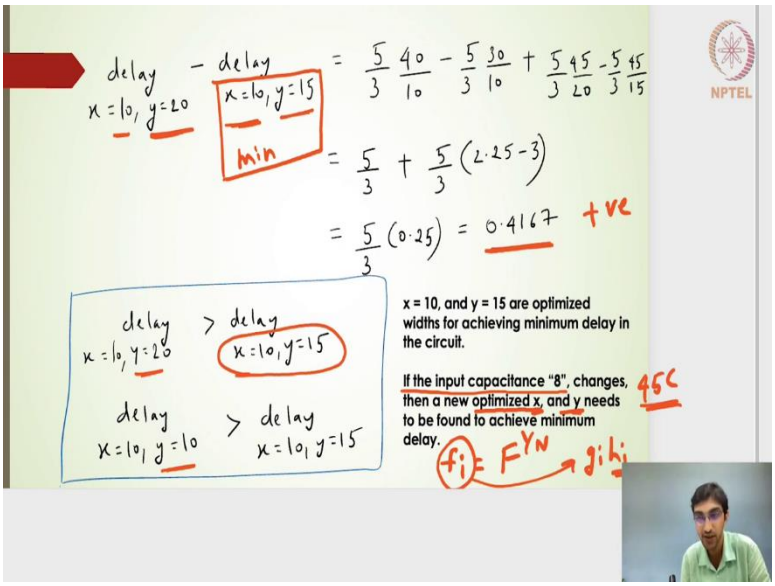

What if I use a y = 20 value. In the last case we had taken y = 10 that is the first case; the second case I am going to take a higher value of y keeping the x as same as 10, it turns out that even if I have a y = 20 here it is a positive difference, that means the y = 20 and x = 10 is going to give me a delay which is more than y = 15 and x = 10.

In that case it is positive and thereby my delay is optimum or minimum for x = 10 and y = 15 for any other values of x or any other values of y it turns out that the delay is more, that is what we have tried to verify it. We had started if the individual stages sees the same effort delay then we are likely to get then we are going to get the minimum delay the minimum summation of all the stage efforts and that is going to give me or lead to the minimum delay.

Here by taking a different sizes we have identified that if I use a different size than that of whatever we have calculated for the optimum sizes then we are going to get a delay which

is more than what we should obtain. For summarizing this for a different y my delay is actually more than what we achieve for an optimum size of x = 10 and y =15.

There is a small note here saying that if the input gate of 8 changes or the load of 45C changes then I have to reevaluate the x and y value. I have to reevaluate the new or re evaluate the optimum x and y value. If I have the 8 value changed the input to 2-input NAND gate which is now having a gate size of 8, if it is change to some other value and then the load capacitance of what if I see that is going to be different now.

Then my x and y value which was set as 10 and 15 that has to be different to give us the new minimum delay, because if 45 and 8 changes the f value is going to change and $F^{1/N}$ is going to change which is going to give me the individual stage efforts, this individual stage efforts is going to have a different $g_i h_i$. My x value and y value which defines the h_i value is going to change.