Design and Analysis of VLSI Subsystems
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Lecture - 25
Elmore delay

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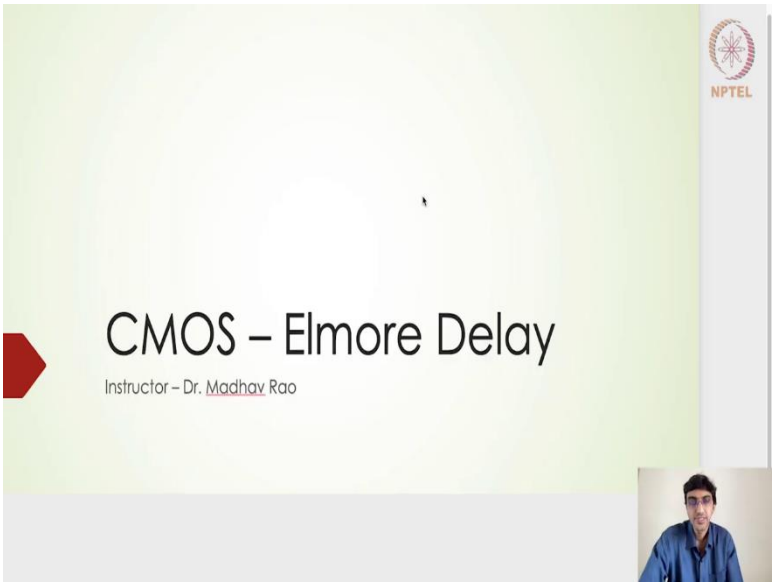

Hello students, welcome to this particular lecture on Elmore Delay. In this particular lecture we will look into one particular model of delay that is called as an Elmore delay model. We will arrive at the estimating the delay of second order circuits using an Elmore delay. We will be deriving the expressions that has been used for the Elmore delay method.

One of the reasons for having this particular Elmore delay method is to make use of this model for a higher order RC circuit and this RC circuits are nothing but it is a model switching resistance and then the parasitic capacitances that has been modeled from the transistor-based circuits.

If I am looking at a very higher order digital circuits, looking at the higher order digital circuits we will then approximate into an higher order equivalent switching resistance and in the capacitance model. Applying the Elmore delay method on this higher order RC circuit should be able to give us the propagation delay, falling or rising or even the contamination delay falling or rising.

To obtain those values, we use this particular Elmore delay method are turns out that the Elmore delay method is kind of a non-linear model, but it is very very effective and it is very very handy, handy to use or rather it could be very easy to use as well. Let us draw a 3 input or a 2 input NOR gate.

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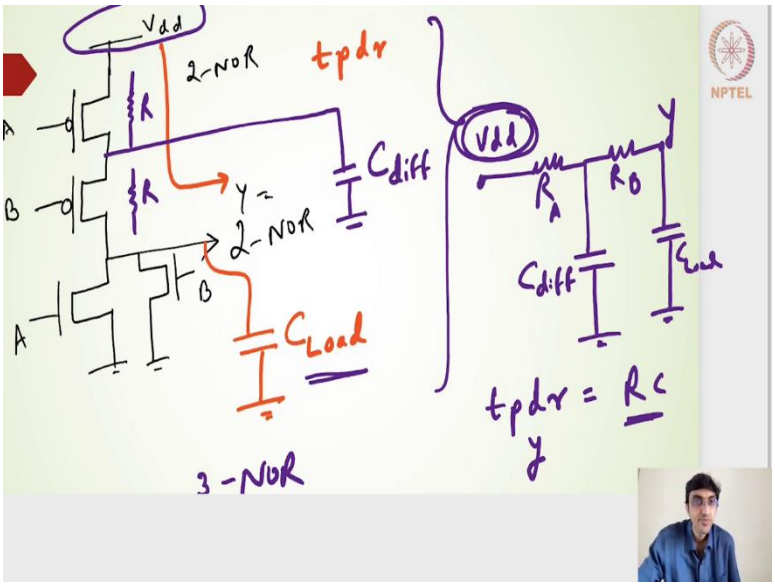

Let me draw a very simple one a 2 input NOR gate. I am going to draw on the PMOS side. This is a 2 input NOR gate connected to the V_{dd} source and this is a PMOS transistor and then this is my NMOS transistor.

That is output and here I have the pull down circuit, I have the NMOS transistors this is my A and B and then this is my subsequent A and B on the pull up side, this is a 2 input NOR gate.

Let us say that I have the switching resistance also estimated for each of this transistor assuming that the widths and then the lengths of the transistors are the same on the PMOS and NMOS side. Let us say that I have this is nothing but an equivalent resistance of R and if I want to find out what do you say the propagation delay of the rising.

If I want to find out the propagation delay rising for the circuit, I need to have the capacitance I know at the output node I will have some kind of an equivalent capacitance. I am just going to write it as C_{load} for time being we will be able to estimate it the exact

value of the capacitance at the output node when once we learn the diffusion capacitances and then we will also have some kind of a capacitances here.

I am going to draw that some kind of a capacitances at this particular node. I am going to write it as C_{diff}. What we have is a source node here V_{dd} and then a switching resistance of the PMOS transistor A and then connected to the C_{diff} capacitance.

Then we will have one more switching resistance of the transistor B and then we will have the load capacitance $_{load}$ capacitance or the C output capacitance, it is basically a two order circuit. If I want to draw it in terms of RC circuit it will be in this form V_{dd} and then I have the R_A PMOS transistor and then I will have the capacitance here, I am going to write it as C diffusion and then I am going to have this R_B side and then we will have the C_{load} capacitance or the C output capacitance.

This is my output node Y and then this is my the source power supply V_{dd}. In this case if I want to find out the propagation delay rising tpdr rising, for the output node y it becomes a two or second order RC circuit. It is an RC circuit, but it is a cascaded RC circuit or a second order RC circuit.

If I have a 3 input NOR gate, in fact for calculating the propagation delay rising, I will have a third order RC circuit, one more RC network will get cascaded. I will have $R_A C_{diff}$ $R_B C_{diff}$ and then RC along with the C_{load} or the output capacitance so on. If I want to find out the N input NOR gate rising delay I will have N such ordered RC circuits.

In the other way on the pull down side if I want to find out the propagation delay falling for a 2 input NAND gate, again instead of the V_{dd} we will have the sourcing the node or the sinking node will be the ground.

Instead of this V_{dd} we will have the ground and then the capacitances will be discharging. The C_{load} will be discharging through the two of the transistors A and B because on a 2 input NAND gate we will have on the pull down side, the transistors A and B will be in series and on the pull up side we will have the A and B transistors to be in parallel.

In a digital circuits, if I want to find out an equivalent the propagation delay falling or rising for a higher order digital circuits, then we need some method which will be able to simplify our higher order RC circuits. Because RC circuit is actually coming from

simplifying or approximating our transistors into an switching resistance and then the capacitance, anyways we are going to do that. Ultimately, we will have a much higher order RC circuits, and we need to find out a method which will help us in establishing the delay for this higher order RC circuits and Elmore delay is one such method.

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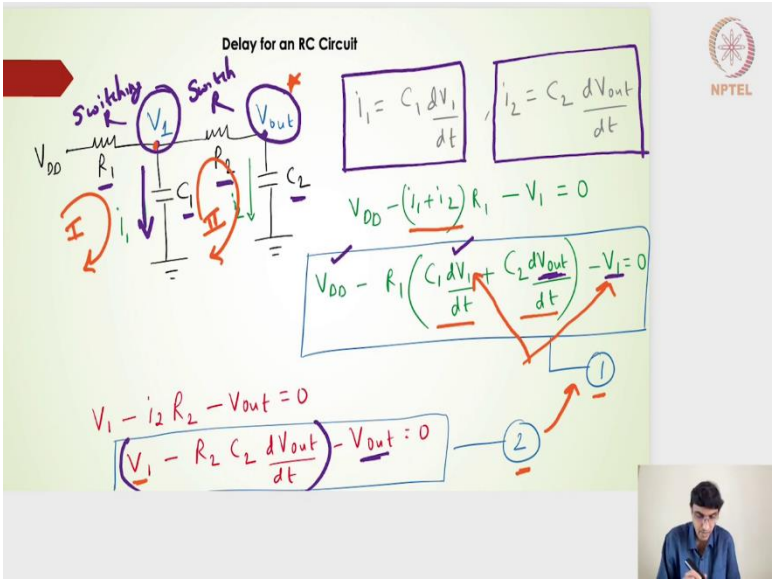

Moving ahead. I have taken a very simple second order RC circuit. I have R_1 and C_1. R_1 here and then C_1 again cascaded it to R_2 and C_2 and we need to find out the delay of the RC circuit. I have two nodes one is the output node here V_{out} another one at this point of time I am going to call it as V_1, there are two nodes V_1 and V_{out}.

I know this current i_1 which is flowing across this capacitance C_1 will be nothing but,

$$i_1 = C_1 \frac{dV_1}{dt}$$

This is my charging current, again we can consider this R_1, C_1, R_2, C_2 as nothing but an approximated RC equivalence circuit coming from the 2 input NOR gate.

I have my this current i_1 and I will have my current i_2, which is flowing along this branch of C_2 can be considered as,

$$i_2 = C_2 \frac{dV_{out}}{dt}$$

This is again a capacitor charging current equation. Now, what we really want is to find out an expression for V_{out} at this point of time and similarly once we will be able to identify the V_{out} expression we should be able to find out what is the expression for V_1.

What we had seen in an inverter circuit V_{out} initially it was a linear and then exponential. Similarly, V_1 or rather the output of the inverter circuit we has a linear and an exponential model and then from there we were able to find out what is the propagation delay falling.

For an inverter also what we did was we calculated the switching resistance and then the capacitance and now we are stating that whatever is the load capacitance seen at the output current multiplied by the switching resistance will be my propagation delay.

Assuming this R_2 and R_1 are my switching resistances, these are nothing but the switching resistances coming from the transistors switching resistances. Here also this is nothing but the switching resistance R_1 and R_2. C_1 and C_2 are coming from the whatever is the capacitances seen at the node V_1 and seen at the node V_{out}.

C_2 can also be considered as the parasitic capacitances, or the depletion capacitances, or the diffusion capacitances of those particular transistors as well as the wire capacitances as well as the input capacitances coming from the next stage.

If the there are two stages one stage cascaded to another stage, the output node we will have an equivalent or the sum of all the capacitances will be nothing but the diffusion depletion capacitance plus the wire capacitances plus the input capacitances coming from the second stage, that is about the C_1 and C_2.

What I am going to do is we want to find out the solutions of V_{out} and V_1. In that case we will try to apply some KVL method. One KVL we will apply it in this particular branch and another KVL we will apply it in this particular branch. This with the 1st KVL is this,

$$V_{dd} - (i_1 + i_2)R_1 - V_1 = 0$$

$$V_{dd} - R_1\left(C_1 \frac{dV_1}{dt} + C_2 \frac{dV_{out}}{dt}\right) - V_1 = 0 \qquad (1)$$

I have this one particular equation coming from the KVL loop of one. On the 2nd one on the 2nd KVL loop here we will get,

$$V_1 - i_2 R_2 - V_{out} = 0$$

$$V_1 - R_2 C_2 \frac{dV_{out}}{dt} - V_{out} = 0 \qquad (2)$$

Let me minimize this, I will have perfectly ordered maybe little bit more and I think this is perfect. Moving ahead I have two KVL equations. Let us go back what we want is basically a solution of V_{out} at this point of time.

If I can somehow have this either of one or two equations only in terms of V_{out}. It could be first order differential of V_{out} it could be second order differential of V_{out} also. But there should not be any V_1 terms among this 1 and 2 equation, what we are going to do is substitute 2 in 1. Put this in here and we want to erase out V_1.

$$V_{dd} - R_1 C_1 \left[\frac{dV_{out}}{dt} + R_2 C_2 \frac{dV_{out}^2}{dt^2}\right] - R_1 C_2 \frac{dV_{out}}{dt} = V_{out} + R_2 C_2 \frac{dV_{out}}{dt}$$

That I will have an all the first equation of the first KVL loop derived equation everything in terms of the V_{out}.

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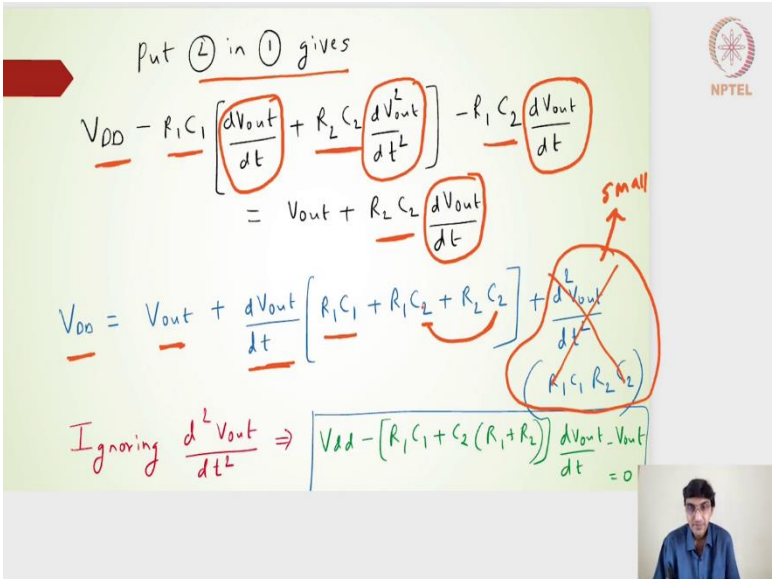

If I look closely into this I will have a constant value and I have this dVout by dt on the left hand side common,

$$V_{dd} = V_{out} + \frac{dV_{out}}{dt}[R_1C_1 + R_1C_2 + R_2C_2] + \frac{dV_{out}^2}{dt^2}(R_1C_1R_2C_2)$$

This particular term we are going to neglect it, saying that the second order differential with respect to time is going to give me a very very small magnitude value and that is something we are going to ignore.

This assumption we are going to ignore this and this assumption we are making it, because as we have seen from the inverter output voltage profile it is going to be linear profile and then it is going to be gradually going towards the exponential profile.

$$V_{dd} - \frac{dV_{out}}{dt}[R_1C_1 + R_1C_2 + R_2C_2] - V_{out} = 0$$

If I consider a decreasing linear profile or increasing linear profile in this particular case for the charging for the rising time. The increasing linear profile if I do a first order differentiation it will be a constant and if I do one more time of a differentiation it will be a 0.

If it is a linear profile or if it is an exponential profile going towards an exponential profile, we are assuming that it will be somewhere there and thereby its second order differentiation will be very very small, we are going to ignore that. Ignoring that what we get is the first order differential V_{out} term and then V_{dd}.

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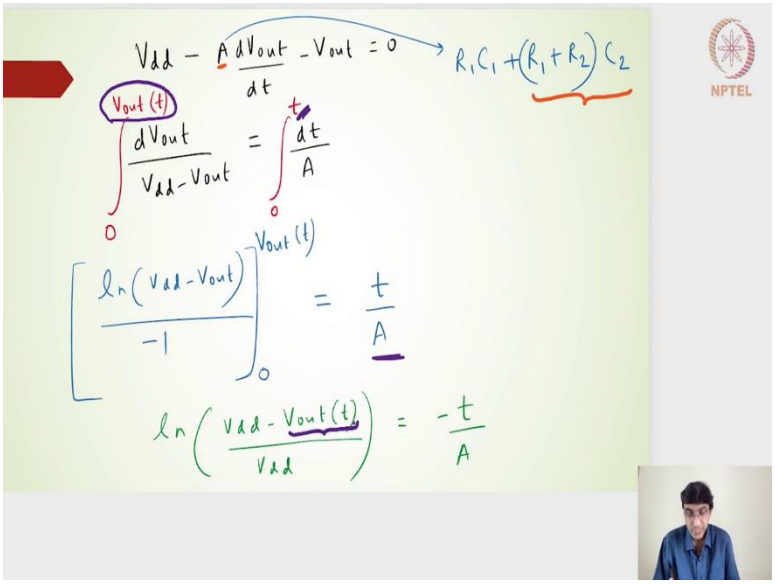

$$V_{dd} - A\frac{dV_{out}}{dt} - V_{out} = 0$$

Where, $A = R_1C_1 + (R_1 + R_2)C_2$

Let me go back a bit just to identify this particular expression, which is kind of very very important. I have R_1C_1 and then this C_2 if I get it common I will make $(R_1 + R_2)C_2$ in brackets very very important at this point of time.

Moving ahead, I have this particular equation and then this particular equation we have anyway seen in the capacitor charging profile.

$$\int_0^{V_{out}(t)} \frac{dV_{out}}{V_{dd} - V_{out}} = \int_0^t \frac{dt}{A}$$

We are interested in finding out what is the $V_{out}(t)$. Then if I solve this particular integral I will get the solution of this particular integral on the left hand side will be nothing but,

$$\left[\frac{\ln\left(V_{dd} - V_{out}(t)\right)}{-1}\right]_0^{V_{out}(t)} = \frac{t}{A}$$

Further resolving this,

$$\frac{\ln (V_{dd} - V_{out}(t))}{V_{dd}} = \frac{-t}{A}$$

Eventually I should be able to find out what is $V_{out}(t)$.

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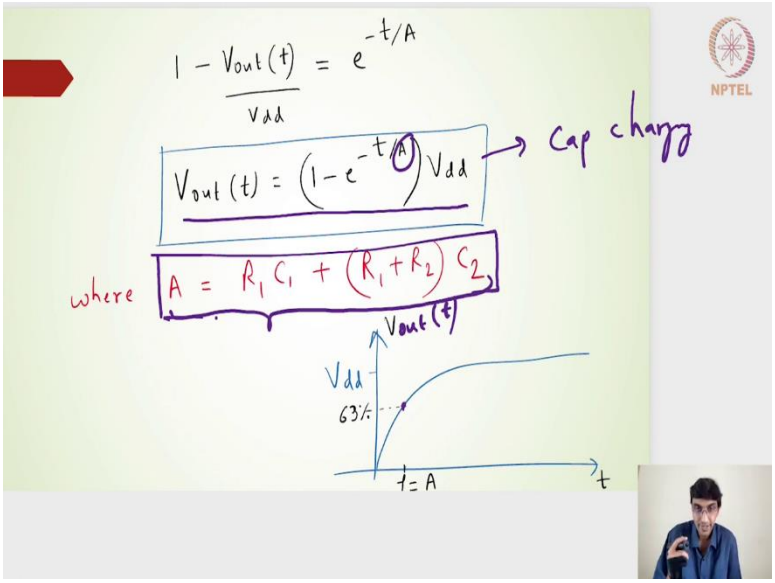

$$1 - \frac{V_{out}(t)}{V_{dd}} = e^{-t/A}$$

$$V_{out}(t) = (1 - e^{-t/A})V_{dd}$$

$V_{out}(t)$ is nothing but our capacitor charging current equation, charging voltage profile equations. This expression is very very similar to our capacitor charging.

Consider this A value that is coming from that constant $A = R_1C_1 + (R_1 + R_2)C_2$, this is what the profile I have drawn here. The V_{out} profile I should have written $V_{out}(t)$ with respect to t and at 63 percent it is a τ, which will be nothing but my A. Again, this second order $\frac{dV_{out}^2}{dt^2}$ is something we have ignored and then we got this approximated capacitor charging profile, which turns out to be very very close to our if I consider the R_1C_1 and R_2C_2 and put some values in R_1 and $C_1$and R_2 and C_2 and find out the output voltage, this comes out to be even if I consider the second order differential.

If the spice considers that and then if I find out the V_{out} with respect to time either in a multisim or in a in an Ltspice I will get close to this particular voltage profile. Ignoring the

second order output voltage is giving us a very close value. Although not accurate value, but it is a very very approximate value, in that sense we are good. This is what we get and if I look into the input side and then given to a circuit and then taking the output.

What we have analyzed is, for an inverter circuit it will be RC and that will give me the propagation delay to be very very conservative assuming that the input side is a step, its not a step input it will be some kind of a ramp input then at a conservative approach. We are saying at the output side $t_{pdf} = t_{pdr} = RC$ that is what we will come to. This time constant also it looks like a time constant.

This becomes our delay parameters assuming that the input to the 2 input NOR gate is not a step input it will be a ramp then this becomes my rising propagation delay rising for the 2 input NOR gate.

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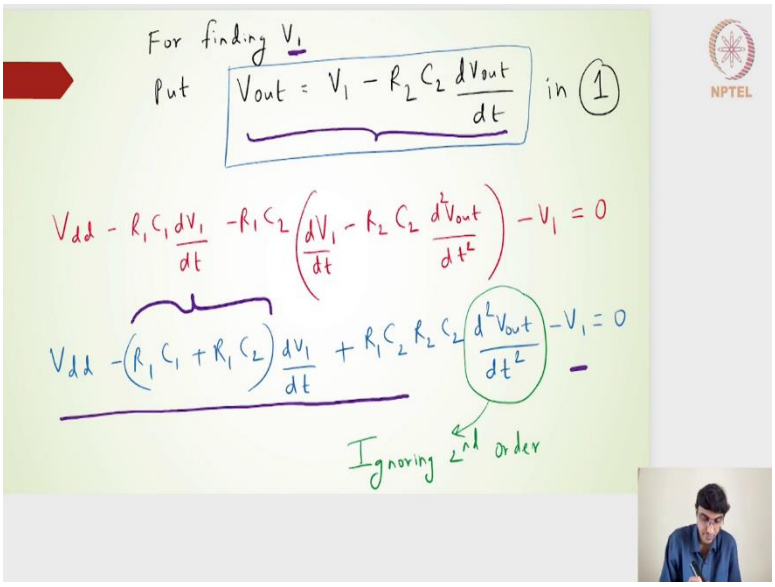

Now, what we are interested is there were two nodes V_1 and V_{out}. We are also interested in finding out the V_1 and I have two KVL equations written down. What we want is basically from those two KVL equations we want all the terms in V_1. Whether it would be $\frac{dV_1}{dt}$, that is also fine V_1 and then constant that is also fine, but what we do not want is anything V_{out}. If I go back to this particular starting equations.

I have these two equations, what we want is everything in terms of V_1, because we have anyways calculated the solution for V_{out}. Similarly, we want to derive an expression for

V_1. I have this in the first equation, I have this V_1, this particular term to be $\frac{dV_1}{dt}$ and then this is anyways a constant value. I need to replace this V_{out} term. Second equation gives me V_{out} in terms of $\frac{dV_{out}}{dt}$ and then V_1.

If I put this 2 in 1 here, I will get this differential of this V_{out}. I have to do a differential of this particular terms. I will get a second order differential of $\frac{dV_{out}}{dt}$ square and then I will anyways get a single order differential of V_1 and then second order differential of V_{out} anyways we are going to ignore it. That is the same thing which we have done in the last solution while we were trying to find the solution of V_{out}.

Similarly for finding the solution of V_1 are going to ignore the second order differential of V_{out}. Moving ahead, we were somewhere here finding the V_1,

Put this is $V_{out} = V_1 - R_2C_2\frac{dV_{out}}{dt}$ into a 1.

$$V_{dd} - R_1C_1\frac{dV_1}{dt} - R_1C_2\left(\frac{dV_1}{dt} - R_2C_2\frac{dV_{out}^2}{dt^2}\right) - V_1 = 0$$

$$V_{dd} - (R_1C_1 + R_1C_2)\frac{dV_1}{dt} + R_1C_2R_2C_2R_2C_2\frac{dV_{out}^2}{dt^2} - V_1 = 0$$

Then ignoring the second order differential.

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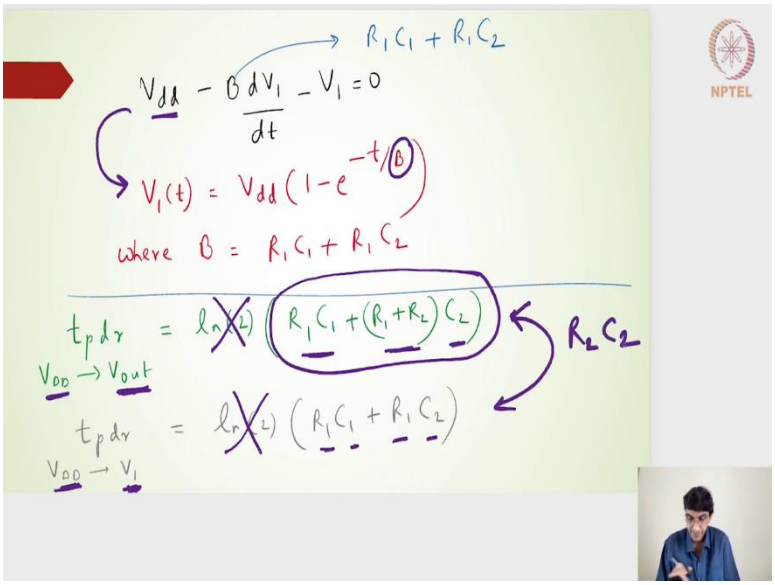

Finally, we will get,

$$V_{dd} - B\frac{dV_1}{dt} + -V_1 = 0$$

Where $B = (R_1C_1 + R_1C_2)$

Everything is in terms of $V_1(t)$ and this V_{dd} is anyways a constant.

$$V_1(t) = V_{dd}(1 - e^{-t/B})$$

Again, I mean, how do we get arrive into this particular expression to this particular solution is integrating on the both sides and then putting the limits of 0 to V_1 and then 0 to t on the time side as well as on the voltage side. We should be able to get this particular expression very very similar to what we had derived for the V_{out} expression.

The propagation delay rising is,

$$t_{\substack{pdr \\ V_{dd} \to V_{out}}} = \ln(2)\,(R_1C_1 + (R_1 + R_2)C_2)$$

$$t_{\substack{pdr \\ V_{dd} \to V_1}} = \ln(2)\,(R_1C_1 + R_1C_2)$$

I am actually ignoring a log of 2 here. Log of 2 you can take it with the consideration, that the input will be a step input, but if the input is not a step input then we will take the conservative approach and they have only the sum of this products of R and C. This is what we get the propagation delay rising for the V_{out} node and then the V_1 node. Looking closely at it, I have 1 term $(R_1C_1 + (R_1 + R_2)C_2)$.

I have this term, there is one R_2C_2 is extra as compared to that of the propagation delay rising for the V_1 output node. If I compare actually these two equations what we get is, the delay for the V_{out} node to reach to the 50 percent or the halfway point of that V_{dd} is actually more, this is R_2C_2 more.

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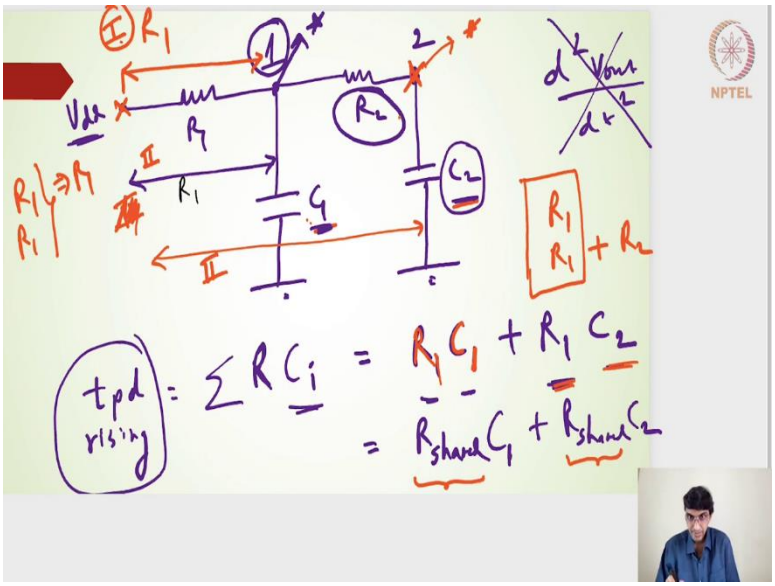

I hope you have understood this or you have analyzed that. Coming back to our original circuit of V_{dd} and then R_1 and C_1 and then I have this C_1 here and then I have this R_2 and then I have this C_2. What it says is, the propagation delay rising is nothing but the summation of R into all the node capacitances also called as the leaf capacitances.

$$t_{pd}{}_{rising} = \sum RC_i$$

The capacitances connected to the individual nodes. I am going to write it as 1 and then 2. It is nothing but the propagation delay rising or falling, in this case it is rising because the V_{dd} is connected. It will anyway is going to charge the capacitance C_1 and C_2. The rising propagation delay will be nothing but some R multiplied by this capacitance C_1 and then some R and multiplied by this capacitance C_2. It includes all the leaf capacitances, it includes all the node capacitances. Now, this particular some capacitance are here some value of capacitances is it depends on the node I am selecting.

Let us say that I am selecting a node1 here. We are interested in finding the propagation delay of the node1. The node1 achieves the 50 percent or the halfway point of the V_{dd}. What is that particular duration once it reaches the halfway point of the V_{dd}.

In that case, this is my node of interest. My propagation delay rising turns out to be from my previous second order R and C network calculation, it turns out to be $R_1 C_1 + R_1C_2$. It is very very interesting that it does not accommodate R_2 at all.

Although we know that in charging this particular capacitance C_2 it takes R_1 and R_2 path, but for approximating because we have ignored that second order $\frac{dV_{out}^2}{dt^2}$ and because of this ignoring this particular term we have actually made the second order RC circuit equivalent to a single order RC circuit and then estimated the time constraint which is nothing but a propagation delay rising.

First for our simple simplified calculation it does not account R_2 while finding the propagation delay for the output node 1, if my node of interest is 1 it does not accommodate R_2. Now, this R_1 and R_1 here if I consider the capacitances C_1 and C_2. It is also called as the shared resistance for the capacitance C_1 and of course the share resistance for the capacitance C_2, that is how the nomenclature has come.

$$t_{\substack{pd \\ rising}} = R_{share} C_1 + R_{share} C_2$$

Now, what is this shared capacitance right? The shared capacitance is nothing but a common capacitance between the two paths and what are these two paths? One path is the path from the source to that of the node of interest.

This is my path and here whatever the resistance I see I am going to write it down as R_1 that is one particular path. The other path is isolated or it is the other path is very discretized for the individual capacitances. If I am actually finding out the shared resistance for the C_1 capacitances. Then my another path is nothing but the path from the source, path from the source to that particular capacitance node.

The resistive path I need to find out for C_1 will be nothing but R_1, I will use a different color. This is my 1 path, that path is common for both the capacitances C_1 and C_2. If I want to find out the equivalent or the shared resistance for the C_1 and the shade resistance for the C_2, that particular path from the source to that particular node of interest will become same. This is my 1st path that is a skew path, the 2nd resistive path is with respect to its individual node capacitance.

For the C_1, I will have the path of R_1, for the C_2 I will have the path of $R_1 + R_2$. In that sense if I want to find out for the C_1 capacitance, for the C_1 capacitances between the two paths 1 and 2, this is my 2nd path, this is I am going to write it here.

For the C_1 capacitances there are two paths one is coming from the source to that node of interest which is R_1. I am going to take it R_1 and then the 2nd path is nothing but from the source to the leaf capacitance or the node capacitance C_1 which is R_1.

The common here the shared one, is nothing but the output of this is nothing but R_1, that is what I am going to write. This is my R_1 which is nothing but the shared resistance for the capacitance C_1 for the C_2 here first path resistive path is R_1 the second path is actually from source to the C_2 capacitance is nothing but R_1 plus R_2, the common here is nothing but R_1.

I am going to take it as R_1 here. That becomes my shared resistance for the capacitance C_2. My propagation delay rising, if my node of interest is 1 is nothing but the shared capacitances which is nothing but R_1C_1 + shared resistance C_2 which is nothing but R_1C_2. If I similarly, do it for the 2nd node of intersect, the first path for the 2nd node of intersect will be nothing but $R_1 + R_2$ for C_1 the resistive path will be R_1.

In that case my common resistance will be R_1 for C_1 capacitance, for the C_2 my resistive path is nothing but $R_1 + R_2$ because this is my node of intersect and the resistance path for the C_2 is nothing but $R_1 + R_2$, my shared resistance will be $R_1 + R_2$.

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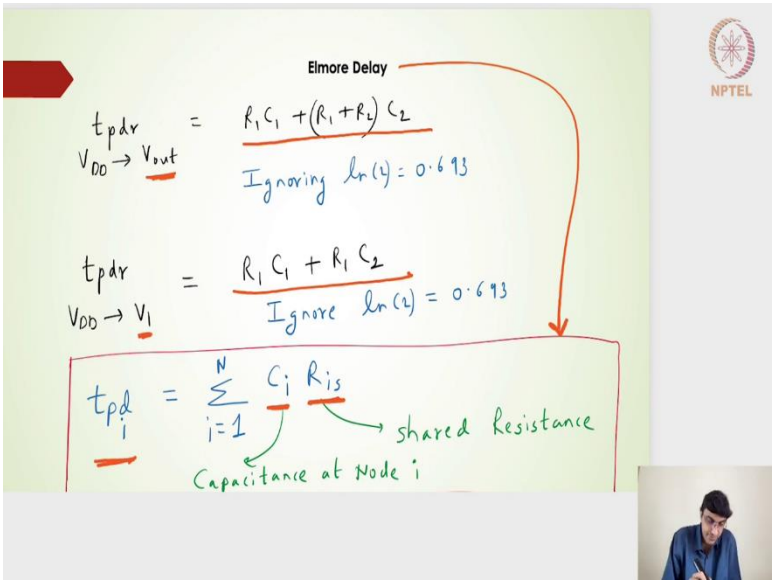

The propagation delay rising is considered as $(R_1C_1 + (R_1 + R_2)C_2)$, if I am considering the V_{out} node and then if I am considering the V_1 node, it is nothing but $(R_1C_1 + R_1C_2)$, I am ignoring this log2 that is nothing but 0.693 assuming that the input side, it is not a step input it could be a ramp input it could have some kind of an input transition

The Elmore delay method is nothing but this particular expression. The t_{pd} could be a propagation delay falling or rising is nothing but,

$$t_{pd_i} = \sum_{i=1}^{N} C_i R_{is}$$

All the capacitances at the node, I multiplied by the shared resistances for the node I and it could have N nodes. It will be from 1 to N nodes, it should include all the capacitances in that particular circuit and then multiply with that of the shared resistance seen by the individual node capacitances.

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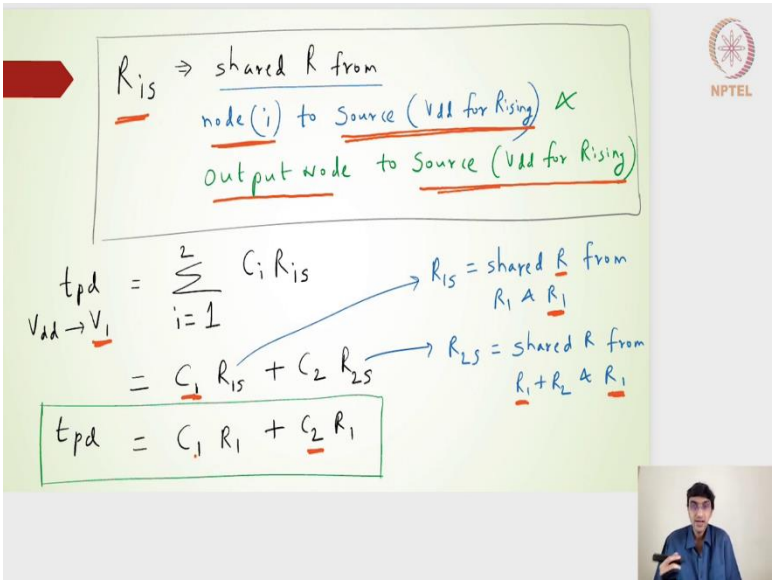

Hope this is clear. Just for a better understanding I have just written it here R_{is} is nothing but the shared resistance from the node from which the capacitance is connected to all the sources whether it is V_{dd} or ground, for V_{dd} for rising ground for falling output and then whatever node is my output node of intersect.

The output node to that particular source power supply, whether it is the V_{dd} for rising and then 0 for the ground. In the same way what I had shared in the 9th slide, the shared resistance from R shared resistance R for the node C_1, V_1 of interest will be nothing but,

$$t_{\substack{pd \\ V_{dd} \to V_1}} = \sum_{i=1}^{2} C_i R_{is}$$

$$= C_1 R_{1s} + C_2 R_{2s}$$

$$t_{pd} = C_1 R_1 + C_2 R_1$$

Then we get this propagation delay rising for the V_1 node of interest.