Design and Analysis of VLSI Subsystems
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Lecture - 24
CMOS Inverter approximated to RC Circuit

Hello students. Welcome to this lecture on inverter which is kind of approximated by an RC circuit and where R represents the switching resistance of the transistor which is operating in this particular at any point of time and C represents the capacitance seen at any of the output nodes or any kind of a diffusion nodes which is of interest to us. What we will see is that we will take an inverter circuit and then try to approximate the R and C (approximated RC) circuit and proceed further.

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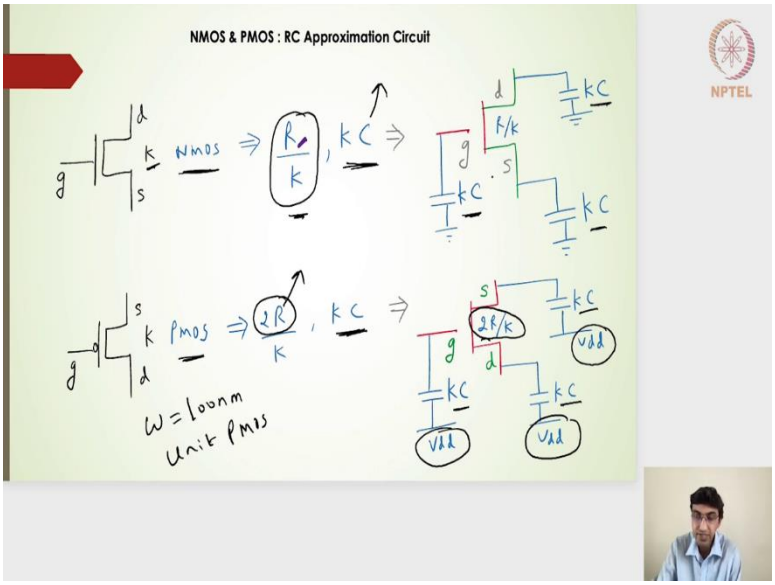

Moving on what we had seen is an NMOS transistor or a unit NMOS transistor has a unit resistance of R. This is the R and if I scale the transistor by k times then the switching resistance is going to scale down or is going to decrease by k times. Thereby the switching resistance is of the value $\frac{R}{K}$. The width of the NMOS transistor is k times the unit NMOS transistor width. The unit NMOS transistor width is anyway is 100nm which we had seen previously.

If it is k times more than that of the 100nm the capacitance will be k times into C, where C represents the unit capacitance. Now if C represents the capacitance for a unit NMOS transistor and similarly k times the width of the NMOS transistor will give me the switching resistance of $\frac{R}{K}$.. To replicate that into a transistor level, this is what we have drawn. At the gate side the capacitances will be scaled by k times diffusion and then the parasitic capacitances will be scaled by k times and the switching resistance is denoted by $\frac{R}{K}$.

For a unit PMOS is again a width of 100nm. In this case the switching resistance of a PMOS will be nothing but twice that the switching resistance of an NMOS. Again it is attributed to the lower mobility which the holes have with respect to that of the electrons.

We will have 2R, where R represents the unit NMOS switching resistance and if the PMOS transistor is scaled k times the 100nm which is the unit PMOS transistors width. Then in that case we will get $\frac{2R}{K}$. The overall switching resistance of the PMOS transistor will be scaled down by k times. The capacitance however will be scaled up by k times. KC is what we will see for the gate capacitances and as well as for the depletion and then the parasitic capacitance, that is what is represented for the PMOS structure here. The PMOS structure, the gate side you will see a kC. Note that it is connected to the V_{dd}, the gate side is at a higher potential than that of the gate and the body is actually connected to the gate, no body is connected to the V_{dd} terminal.

That is what I have written here and you can see that the capacitances are scaled up by k times kC, k C and k C. The switching resistance is anyways $\frac{2R}{K}$, this is what is denoted here. The difference here on the PMOS side as well as on the NMOS side is the switching resistance. The gate capacitances as well as the parasitic and depletion capacitances remains the same. Hope you have understood this.

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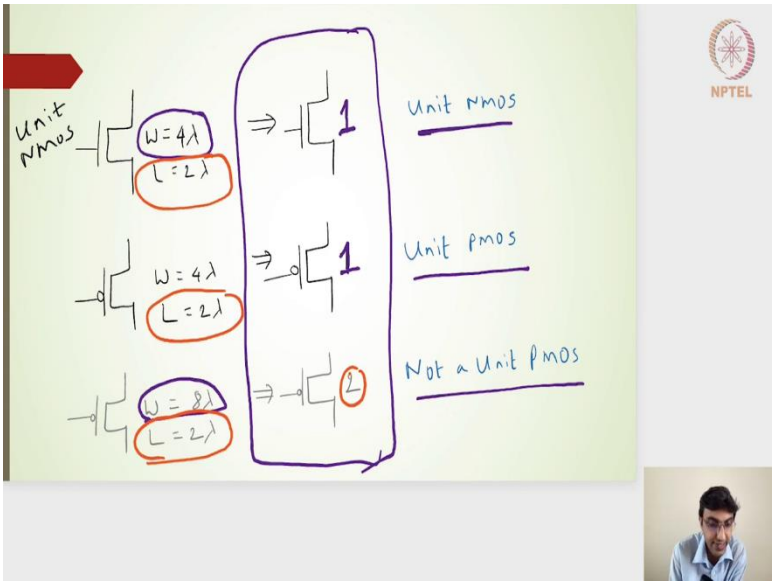

Moving further, just to summarize the unit NMOS. This is the unit NMOS, because the moment I see w is equal to the width of the NMOS transistor as 4λ where λ is equal to 25 nm, 2λ will be the channel length of the 65nm technology node which gives us 50nm of the channel length, 4λ will be 100nm. That is our unit NMOS which we write it as 1. NMOS transistor with the numbering of 1 or with the labelling of 1 represents that it is an unit NMOS.

Similarly, for the PMOS transistor width of 4λ, length of 2 λ and then denoted by a 1 here, on the transistor side is nothing but a unit PMOS. If I have a width of 8λ for the PMOS that means, I am writing a 2 here which means that the width is twice that of the unit PMOS transistor. 2 represents twice the width of the unit PMOS transistors. Then we can say that it is not a unit PMOS, the width is 2 times that of the width of the unit PMOS transistor. This is a general the naming conventions of the transistors, this particular portion. What we have seen is the actually the channel length.

The channel length in all these cases remains 2λ. We generally do not change or modify the channel length. What we change is the w parameters and then those w parameters can be represented in terms of scalar quantity here. Instead of k times I have written 2 times or I can write it as 4 times or I can write it as 10 times. What it represents it is the width is scaled 2 times or 4 times or 10 times more than that of the unit PMOS or NMOS transistors.

In most of digital design the channel length does not change. We are not going to manipulate the channel length. We are not going to scale the channel length, we are going to limit it to the lowest possible channel length which will be 50nm or 2λ for a 65nm technology node. What we are going to change and what we are going to represent the scaling is nothing but the width dimensions. Hope this is clear moving ahead.

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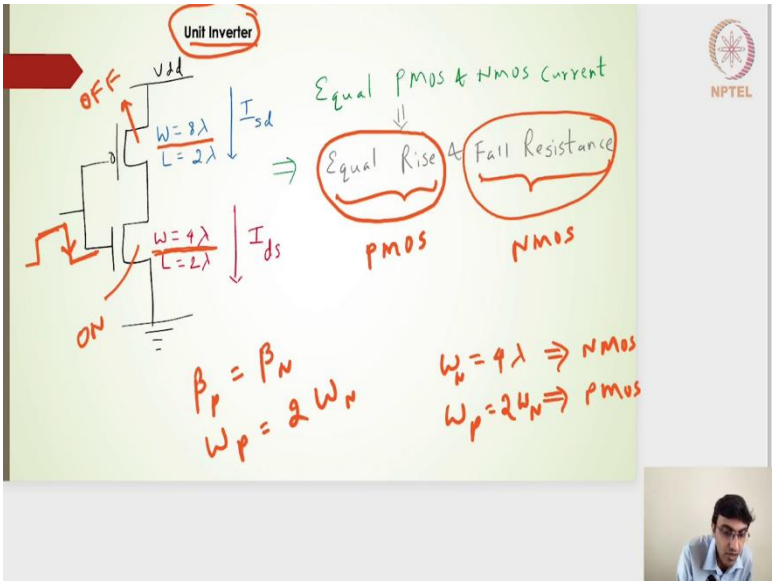

We have designed a unit inverter and what it represents is the unit inverter is the lowest transistors, the lowest PMOS dimensioned transistors, the lowest NMOS transistor dimension and where the current of the PMOS and then the current of the NMOS are equal, that is what a very brief definition is. What it really means is can I have an inverter with the lowest possible sizes of the transistors of PMOS and NMOS with the equal rising resistance and then the equal falling resistance.

If I want the equal rising and falling resistance, what it means is if I have a step input here at the input side and if it is step input I know that the NMOS transistors will be on. NMOS will be on in that case PMOS will be off. All my switching resistance or when we do the delay calculation, it is only through the NMOS current, the discharging of the capacitor takes place through the NMOS transistors current.

I will actually utilize the NMOS current I_{ds} and then calculate the propagation delay. Similarly, we have seen that the switching resistance which we calculate using the NMOS

transistor because that is the one which is operating and that is the one which is discharging the capacitor and bringing the output node voltage to 0.

That will give me the fall resistance, whatever is the current of the NMOS that will help me in establishing the fall resistance of the NMOS transistor. Similarly, if I have the step input is going back to 0, in this particular transition that the PMOS transistor will be on and the NMOS transistor will be off. In that case I will get the rising resistance because my output node is arising through a V_{dd} value, the rising resistance I can get it from the PMOS.

What we need is for defining or designing the unit inverter is the PMOS transistor should have an equal. The PMOS transistor should have a rising resistance or the switching resistance of the PMOS transistor should match with that of the NMOS transistor switching resistance.

In the long channel model we know that the resistances will match if the current matches with the maximum current or the saturation current and the linear current of the PMOS could match with that of the saturation and linear current of the NMOS. In that case we should be able to get the same resistances and that is possible only if I take the $\beta_P = \beta_N$ which means that the$W_P = 2W_N$.

What we still have the design requirement of the unit inverter is it still should be of the lowest size. The lowest possible size on the NMOS side I can get is w = 4λ that is the lowest possible dimensions I can get for the NMOS. For the PMOS, I will have the width which I need to have to be twice that of the width of the NMOS, that becomes 8λ.

The unit inverter is not made up of unit PMOS and unit NMOS. It is actually made up of unit NMOS, but the PMOS side it is twice that of the unit PMOS. The width here should be nothing but 8λ here for the PMOS, whereas the width of the NMOS is 4λ. The reason for the unit inverter is we want the equal rise and the falling resistances.

That is something you should make a note of it unit inverter is not made up of unit PMOS and unit NMOS. It is actually on the PMOS side it is twice the width that of the unit PMOS and on the NMOS side it is the unit NMOS, hope you have understood this.

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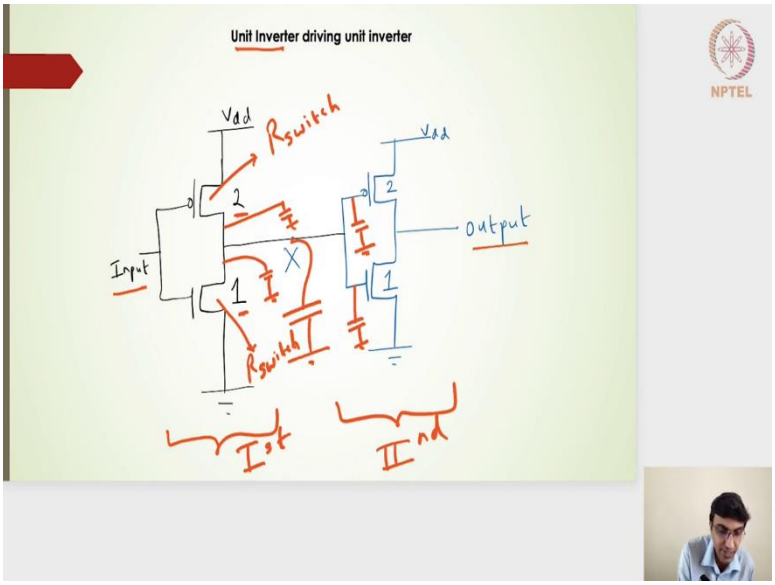

Moving ahead, what we have now is a unit inverter which can be represented as 2:1; 2:1 represents the width on the PMOS side is scaled 2 times then that of the unit PMOS. 1 represents the scaling is only 1 of that of the unit NMOS. I have now 2:1 which will give me the equal rising and falling resistance. What it really means is you will get equal amount of current on the PMOS and in the NMOS both the linear and saturation currents are of the same level.

Now if this particular unit inverter is actually driving one more unit inverter, this output x node is connected to another inverter of 2:1 and then the output is taken. I have an input provided to the first stage. This is the first stage and this one is our second stage. The input is provided to the first stage I am taking the output, output is cascaded or fed to the next stage. Then we will get the output and both the inverters are 2:1 inverters.

In this case how do I find out the propagation delay falling or whatever the rising is of course, depends on the output whether it is falling or rising. If the input is rising, I will naturally get the output to be rising because it is 2 inverter stage and if the input is falling I will naturally get the output to be falling. At this particular point when I have 2 stages cascaded it will be interesting to note what should be the overall capacitance here. We should be able to establish that because we know there will be the parasitic capacitance is coming from here and then there will be a parasitic capacitance coming from here from this particular transistors to the body and parasitic capacitance coming from the PMOS

transistors terminal to the body and then we have the capacitances on the gate side of the next stage contributing to the x node and then the capacitance on the gate side of the next stage NMOS transistor contributing to the x node.

Once I have this capacitances. Then I should be able to estimate what should be the switching resistance of this PMOS transistor and then what should be the switching resistance of the NMOS transistor. We know that the falling and then the rising resistances that is the switching resistances for a 2:1 unit inverter is nothing, but same.

If the switching resistance of an NMOS we know that in a long channel model it will be around 560 Ω. For the width of 2 times the unit PMOS, the PMOS transistor will also have the switching resistance as that of the 560Ω.

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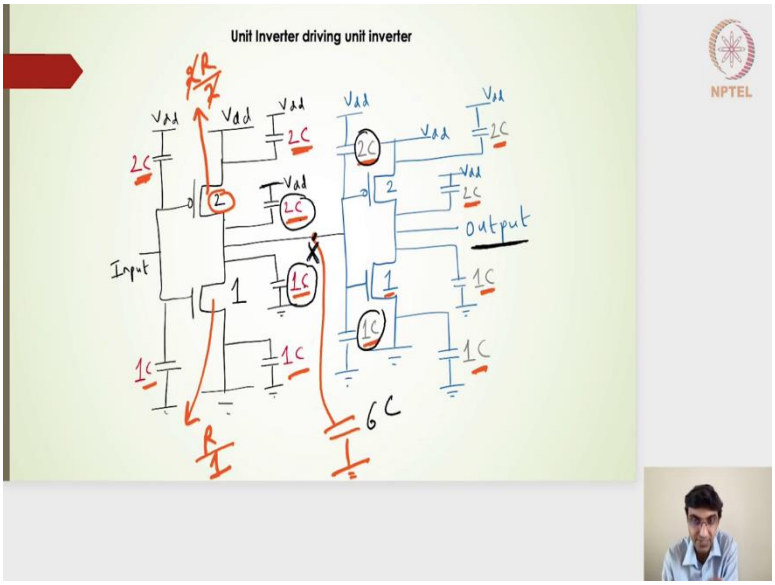

With this particular parameter, let us try to establish what should be the propagation delay. In this particular diagram although it looks very very dense it is nothing but what I have drawn in the previous slide. I have just drawn the capacitances here the capacitances are nothing but 2C. Because it is the scaling of 2 is there here on the PMOS side the scaling of 2 is there 2C and then 2C here. On the NMOS side for the first stage inverter, on the NMOS side I have a scaling of one that is why the capacitances remains 1C, 1C and then 1C.

The switching resistance for this should be R and then whatever is the scaling factor it will be 1. The switching resistance of this for the PMOS, we know that it is nothing but $\frac{2R}{K}$ which is nothing but 2. I will get same as that of R, hope this is clear. This has been cascaded to the another 2:1 inverter. I will get the scaling of 2 into the unit capacitor, unit PMOS capacitances 2C here, 2C here, again the scaling is 1 here, that means I will get 1C, 1C and on the gate side I will get 1C.

The overall capacitances that I can see on the x node will be nothing but this particular capacitance in parallel with this particular capacitance. Of course, in the AC analysis or in the transient analysis this V_{dd} we will consider it to be grounded. This will be 1C + 2C + 2C coming from the next stage inverter and then 1C also coming from the next stage NMOS gate capacitance.

I will have 2C + 1C + 2C + 1C it will be equivalent to 6C capacitance that has been seen at the output node X. Of course, it is not the output node X it is an intermediate node X, the output is still this after the second stage. I am talking about this particular output node which is an X node, which is nothing but the output after the first stage.

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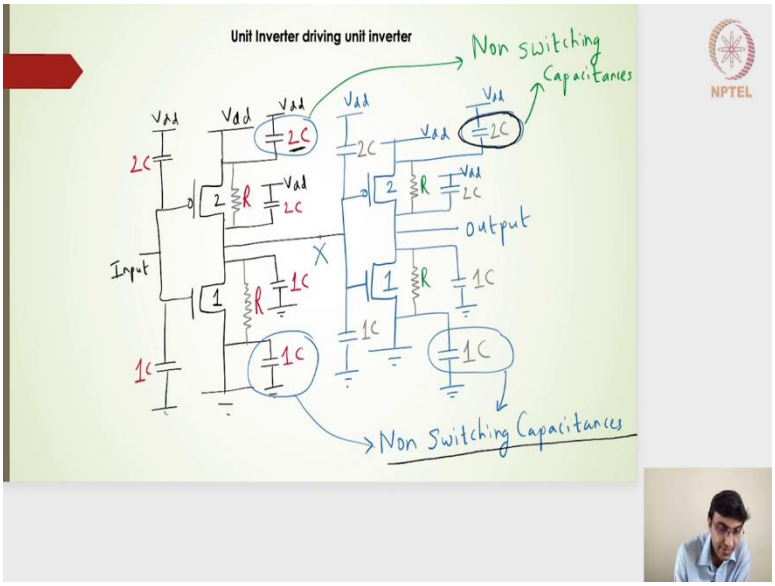

Moving ahead, I have just drawn here, this slide is very very similar to the previous slide. Just that the switching resistance I have drawn which is nothing but R and R here and R here and R here. Hope this is clear and of course, X will have a capacitance of 6C. Moving ahead this is something we are anyways aware about this particular capacitance the 2C

capacitances here and the 2C capacitances here which is having on both the terminals it is a V_{dd}.

Then similarly the 1C capacitances here and 1C capacitances here on both the terminals it is the ground. Any changes in the input side or any changes in the X output node will not have any change in the 1C and 2C capacitances here. The voltage across the 1C and 2C capacitances because on both the sides it has a fixed potential of V_{dd} or ground.

Similarly, it will have the same effect on 2C and 1C on the second stage inverter. Any change in the input X node any change in the output here will not have any effect on the 2C and 1C capacitances. Because again it is fixed to the both the 1C and 2C capacitances are fixed to the DC voltage sources the constant voltage sources, it is also called as a non-switching capacitance. That is what this slide says hope this is clear.

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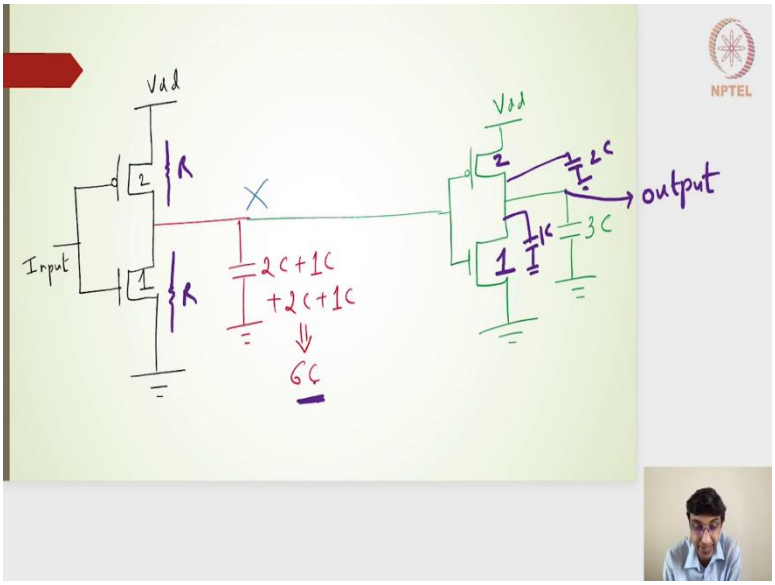

Moving ahead this is what we have 2:1 inverter the switching resistance. Let me draw this the switching resistance is nothing but R here and the overall capacitance is 6C connected to the another next stage inverter which is the output capacitance is 3C, because here it is nothing but 2:1.

I will get one capacitance 1, 2C capacitance coming from here that we have seen in the last slide and then 1, 1C capacitance coming from this particular drain 2 body of the

NMOS. Overall, on the output side I will actually get on the output side 3C, capacitance on the intermediate output X node I will get 6C capacitance.

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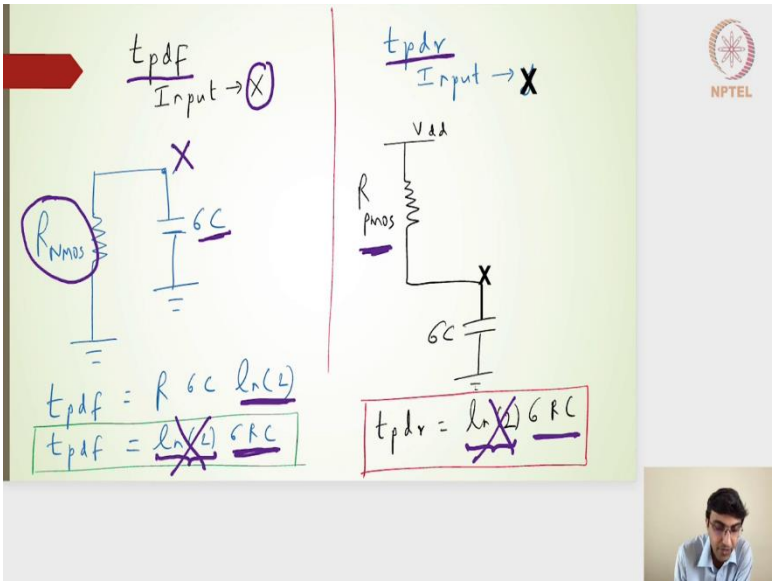

What should be the propagation delay falling from input to X node (t_{pdf} $_{input \rightarrow x}$). I am taking stage by stage. The first stage input and the first stage output is the X node, the second stage input is the X node and the second stage output is nothing but the output node. The propagation delay falling and propagation delay rising (t_{pdr} $_{input \rightarrow x}$) is what I am considering for the first stage. From input to X which is the output of the first stage what should be the propagation delay falling and similarly what should be the propagation delay rising for the input to the X node.

I have written the X node and then X node C is a capacitance of 6C and for the falling is anyways the NMOS transistor which ensures that the X node discharges to 0. For the rising it is nothing but the PMOS transistor switching resistance which makes sure that the X node is reached to the V_{dd} level and that is why I have the PMOS transistor in wherever I want the rising propagation delay. I need the switching resistance of the PMOS transistor which is connected to the V_{dd}.

Here the R switching NMOS resistance is connected to the ground.

$$t_{pdf} = R6Cln(2)$$

By neglecting ln(2),

$$t_{pdf} = 6RC$$

Similarly,

$$t_{pdr} = 6RC$$

If it is a unit, if it is a step input then I will consider the ln(2), if it is not given that, it is not a step input then I can even neglect this ln(2). I will take the conservative approach of 6RC. Hope this is clear.

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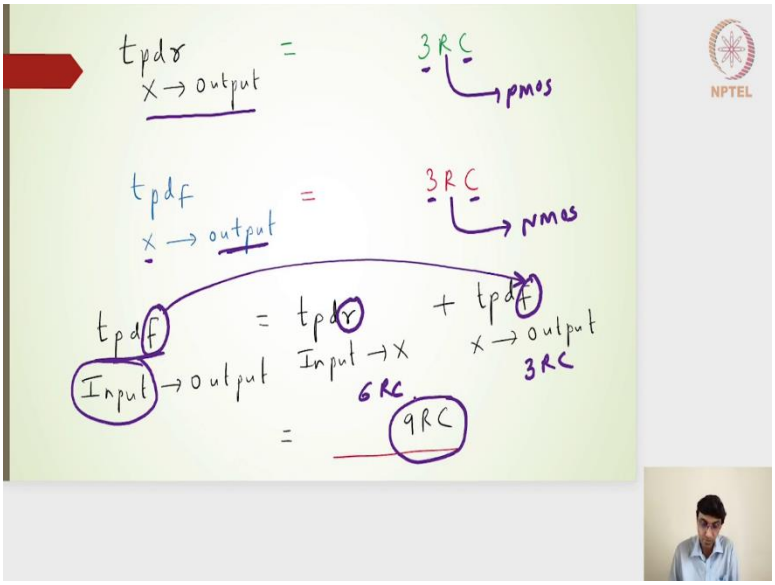

The propagation delay rising and falling for the second stage which at the output node it has only 3C, capacitance. The propagation delay rising for the second stage is,

$$t_{\substack{pdr \\ x \to output}} = 3RC$$

The switching resistance for the rising it is the switching resistance of the PMOS. PMOS it has a width of 2. That is why it is switching resistance will be R and the propagation delay falling for the second stage,

$$t_{\substack{pdf \\ x \to output}} = 3RC$$

This R is nothing but the NMOS which is having a width of 1C is a switching resistance of R. The overall propagation delay falling for input to output from and assuming that input is not a step input it may be something else, the step input is not mentioned here.

The propagation delay falling from input to output is,

$$t_{\substack{pdf \\ input \rightarrow output}} = t_{\substack{pdr \\ input \rightarrow x}} + t_{\substack{pdf \\ x \rightarrow output}} = 3RC + 6RC = 9RC$$

If I want to get the output of the second stage to be falling that means, I need to have a propagation delay falling here. Then because the second stage is an inverter the input to the second stage should be a rising input and that is why the first stage I need to calculate what should be the propagation delay rising. Because these first stage output will be rising then only the second stage inverter output will be falling, hope this is clear.

I need to find out the propagation delay rising for the first stage and then the propagation delay falling for the second stage. That is what I have written input to X node of propagation delay rising plus the propagation delay falling for the input to the output. Overall, it will be nothing but second stage will give me 3RC, the first stage it will give me 6RC. Overall, it is nothing but 9RC value very conservative approach when the input characteristics is not given when the step input is not given.