Design and Analysis of VLSI Subsystems
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Lecture - 13
Skewed Inverter and threshold voltage

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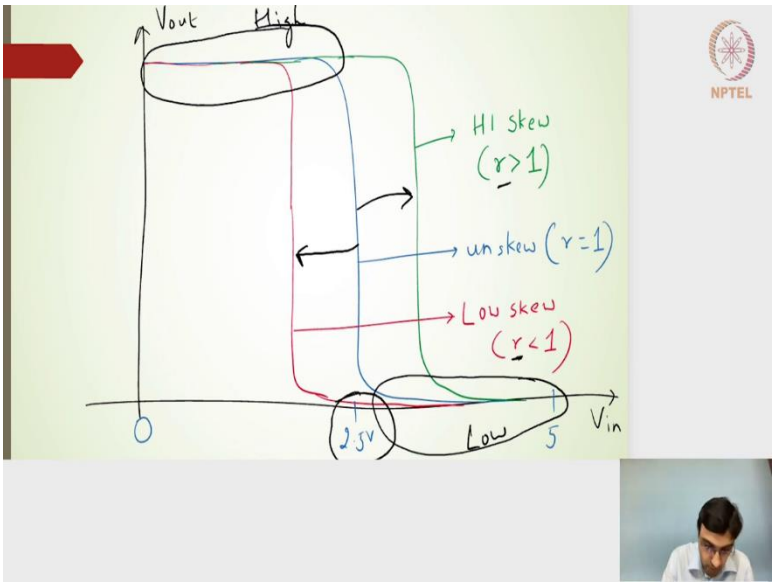

This particular slide talks about the high skew inverter. The previous example, where the skewing ratio was greater than 1, unskewed inverter where the skewing ratio was equal to 1. That means that the beta of the PMOS is equal to the beta of the NMOS. Then the low skew inverter, where the PMOS is more dominant, in the sense that the NMOS the beta is more than that of the beta of the PMOS. That is when we will get the skewing ratio to be less than 1.

If I look into this particular blue line, this is the unskewed inverter. It falls exactly on this particular input voltage of 2.5 volts. So, the threshold value of the inverter. So, we also defined something called as a threshold voltage for an inverter. Remember that the threshold voltage of the inverter is not the same as that of the V_t of the transistor. The threshold voltage of the transistors are different.

For a 65-nanometer technology, the threshold voltage is around 0.3 volts for the NMOS and PMOS transistors. Whereas the threshold voltage for an inverter is nothing but the input voltage, where we will get this particular transition region. Transition region in the

sense, the high output voltage a digital logic 1 moving on to the digital logic 0. That is what is called the transition region.

Wherever the input voltage is making this transition to happen from the high to the low voltage is what we call it as the threshold voltage of the inverter. For an unskewed inverter, the threshold voltage turns out to be 2.5 volts. For a high skew, the threshold voltage will be above 2.5 volts. For a low skew, the threshold voltage will be less than 2.5 volts.

For a low skew you have noticed that, the transfer characteristics is kind of shifted towards the left side, high skew inverter the transfer characteristics has been shifted towards the right side. In fact, the transition region has been actually moved to the right side for the high skew, for the low skew the transition region has moved to the left side. What it implies is the transition region is kind of more controlled by the transistor NMOS or PMOS whichever one is more dominant.

If the PMOS transistor is dominant, so the PMOS is going to push this transition region on the right side and the transition region is pulled to the left side if the NMOS transistor is more dominant.

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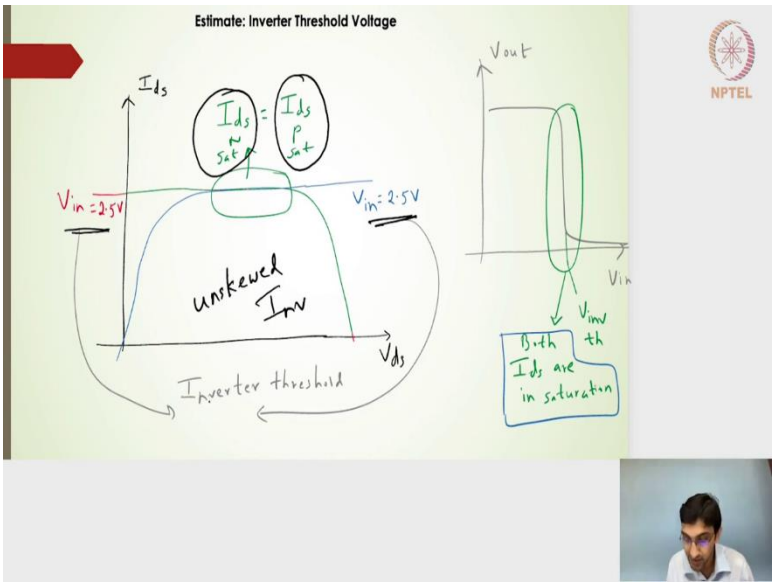

Hope you have understood this, moving ahead. Now we need to estimate this particular threshold voltage. So, can we have an expression which can define this particular threshold

voltage. Remember that the threshold voltage is actually nothing but the series of this particular points as I have drawn here.

Where both the currents are in saturation and then it is a series of intersection points. That means the current of the NMOS in saturation should match with that of the current in the PMOS transistor, where the PMOS transistor is also in the saturation. So, this series or the intersection of this points is where we get this particular transition region or we can use it to define the threshold voltage of the inverter.

Here I have drawn this particular for an unskewed inverter. This is for an unskewed inverter, where I have drawn the input voltage of 2.5 volts, where the current profile is drawn and the input voltage of 2.5 volts, where the PMOS current profile is drawn. The blue line is the NMOS current profile, the red line is the PMOS current profile, wherever they are intersecting. This particular input voltage is my inverter threshold voltage.

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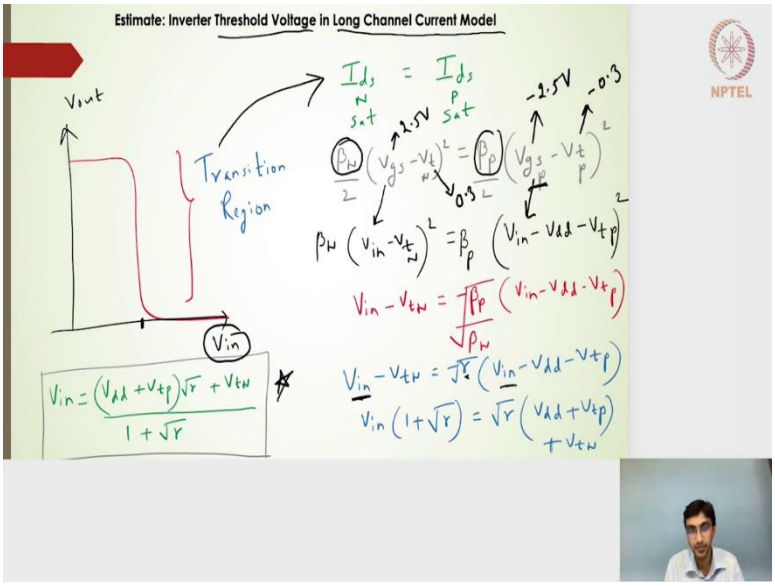

The transition region is actually defined when the NMOS current in saturation matches with that of the PMOS saturation current. If I use this particular long channel current model, the one which we have used for the ideal transistor behaviors, if I use that particular current model for the NMOS and then for the PMOS, when both of them are in saturation. Then,

$$I_{ds_{N,sat}} = I_{ds_{p,sat}}$$

$$\frac{\beta_N}{2}(V_{gs} - V_{T_N})^2 = \frac{\beta_p}{2}(V_{gs_p} - V_{t_p})^2$$

Remember that, this V_{gs_p} if input is 1 volts or rather input is 2.5 volts. let me take an unskewed inverter. This V_{gs} if it is input is 2.5 volts, PMOS will be nothing but -2.5 volts V_{T_N} is anyways 0.3 volts, V_{t_p} is nothing but -0.3 volts.

In the brackets the $V_{gs} - V_{T_N}$ is nothing but 2.2 volts the whole square; here also it is nothing but -2.2 volts the whole square. The -2.2 and then the +2.2 the whole square the levels will match, if it is an unskewed inverter, that means the $\beta_p = \beta_N$.

I am just giving a kind of a hint of why this particular expression is matching or why it is valid. Because if I pick this 2.5 volts, it is actually matching, the levels of the currents are matching. Proceeding this further, this particular expressions further, this V_{gs} of PMOS is nothing but I can write it in terms of $V_{in} - V_{dd}$, where V_{dd} is considered to be 5 volts, in this particular case -V_{tp}.

$$\beta_N(V_{in} - V_{t_N})^2 = \beta_p(V_{in} - V_{dd} - V_{t_p})^2$$

$$(V_{in} - V_{t_N})^2 = -\sqrt{\frac{\beta_p}{\beta_N}}(V_{in} - V_{dd} - V_{t_p})^2$$

Why we are writing this V_{gs} of PMOS in terms of $V_{in} - V_{dd}$ is because we want the threshold region. Inverter threshold voltage which is defined by that V_{in} point, where the translation region starts. I want to find this particular V_{in} value, whether it is 2.5 volts or above 2.5 volts or below 2.5 volts.

That is why the current expressions are actually stated or expressed in terms of V_{in} voltage. If I take square root on both the left hand side and the right hand side, I will get this particular expression,

$$V_{in} - V_{t_N} = -\sqrt{r}(V_{in} - V_{dd} - V_{t_p})$$

Remember that if I am taking the square root, I will get actually two solutions + and -, the + solution does not work, so that is why we have preferred or we have taken the - solution. You can actually do the +, $V_{in} - V_{t_N} = \sqrt{\frac{\beta_p}{\beta_N}}(V_{in} - V_{dd} - V_{t_p})$. You will get a solution, it will be out of the region. You will get a solution something like V_{in} is above V_{dd} or less than 0 volts. So, which is not possible V_{in} should be between 0 and V_{dd}.

That is why we have taken the - sign. The minus sign if I take this, $\frac{\beta_p}{\beta_N}$ can be expressed in terms of the skewing ratio r here. So, V_{in} here, V_{in} this, V_{in} take it on to the left hand side, I will get this particular expression,

$$V_{in}(1 + \sqrt{r}) = \sqrt{r}(V_{dd} + V_{t_p} + V_{t_N})$$

If I am taking this V_{in} want to express what should be V_{in}. This $1 + \sqrt{r}$ should be taken into the denominator side and this is what I will get. The expression for finding the threshold voltage in terms of the skewing ratio for the long channel current model is given by this particular expression.

$$V_{in} = \frac{\left(V_{dd} + V_{t_p}\right)\sqrt{r} + V_{t_N}}{1 + \sqrt{r}}$$

Hope this is clear, moving ahead.

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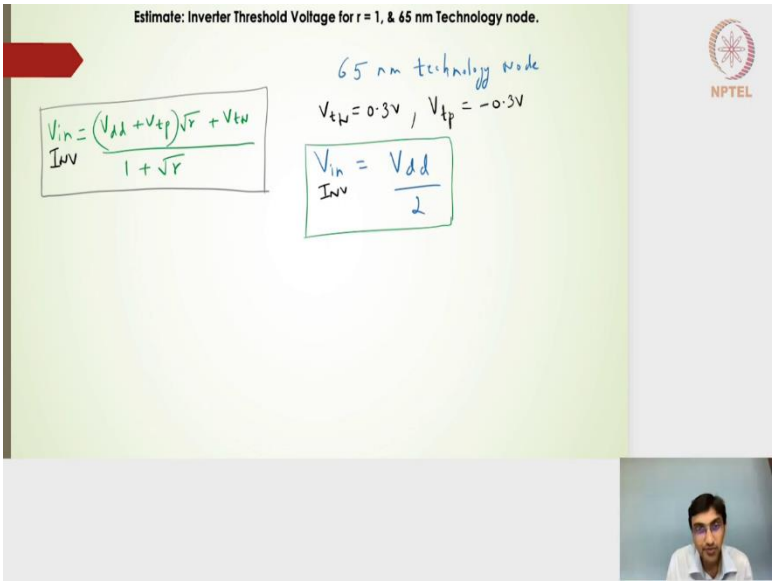

The inverter threshold voltage is given by the same thing, whatever we had got in the previous slide. For a 65 nanometer technology nodes when r = 1, that means it is an unskewed inverter. I am going to write this as an unskewed inverter, because r = 1. If I put the value of r = 1, this is nothing but 1, the $\sqrt{1}$ is anyways 1, $\sqrt{1}$ is 1. The denominator will be 2.

V_{t_N} for a 65 nanometer technology node, we know that V_{t_N} = 0.3, V_{t_p} = -0.3. This is 0.3 volts, V_{t_p} = -0.3 volts, V_{dd} = 5 volts and then we will will get,

$$V_{in} = \frac{\left(V_{dd} + V_{t_p}\right)\sqrt{r} + V_{t_N}}{1 + \sqrt{r}}$$

$$V_{in_{inv}} = V_{dd}/2$$

This is just to validate our expression whether it is correct or not, so what we had seen in our graphical analysis.

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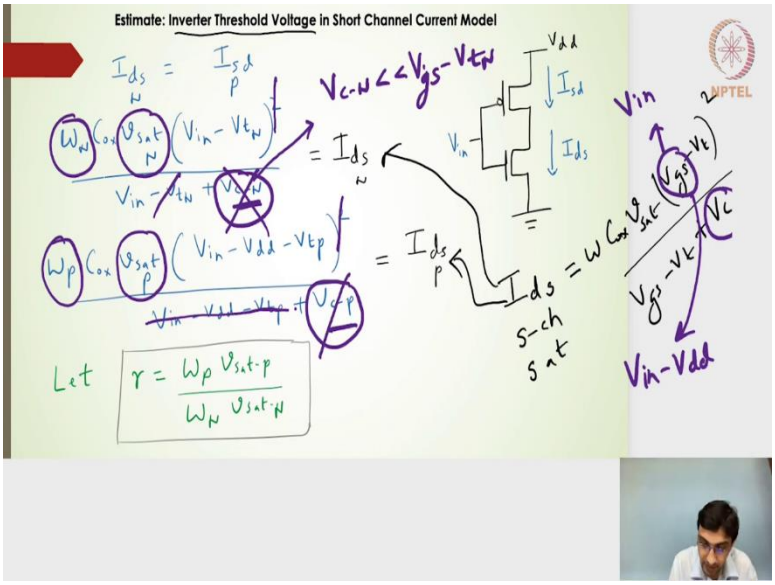

Moving ahead, if I want to estimate it in using the short channel current model. Remember that for the PMOS and NMOS. We now have two different current models, one is a long channel and one other is the short channel. Short channel is the one which scatters towards the mobility degradation and velocity saturation.

It does not accommodate the modulation index, it does not accommodate the change in the drain to the body depletion region and the reducing the channel. That we are not considered yet, but the short channel current model considers only the mobility degradation and the velocity saturation. We have a different expression for that.

Again, even if I am using the same expression, the saturation currents of the NMOS and the saturation currents of the PMOS if I equate it. I should be able to find out what is the inverters threshold voltage. If I am equating the NMOS and PMOS. So, my NMOS the saturation current for the short channel, let me write it here.

$$I_{ds_N} = I_{ds_p}$$

$$\frac{W_N C_{ox} V_{N_{sat}} (V_{in} - V_{t_n})^2}{V_{in} - V_{t_n} + v_{c-n}} = I_{ds_N}$$

This is our general expression. For an NMOS it will be the critical voltage of the NMOS and for the PMOS it will be the critical voltage of the PMOS. That is what I have written it here.

$$\frac{W_p C_{ox} V_{p_{sat}} (V_{in} - V_{dd} - V_{t_p})^2}{V_{in} - V_{dd} - V_{t_p} + v_{c-n}} = I_{ds_p}$$

This particular is short channel current equations and then for the NMOS and then for the PMOS. Of course, the V_{gs} value, let me pick up a different color pointer. The V_{gs} value is now stated in terms of V_{in} for the PMOS and for the NMOS it will be nothing but $V_{in} - V_{dd}$. Similarly for the critical voltage it is defined in terms of the v_{c-n} and then v_{c-p}. This is what we get the current expressions and we need to equate these two current expressions. The skewing ratio for the short channel current model we do not have a β here. The long channel current had the β, but here for the short channel current, it is not the β, it is now W_p.

This particular terms W_N and velocity saturation put together divided by the W_p and v_{c-p} put together. That will be my skewing ratio now.

$$r = \frac{W_p V_{sat_p}}{W_N V_{sat_N}}$$

If I consider those skewing, I mean this as a skewing ratio for the short channel model, equate these two currents.

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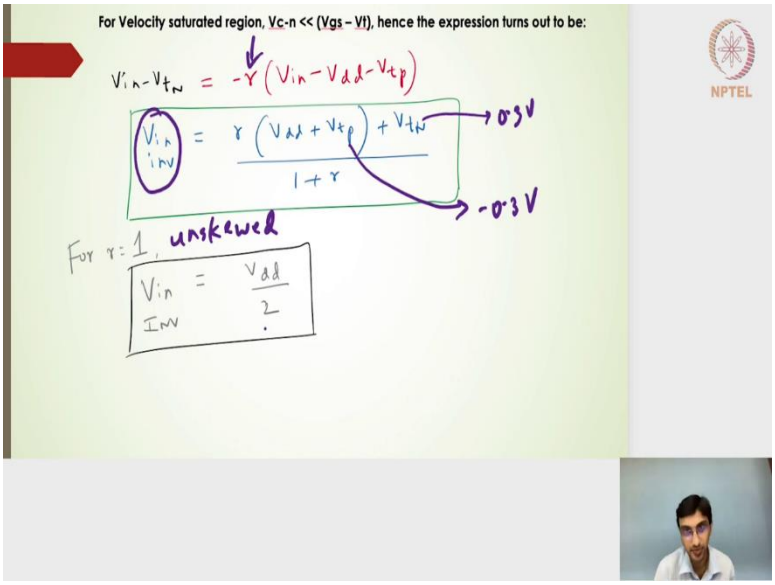

Then I should be able to get an expression, then I should be able to equate these two and then take the r value the skewing ratio, then I should be able to equate it appropriately. There is one more condition which we have taken for the velocity saturated or velocity saturated dominant region in among the transistors. What it means is, if you remember the V_{ds} saturation point is a function of the pinch off effect and the critical voltage.

It is basically the pinch off effect and then the velocity saturation region effect and that determines the V_{ds} saturation. That is when in the short channel model, the currents starts getting constant value. In a velocity saturated dominant region, that means if the v_{c-p} value or the v_{c-n} value in those respective transistors. $V_{c-n} \ll V_{gs} - V_t$. Hence the expression turns out to be

$$V_{in} - V_{t_N} = -r(V_{in} - V_{dd} - V_{t_p})$$

I can actually neglect this $V_{in} - V_{t_N}$. So, this will get. It will become a linear law. Now, if you remember the earlier lectures, we had the square law and then the linear law. So, this is approximately a linear law in a velocity saturated region.

Similarly for the PMOS also, in fact I will have v_{c-p} to be neglected, if it is a velocity saturation region and then this one will get cancelled out. We can approximate it and then finally we will have in a velocity saturated or dominant region, we will eventually get something like this, putting the skewing ratio also into this particular expression. And I have taken a, yeah, I think it becomes a now if I go back, alright, so I will get this particular expression. And finally, the V in inverter the threshold voltage; so this should be the V inverter threshold the voltage is nothing but expressed,

$$V_{in_{inv}} = \frac{r\left(V_{dd} + V_{t_p}\right) + V_{t_n}}{1 + r}$$

If I put r = 1 that is for an unskewed inverter. For an unskewed inverter what should be the value? It turns out to be if r =1, V_{t_p} is anyways negative, V_{t_n} = +0.3 volts, this is +0.3 volts and then this one is -0.3 volt. It will get cancelled. The denominator is anyways will become r = 1, we will be make it 2, this is anyways 1, so we will get,

$$V_{in_{inv}} = V_{dd}/2$$

In this particular lecture what we had seen is using the long channel and then the short channel current model, what should be the inverters threshold voltage, what should be its input voltage that has been applied to the inverter, where we will get the transition region. The output from high to low that is what is called as the transition region.

What should be the input voltage and that is what we have expressed using the long channel model. For the short channel model, especially for the velocity saturated region, this is the particular expression. It is becoming a function of the skewing ratio as well as in the long channel model, it is the inverter threshold voltage is a function of the skewing ratio, as well as in this particular short channel model, the inverter threshold voltage is a function of the skewing ratio.