Design and Analysis of VLSI Subsystems
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Lecture - 10
DC characteristics of Inverter

Today's topic we are going to start the CMOS inverter. As you may be knowing the inverter is the most primitive form of the CMOS digital circuits, especially the digital circuits component. This is what we are going to do today. We will look into more details on the inverter and its current characteristics and using the current characteristics we will have a look at the output versus the input characteristics also called as the transfer characteristics of the inverter circuit.

If you know one can understand the inverter DC characteristics and the transfer characteristics. DC characteristics represents nothing but the current versus the voltage profile. If one can understand that, then the student should be able to appreciate and understand the other digital circuits and its DC and the transfer characteristics. We will begin with the inverter characteristics and see how it goes.

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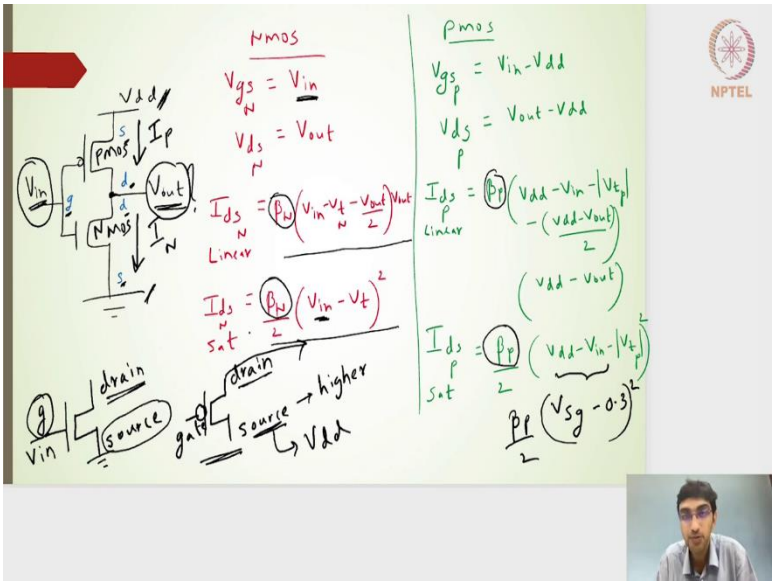

The inverter is, as you may be knowing it is formed of the NMOS transistor and then the PMOS transistor. This is one such circuit where the PMOS is there, PMOS is in series with of the NMOS and where the PMOS is connected to the V_{dd} rail. V_{dd} represents a higher

voltage rail and then the NMOS is the connected to the ground rail. Let me use my pointer, so that I can direct the pointer to the specific points in the circuit.

This is basically the inverter circuit, where the PMOS and NMOS transistors are in series. This particular V_{dd} which is a higher voltage rail compared to that of the ground. Rail in the sense, what in most of our digital circuits design, we will be using or we will be calling the rails as nothing but a power supply we call it as the rails the reason being the rails is defined for the transistor when it actually goes into the layout.

When you fabricate, we have a metal line which is powered by V_{dd} rail, which is powered by one particular power supply, and another one the ground metal line which is connected to the ground power supply. That is how the term rail has been defined for the digital circuits in some of the cases you might and not only some of the cases, but also in few other cases where you will see multiple rails, what it really means is you will have multiple power supplies. You will have multiple power supplies connected to the multiple metal lines. One such case could be a different V_{dd} rails where you have V_{dd1} or V_{dd2} and V_{dd3} and so on.

Those are the different techniques which have been evolved over the times to for several purpose for several applications like to improve the performance or improve the power to save the power or to save the leakage or improve the leakage and get those benefits to that particular digital system design.

Anyway, coming back to this particular topic, where we will have only one power supply which is a V_{dd} and the ground of that power supply is disconnected to this particular ground of the circuit. The question is, if I really want an inverter, how do I connect this PMOS and NMOS transistor.

If I actually connect this PMOS, NMOS transistor closer to the ground rail, and then the PMOS transistor closer to the V_{dd} rail and have them connected together. That means, that they are in series and the PMOS will be closer to V_{dd} rail and NMOS is closer to the ground rail then I should be able to get the inverter output. If I actually swap those positions of the PMOS and NMOS I may not get the inverted output. The inverted output means if V_{in} is high the output should be low and if the input is low the output should be high.

If I swap these two particular positions of PMOS and NMOS I will not be able to get the inverted output and that is why we will have this particular circuit. Just to make a point if I actually swap this positions I will actually get a buffer circuit I will actually get V_{out} to be following the V input, but it is also a very bad buffer design and we will come to it or we will have an deep analysis on that sometime later.

Coming back to this particular inverters circuits, where I have the PMOS and then the NMOS connected in series, although the input that means, the gate of those two transistors the PMOS as well as the NMOS are connected are tied together and that has been supplied with the input voltage V_{in}. The output is, whatever is the common point here of the two transistor is probed as the output voltage.

Now, if I want to actually label the source, drain and the gate terminals of both this transistors. Let us pick the NMOS transistors and let us try to label this. What I am doing is, I have this NMOS transistor where I need to define the gate. I need to define which one is source, which can be represented as s and then I need to define the drains.

For an NMOS transistor we know that the drain has a higher potential than that of the source. The source indeed should have a lower potential than that of the drain. That source should be connected. If I have a power supply of V_{dd} and ground I might as well connect the source with that of the ground potential. The gate is anyways it is an input voltage. I will connect this to the input voltage. That is what I have done here.

I have labeled my source terminal which is connected to the ground is labeled as source here and anyways the gate is nothing but the input voltage that is been feeding into the gate terminal of this particular transistor. If this is the source terminal the other side of this transistor should be the drain.

So, g d and s represents the gate, drain and the source terminal on the PMOS side. The representation or the notation of the PMOS is nothing but very similar to that of the NMOS, just that at the input side it is a bubbled input alright. This is what we will have. This is how the PMOS transistors are denoted and let us say a source and drain again the same thing and then we know where the gate should be also.

For PMOS we know that the source should be at a higher potential than that of the drain right. The source should be at a higher potential. This should be at a higher potential then

that of the drain. If the PMOS is actually tied between this V_{dd} rail. The PMOS is tied between the V_{dd} rail and that of the common terminal here. In fact, this particular transistor, if we look into it one side it is the V_{dd} rail other side it is the ground rail.

This particular potential can in fact reach to a maximum of this V_{dd} or the minimum of this particular ground. The output voltage here whatever I have taken from this two terminals which are connecting to each other. The terminal of the PMOS transistor and the terminal of the NMOS transistor which are connected to each other.

This particular output node whatever I am saying at this point of time. This particular node potential can reach a maximum of V_{dd} and then a minimum of 0. This particular node potential cannot go beyond V_{dd}. Although it cannot go beyond V_{dd} for a particular constraints. We will have a look at it later. Let us say that the V_{out} or this particular node cannot go beyond V_{dd}.

For this particular transistor of the PMOS, the highest potential is actually V_{dd}. On the other side it will be lower than V_{dd} or it can reach a maximum of V_{dd}. It is better to have the source here which is connected to the V_{dd} and then the drain side connected to the node where the NMOS transistor, the other terminal of the NMOS transistor starts.

What it means is for this particular transistor we have the gate terminal here. We have the source terminal which is connected to the V_{dd} that is the source because the source is a higher potential than that of the other terminal and the other terminal is the drain terminal d. So, that is how we have labeled this source, drain and gate terminals for the PMOS and an NMOS transistors which are in series.

Although the gates are connected or tied together. The drain terminals here of both the NMOS and PMOS are actually connected in series. We will see what should be the output voltage with respect to the whatever is the input fed, what should be the output voltage. That is what our aim is in this particular lecture, we need to find out what is the output voltage given an input voltage.

Given an input voltage ranging from 0 to V_{dd}. If the input voltage is V_{dd} what should be the output. If the input voltage is 0, what should be the output. If the input voltage is $V_{dd}/2$ what should be the output. If the input voltage is less than $V_{dd}/2$ and greater than 0 what should be the output voltage and then so on.

We should be able to find out the output voltage if we can identify the currents, if we can identify or write an expression of the current. This current of PMOS and then this current of NMOS and why I am writing the current equation here is or I am drawing the current for the PMOS and NMOS here is because both this transistor are in series.

Thereby this current should be same and this particular current is same given an input. I should be able to write an expression for this particular current of PMOS. Given an input I should be able to write an expression for the current of the NMOS equate it and I should be able to find out what is the output voltage. Hope this is clear.

Given an input voltage I should be able to find out what is the output voltage and if I vary the input voltage my current will vary and thereby it should be able to find out what is the output voltage. It becomes very interesting if we can draw the current versus the input voltage profile or the current versus the output voltage profile as well as the output versus the input profile.

Now, how do we get the current values and how do I draw or derive the current expressions for the PMOS and the NMOS transistors. That is what I have actually put here in NMOS and then the PMOS. I have drawn a barricade here and then written down the current and then the current expressions for the NMOS, the current expressions for the PMOS.

Note that the current expression for PMOS and NMOS there are three different modes: one is the cutoff mode another one is the linear, another one is the saturation region. So, the cutoff region is very very simple, the current should be 0 in the cutoff region. Whenever the input voltage or the V_{gs} value for the NMOS is less than 0.3 volts or the V_t value, then the current is 0 and for the V_{sg} for the PMOS, if it is less than 0.3 volts then it should be the current should be 0 for the PMOS. Assuming that the transistors will be in linear or the saturation region. I need to find out, we are always writing the current expression in terms of V_{gs} and V_{ds}.

The current is always a function of V_{gs} and V_{ds}. What I am going to write is the expressions of V_{gs} and V_{ds} in terms of these two new variables like the V_{in} and then the V_{out}.

If I am picking this particular NMOS transistor then,

$$V_{gs_n} = V_{in}$$

$$V_{ds_n} = V_{out}$$

The current expression I_{ds} in linear and saturation is,

$$I_{ds_{n_{linear}}} = \beta_n(V_{in} - V_{t_n} - \frac{V_{out}}{2})$$

$$I_{ds_{n_{sat}}} = \frac{\beta_n}{2}(V_{in} - V_{t_n})^2$$

In terms of V_{gs} instead of I have replaced this V_{gs} variable with that of the V_{in} and then V_{ds} variable in terms of the V_{out} and that is how I am getting this particular current equation. This is the current equation of the linear and then this is the current equation of the saturation. And then similarly if I want to find out the current expression for the PMOS transistor. The PMOS transistor which is nothing but which is there closer to the V_{dd} rail and then I know what is the terminal labeling as source, drain and gate.

The current we know that it is nothing but in the linear and saturation region, I will have the V_{gs} and then V_{ds} of the PMOS variable. And if I can somehow replace those variables of V_{gs} and V_{ds} in terms of V_{in} and V_{out}. Then I will have both these currents PMOS and NMOS currents, written or expressed as a function of V_{in} and V_{out}. So, that is what I want. We will derive the V_{gs} for the PMOS.

$$V_{gs_p} = V_{in} - V_{dd}$$

$$V_{ds_p} = V_{out} - V_{dd}$$

Current I_{ds} of the PMOS saturation is,

$$I_{ds_{p_{sat}}} = \frac{\beta_p}{2}(V_{dd} - V_{in} - |V_{t_p}|)^2$$

V_t for the PMOS is always minus of 0.3. I have taken the mod of it. It will be minus of 0.3 the whole square alright. This is what I am assuming. This beta P by 2. V_{sg} is denoted or expressed as V_{dd} minus V_{in}, that is what comes here.

Current I_{ds} of the PMOS linear is,

$$I_{ds_{plinear}} = \beta_p(V_{dd} - V_{in} - V_{t_p} - \frac{(V_{dd} - V_{out})}{2})(V_{dd} - V_{out})$$

Now I have both the currents of NMOS and PMOS which are in series. The currents should be same, but expressed in terms of V_{in} and V_{out} and V_{dd}. Of course, V_{dd} will not be a variable, it will be a constant value. So, I have now the current equations in the form of V_{in} and V_{out}. Hope this is clear.

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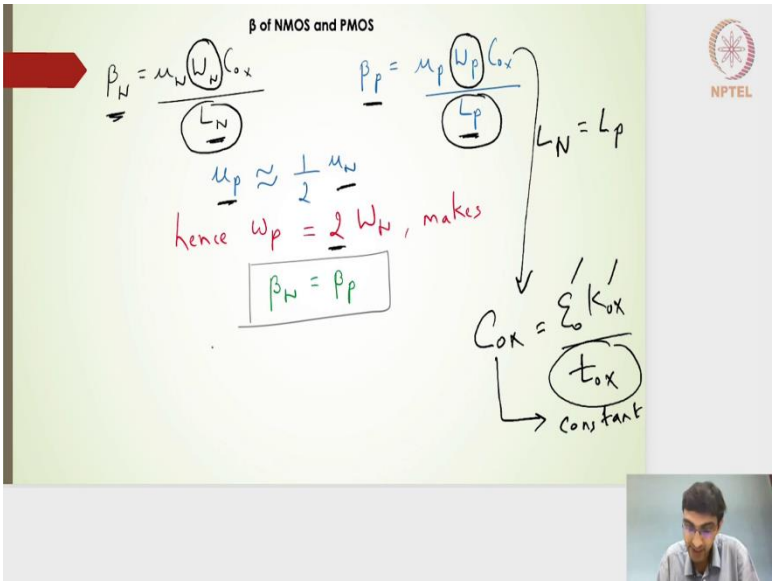

Moving on we had expressed the current expressions of the current equations in terms of β_N and β_p.

Where,

$$\beta_N = \frac{\mu_N W_N C_{ox}}{L_N}$$

$$\beta_p = \frac{\mu_p W_p C_{ox}}{L_p}$$

The channel length in fact for the PMOS and NMOS for a particular technology node we are not going to change the channel length at all. This remains constant.

In fact, L_N and L_p will be same. L_N the NMOS channel and then the PMOS channel will mostly be the same that is how the fabrication process does not allow us to change the

channel length. What we can change is the W, the width of the transistors of the PMOS and NMOS transistor. C_{ox} again is a constant.

Where, $C_{ox} = \frac{\epsilon_o K_{ox}}{t_{ox}}$, $\quad K_{ox} = 3.9$

This is a constant t_{ox} for a fabrication process again for a particular technology node it is a constant. C_{ox} will be a constant value for both NMOS and PMOS. We cannot have a t_{ox} for a NMOS separate or different than that of for a PMOS. My C_{ox} will also be the same, mu for NMOS and mu for PMOS will be different. But, again it will be for an ideal long channel behavior or a model it will be a constant values.

Although the PMOS we effectively take it as close to half of that of the mobility of the NMOS. In that case if I want the β_N and β_p to be the same then,

$\mu_p = \frac{1}{2}\mu_N$

Then I need to increase the width of the PMOS appropriately. In such a case if I have to scale the width of the PMOS such that,

$$W_p = 2W_N$$

Therefore,

$$\beta_p = \beta_N$$

The advantage of having this β NMOS and PMOS to be the same, if I go back to the slide of where I had written the current expressions. If I look into the saturation currents. This β if it is same the β if it is same the betas here if it is same and the way I can make it same is because the width of the PMOS the width of the PMOS is made twice that of the width of the NMOS and then I will have this β to be same and thereby I will have this current equated and then I should be able to find out the V input or rather if I make this β to be same and if I am equating the currents. I do not know whether it will be the saturation of PMOS and saturation of NMOS will be equated or linear of NMOS and then saturation of PMOS will be equated there I should be able to find out the Vout as a function of only V input. What we are trying to do here is we are making the β to be the same, not necessarily that the β will always be the same.

If I want to change the width of the NMOS and then the PMOS. It is not necessary that the β will always be the same, but just for the primitive calculations I am taking a very simplest case making the β to be the same, and then trying to see what happens to the output as a function of input or input as a function of output alright.

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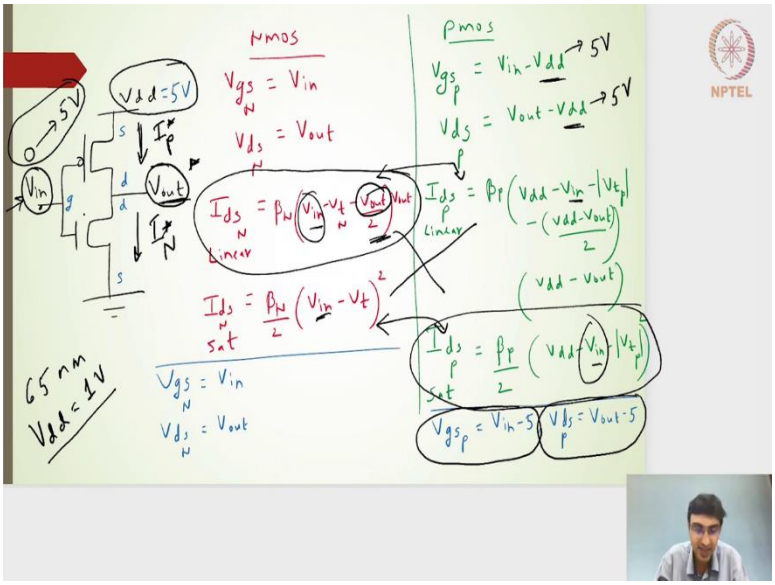

Coming back to this particular slide of the inverter, where we had the PMOS and NMOS in series. This particular V_{dd} let us for time being let us say that we will fix it to 5 volts. Generally for a 65 nanometer technology node which we will generally use, the V_{dd} values are generally 1 volts not more than that. Maximum of it will go to 1.2. The minimum it might go is 0.8 volts.

But, here I am taking a very kind of a scaled V_{dd}. That I should be able to see the solutions much more at a little bit at a higher voltage. Practically most of the examples of the 65 nanometer technology we will always have it as 1 volts, but just for a theoretical understanding I am just taking it the 5 volts.

What it implies is my input voltage can actually put the input voltage from 0 to 5 volts, not beyond that and not less than 0 volts. It cannot go beyond 5 volts it cannot go less than 0 volts. If I have this 0 to 5 volts; that means, if the input voltage is 0 what should be the output voltage? What should be the current? What should be the current here? What should be the current here?

If the input voltage is 1 volts what should be the current here? What should be the current here? What should be the output voltage? If the input voltage is 2 volts what should be the current here current here and output voltage? If the input voltage is 5 volts what should be the current? And what should be the output voltage? And we have anyways this current expressions right.

If I actually in the last slide we had express this V_{ds} in terms of V_{dd}. Now I will replace this V_{dd} with that of the 5 volts and that is what I have put here,

$$V_{gsp} = V_{in} - 5 \; ; \; V_{dsp} = V_{out} - 5$$

Hope this is clear.

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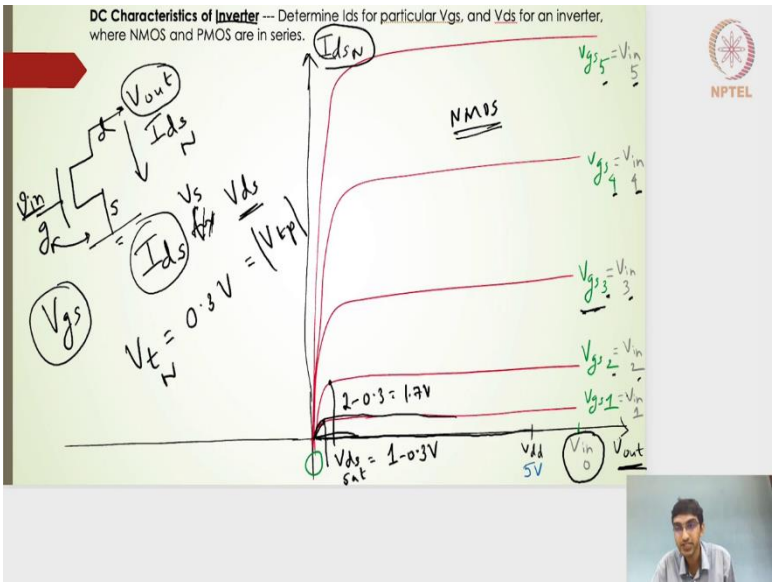

We are now in a position to draw the current versus the output voltage. What it means is for a different V_{gs} values how should the current and then the V_{ds} profile looks like. Now what it we really want is the DC characteristics of an inverter. So, if I go back to the previous slide what we really want is the current here the current here which is same because both the transistors are in series right with respect to the different V_{out} voltage right for a specific values of V_{in} voltage.

What we really want is an inverter if I apply an input here what should be the output voltage, and what should be the current that is what we want. What we are going, I mean

the way we are going to achieve this is we will we would like to have the current expressions of the PMOS and of the NMOS right. If we know what is the current expression of PMOS and what is the current expression of NMOS. For that I need to know what expression of NMOS I need to write whether at the linear region expression or the saturation region expression and equate it to that particular PMOS current. where we need to know that whether the PMOS is in saturation or the linear region. I can actually equate this to this or I can equate it this to this or I can equate it to this to this right or I can equate it to this to this. There are 1, 2, 3 and 4. If I have those four equations evaluated I should be able to know for a particular V_{in} voltage, what is the current, what is the solution current, and what is the solution output voltage.

Now, for example, if I actually equate let me take one such example. If I equate this current and let me say that I will equate this one and if I equate this the current if I equate it because both the transistors are in series I will have this V_{in}. I will have the V_{out} in terms of the as a function of V_{in} and I can make some judgment about it.

But if you do this particular mathematical equation. What I meant was the V_{out} as a function of V_{in} and if I know what is the V_{in} value, I should be able to estimate what is V_{out}. What we can do is if we can have some kind of a judgment of whether the NMOS will be linear or PMOS is in saturation or PMOS is in linear or NMOS in saturation or the vice versa whatever it is I should be able to equate those two expressions.

But, to start with we really do not know whether the NMOS or PMOS is in saturation. It actually depends on this particular V_{out}. If I look at it; it actually depends on this V_{out} and V_{out} is a variable itself. Now we do not know whether it is closer to V_{dd} or the closer to the 0 volts or if this is 5 volts whether it is 2.5 volts or 1 volts or 2 volts.

In that case if we really do not know at this particular point of time, with some experience we should be able to match those currents, but at this point of time when we are very inexperienced, we draw the current versus the output voltage profiles of the NMOS and PMOS graphically and wherever those profiles of the currents intersect the PMOS and the NMOS current.

If they intersect, that means, the NMOS and then the PMOS currents are same at that particular point. That particular point will give me the V_{out} and then the V_{in}. If we do not know the modes or the regions of NMOS and PMOS transistor.

One way to find out the solution of the current and then the output voltage for a given input voltage is to graphically draw the NMOS characteristics, graphically draw the PMOS characteristics and then somehow try to intersect the IV characteristics of the NMOS, IV characteristics of the PMOS. Wherever that intersection happens we know that the currents are same. Those particular voltage values will give me the V_{out} voltage. This is the overall aim.

To begin with what we are doing is I have the NMOS transistor, this is connected to ground and then this is nothing but the output voltage and then we have the gate voltage here which is nothing but feeded with the input voltage, this is the source this is the drain as I had written as per my labelings. In this particular case for an NMOS transistor I know that for a different V_{gs} I should be able to find out the Ids profile.

I_{ds} profile for the V_{ds} or rather I should write it as I_{ds} versus V_{ds} for a particular value of V_{gs}. For an NMOS transistor here, this is nothing but an NMOS transistors standalone profile. Given an fixed input what should be the V_{ds} I mean what should be the I_{ds} for a different values of V_{ds}, this is what I have written: the linear region, saturation region.

Linear region saturation region, linear region, saturation region, linear region, saturation region linear region and saturation region, linear region saturation region for different values of V_{gs}. In this particular case let us take that $V_t = 0.3V$ for the NMOS as well as for the PMOS. For the NMOS is equal to I am going to write it as $|V_{tp}| = 0.3V$..

Anything if V_{in} is 0, we know that the current will be 0. This particular line which is parallel to the x axis is my 0 current line when the input is 0. If the input is 1, that means V_{gs} is actually 1 volts, I will get this particular current profile, up till this particular value is V_{ds} saturation. Which is nothing but 1 minus 0.3 volts, that means 0.7 volts up till that it will be linear and after that it will be saturation.

Similarly, V_{gs} of 2, when V_{in} is of 2 volts, V_{gs} of 2 this is a different V_{gs} value. I will get the saturation current I will get the linear current. Again, this particular value turns out to

be and if I pick this into the V_{ds} axis, this particular V_{ds} value will be nothing but 2 minus of 0.3 that will be 1.7 volts. Similarly, I should be able to find the current versus the V_{ds} profile for a different V_{gs}.

Now, V_{gs} is 3, V_{gs} is 4, V_{gs} is 5 I should be able to draw the current versus the voltage characteristics. Remember if I have drawn this as I_{ds} current, this is nothing but the I_{ds} of NMOS. I_{ds} of NMOS this is the current and if I write the V_{ds} it is nothing but V_{out} minus 0, that is why this particular axis I have written it as V_{out}. For different values of V_{gs} we are drawing the IV characteristics, the I_{ds} current versus the V_{ds}. The I_{ds} is nothing but the I_{ds} of NMOS and V_{ds} is now rewritten as V_{out} minus 0 which is nothing but V_{out}. This particular values V_{gs0}, V_{gs1}, V_{gs2}, V_{gs3}, V_{gs4}, V_{gs5} is relabeled as V_{in} of 0 V, input of 1, 2, 3, 4, 5.

This subscript of 4, subscript of 3, subscript of 2, 1 and 0 and then 5 here represents that the input voltage I am applying an input voltage of 5 volts. V_{gs} will be nothing but 5 volts. If I am applying a input voltage of 4 volts V_{gs} will be nothing but 4 volts and if I am applying an input voltage of 3 volts V_{gs} will be nothing but 3 volts. If I am applying an input voltage of 2 volts V_{gs} will be nothing but 2 volts and then so on.