Semiconductor Device Modeling
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Lecture - 41
DC Model of a Large Uniformly Doped Bulk MOSFET: Qualitative Theory

In this module, we begin a discussion of the DC model of a large uniformly doped bulk MOSFET. In the previous module, we remarked that a modern MOSFET is a small geometry device with substrate atoms arranged randomly. However, to module this device we go about in a series of steps in which the starting point is a large geometry device with uniform substrate doping.

So that is what we are going to start with now. Now we have remarked that there are 9 steps in deriving model for any set of device characteristics.

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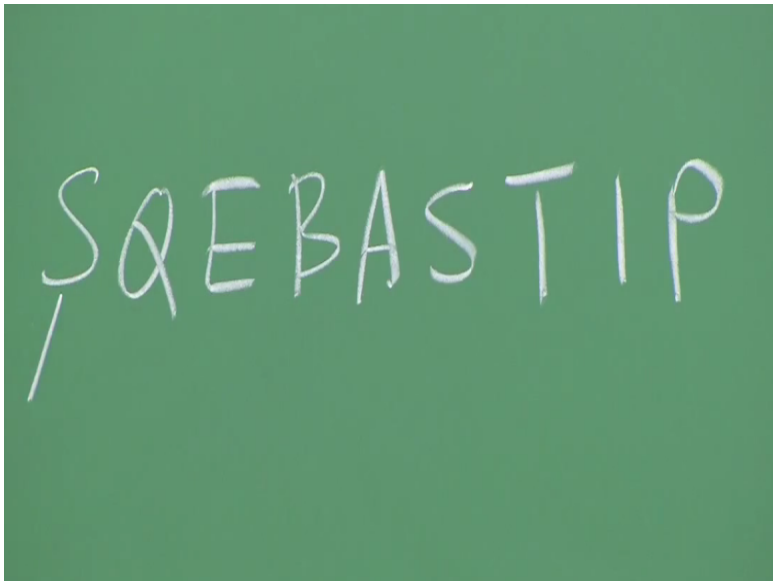

The 9 steps are SQEBASTIP. In the previous module, we discussed the structure and characteristics of the MOSFET. Now once we know what is our goal? What are the characteristics we want to model? We can begin with the qualitative theory. Now that is what is the topic of this particular module.

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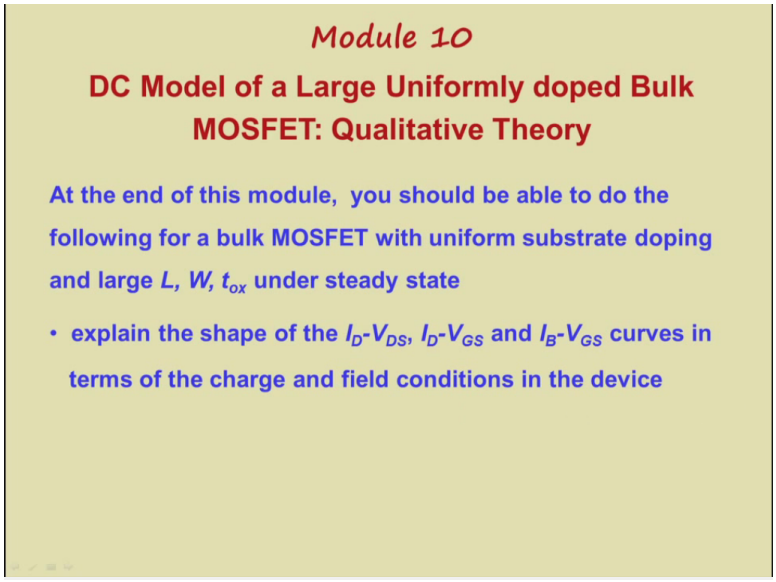

At the end of this module, you should be able to do the following for a bulk MOSFET with uniform substrate doping and large L that is channel length, W that is channel width, t ox that is oxide thickness under steady state conditions. First, we must be able to explain the shape of the ID-VDS, ID-VGS, and IB-VGS curves in terms of the charge and field conditions in the device.

Now note here, we are talking about drain current, we are talking about bulk current or substrate current, but we are not talking about the gate current. Now the reason for this is we are considering a device with thick oxide and if the insulator is thick then the leakage current through that is very small. That is the reason why we are not considering the behavior of the gate leakage.

Now let us look at the shapes of ID-VDS, ID-VGS, and IB-VGS curves, which were introduced in the previous module.

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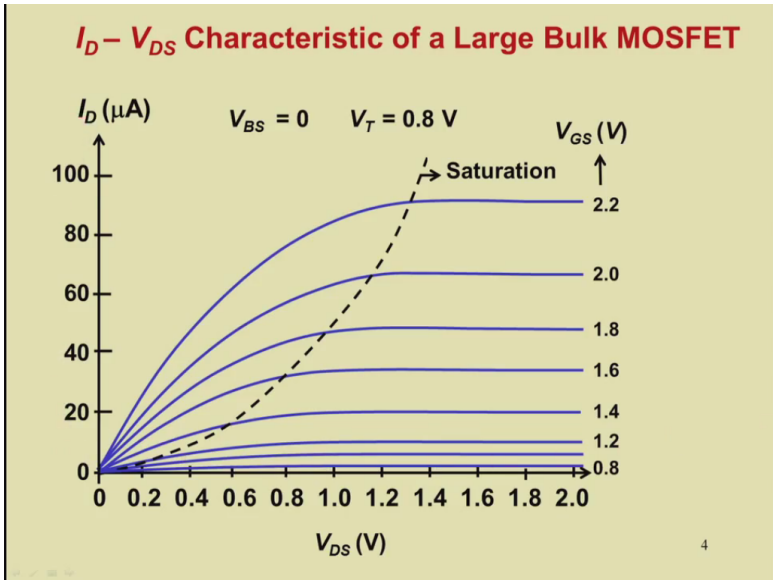

This is a ID-VDS map. The important features here are that the drain current rises as you increase the VDS and progressively the rise tapers off and beyond some point the current becomes almost constant. This is the saturation region. Now the point at which saturation happens are the value of VDS at which the current saturates goes on increasing as VGS increases.

So you can see here this is increasing VGS and the value of VDS at which saturation occurs is going on increasing. Now when you plot the current ID on a linear scale, you cannot expand the portion of the characteristics for VGS less than threshold voltage that is 0.8 volts. VT = 0.8 volts for this device. Now the current for VGS < VT that is 0.8 is important though it is small.

You know that in any circuit the memory of the logic levels 1 or 0 is stored in terms of the charge on a capacitor. Now if the device connecting to a charge capacitor is off, ideally the device should not leak any of the charge; however, in practice we know that even below gate source voltage = threshold voltage there is some small current that the MOSFET draws and this small current would leak the capacitor charge and it may change the logic level.

See in order that the logic level does not change and the memory is preserved, you may have to refresh the circuit periodically. Therefore, the amount of charge that leaks during the off state is important and that is why the characteristics of VGS < VGS = VT. The characteristics of the drain current versus VDS for VGS < VT is important. Now that can be shown if you change the drain current access to a log scale.

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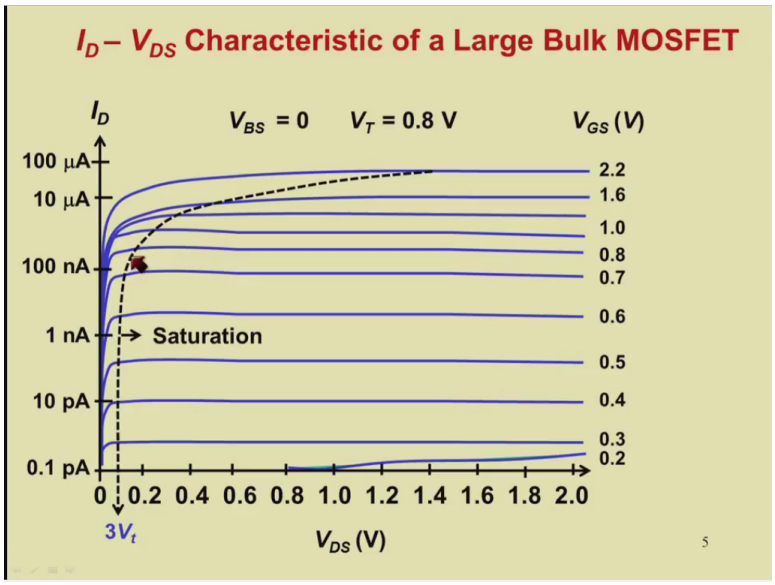

Now when you do that you can see here that the region VGS < VT is expanded a lot. The important feature to be observed here is that the increment in ID on the log scale is uniform for uniform increment in VGS, which means ID versus VGS is exponential for VGS < VT. So this is something we would like to explain. Another feature that you see is that the value of VDS for which the current saturates is approximately constant at 3 times VT for VGS < VT.

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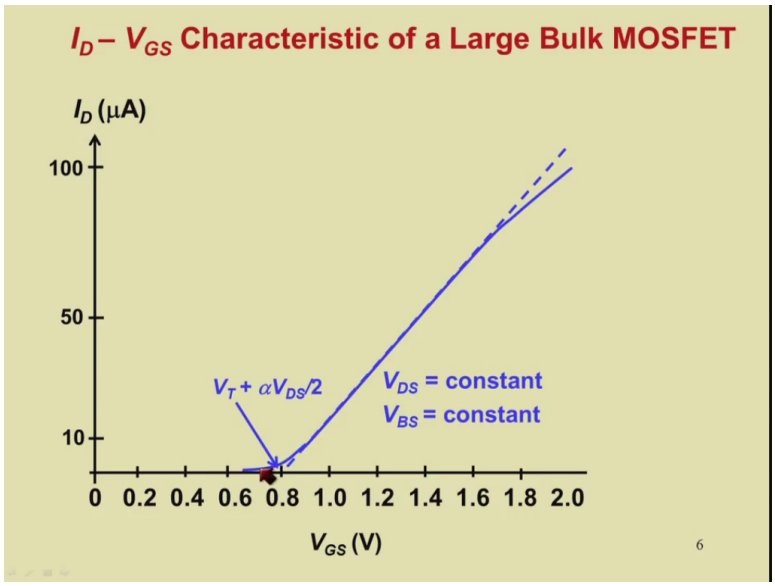

Let us look at the ID-VGS curves that we have to explain in our qualitative model. The ID-VGS curve shows a predominant linear region if extrapolate that linear region to the VGS axis, you can get the value of voltage, which is threshold voltage plus a very small value dependent on VDS. This formula we will explain later when we derive the ID-VDS, ID-VGS equations.

Now for large values of VGS, the rate of rise of ID tapers off a little bit and for values of VGS around VT you find that there is a rapid decrease in the current. Now to expand these current levels near VT once again we use the same trick that we used for ID-VDS characteristics.

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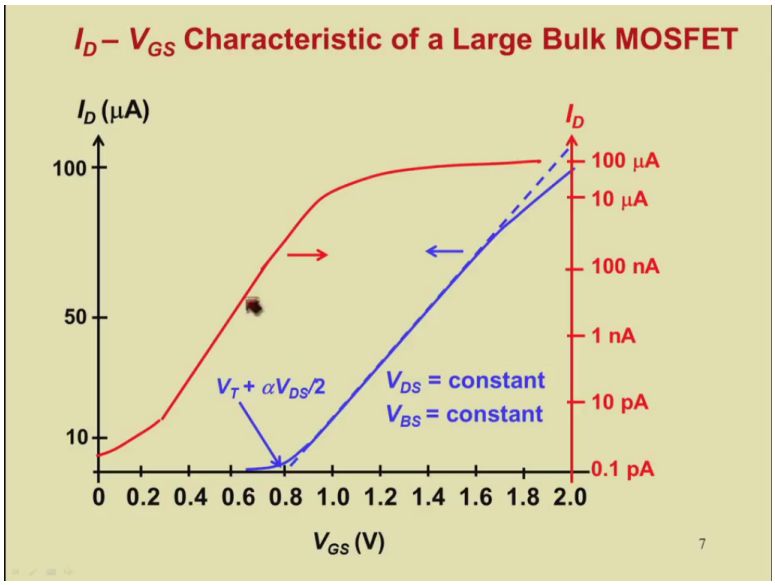

We change the ID axis to a log scale. Here you can see that the ID as a function of VGS is linear when the ID is plotted on the log scale, which means ID-VGS characteristics near VGS = VT that is this region are all exponential in nature ID as the function of VGS is exponential.

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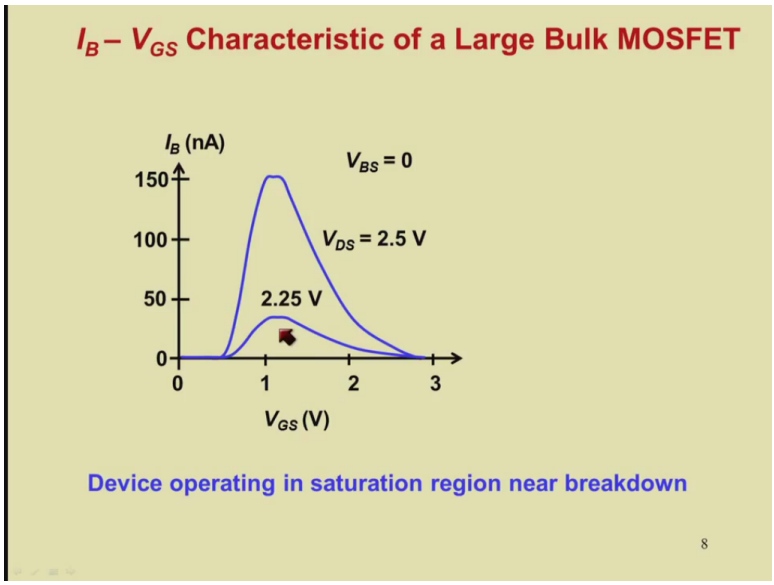

Now let us look at the shape of the IB-VGS curves, which we introduced in the previous module. So the IB-VGS curves are generally plotted for device operating in saturation region

near breakdown because for a device below breakdown the substrate current is not much. So near breakdown what you find is as you increase your VGS for a fixed VDS, the current rises beyond a certain voltage, reaches a peak and then falls off.

The peak occurs at approximately half the value of VDS. When increase in VDS, the current increases, but the shape remains the same. Let us see what other things we should be able to do at the end of this module.

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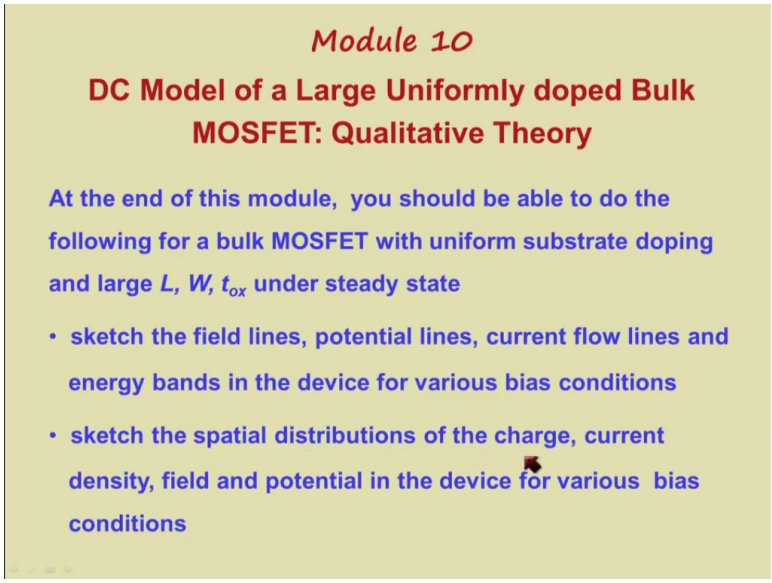

You should be able to sketch the field lines, potential lines, current flow lines and energy bands in the device for various bias conditions and finally you should be able to sketch the spatial distributions of the charge, current density, field and potential in the device for various bias conditions.

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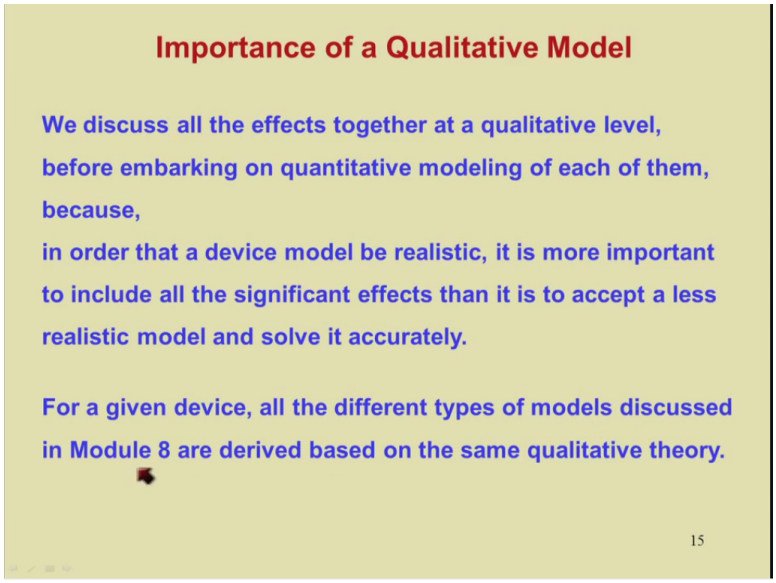

Now let us make a comment regarding the importance of a qualitative model. In qualitative modeling, we discussed all the effects together at a qualitative level before embarking on quantitative modeling of each of them because in order that a device model be realistic it is more important to include all the significant effects than it is to accept a less realistic model and solve it accurately.

For a given device, all the different types of models discussed in module 8 are derived based on the same qualitative theory. Now this is an important point that you have different types of models, but the qualitative theory underlying the various models is more or less the same.

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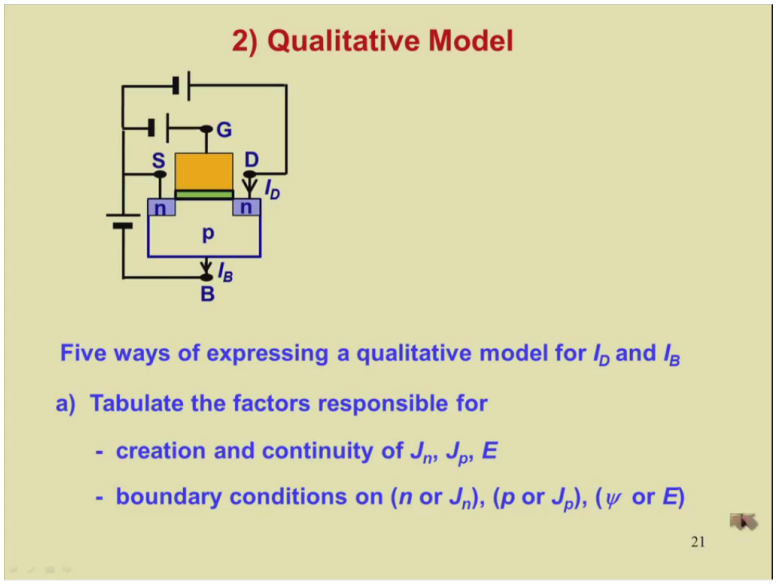

Let us list out what are the things we need to do in qualitative modeling? First, we sketch device schematic showing the bias conditions. Let us consider an N-channel MOSFET. For

an N-channel MOSFET, the drain is positive with respect to source or rather whichever n contact is positive between the 2 n contacts that contact is the drain because in an N-channel MOSFET, the current flow is because of electrons.

The source provides the electrons and the drain collects. Now you know that the most positive terminal would collect the electrons. Therefore, the drain is positive with respect to source so that is this power supply. Now since you need electrons at the interface and the substrate is p-type, the only way you can achieve is if you make the gate positive with respect to source so that is what is indicated here.

Finally, you can have situations in a circuit when the bulk may get reverse biased with respect to the source and that is what is shown here. So these are the 3 power supplies okay. VDS, VGS and VBS. You have the drain current flowing into the drain because the electrons flow out of the drain and you have the bulk current flowing out of the bulk terminal. The reason why the bulk current flows out can be understood very easily considering the polarity of the drain and bulk.

The drain is positive with respect to bulk. Therefore, any current from drain to bulk for example should be in this direction. Same way you can argue about the source to bulk current right from the polarity of the bias here. Now what I am going to do is I am going to list out from a previous module in which we discussed the procedure for device modeling. The steps associated with qualitative modeling. So this is repetition from a previous module.

There are 5 ways of expressing a qualitative model for any characteristics. In this module, we are discussing the characteristics of the drain current and the bulk current of a MOSFET. What are the 5 ways? Now first, we should be able to tabulate the factors responsible for creation and continuity of electron current density, hole current density and electric field and we should tabulate the factors responsible for boundary conditions on carrier concentrations or the carrier current densities and potential or field.

That is n or Jn, any one of the 2 or any one of this pair p or Jp or any one of this pair psi or E.

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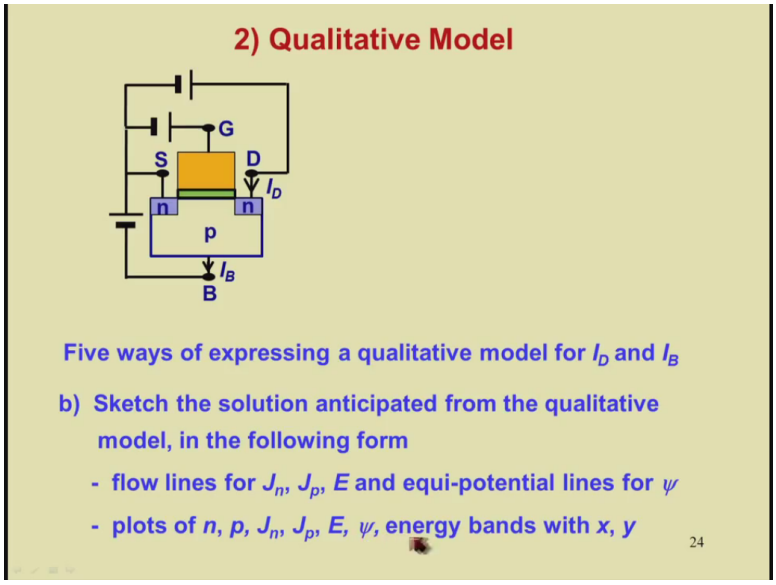

Apart from these 2 ways, the other ways are sketch the solution anticipated from the qualitative model in the following form, flow lines for Jn, Jp, E and equi-potential lines for psi and plots of n, p, Jn, Jp, E, psi and energy bands with x, y that means we must be able to sketch the spatial distribution of carrier concentrations, carrier current densities, electric field, potential and energy bands.

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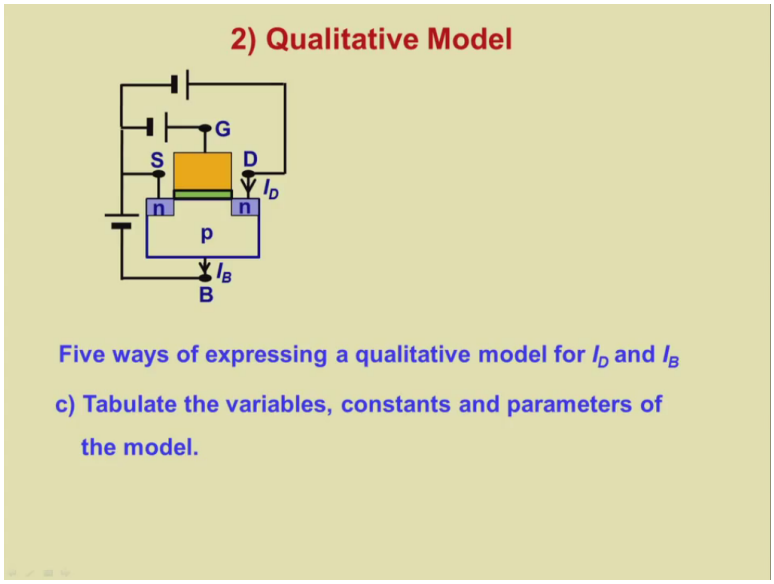

Now apart from these 4 ways, finally we should tabulate the variables, constants and parameters of the model.

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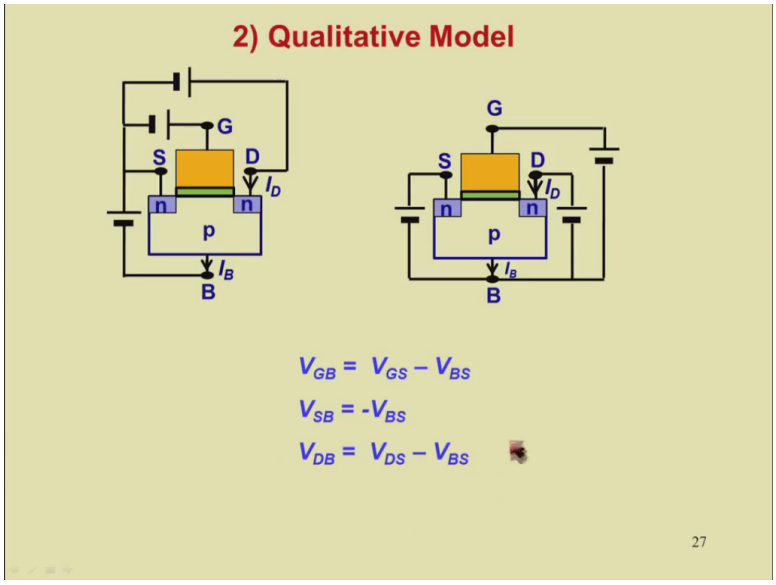

Now let me repeat an important point. In circuit applications, the device is always biased with source as the common terminal. However, from the point of view of device modeling where we want to derive the expression for current as a function of the terminal voltages starting from device physics it proves more convenient to bias the various terminals of the device with respect to the bulk.

Now what is the advantage of biasing with respect to bulk? Here you can see that this power supply appears across these 2 terminals of the source bulk junction. This power supply here VDB appears across the 2 terminals of the drain bulk junction and this power supply VGB appears across the 2 terminals of the gate to bulk junction right. Now you know that it is easy to model the conditions of charge, current etc in the device as a function of the terminal voltage for any junction okay.

So here we can model a charge conditions directly in terms of terminal voltages on the junctions. On the other hand, if you compare it with this picture, here you find for example if you take the VDS, the VDS drops across series of 2 junctions, drain bulk and source bulk junction. So I will have to separate the VDS into the voltages across these 2 junctions if I want to model a charge conditions in the device as a function of this.

Now same thing applies to VGS. So VGS and VSB together will decide the voltage between gate and bulk. So when I want to model the charge conditions in the device as a function of VGS, I will have to take into account VBS also. Now this kind of complication is avoided when you consider all biases with respect to bulk. After we have derived the drain current ID

and IB as a function of VGB, VDB and VSB we can always transform the equations to equations for ID and IB in terms of VDS, VGS and VBS.

These are the equations for doing so. So you take VGB and replace the VGB/VGS-VBS. Now similarly you have the other voltages, VSB - VBS and VDB is VDS-VBS. So you can make this replacement in the equations derived then the characteristics will become a function of VGS, VBS and VDS.

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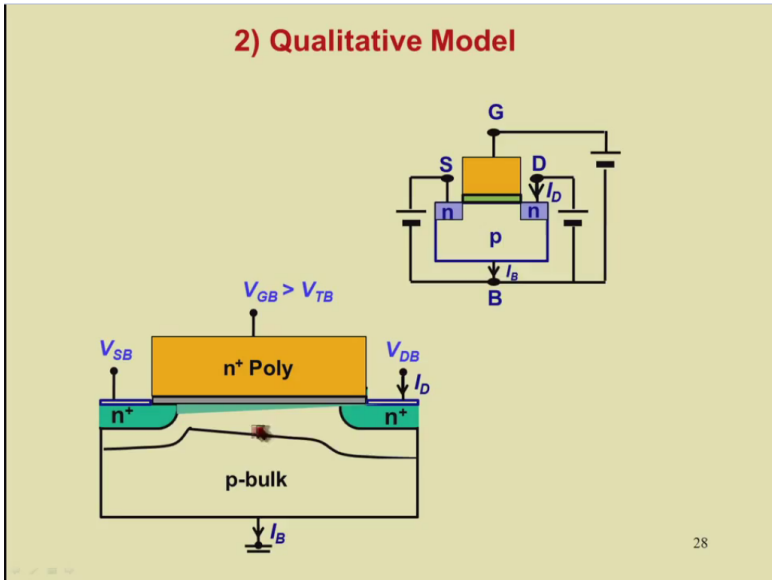

Now let us look into the charge conditions in the MOSFET for the biasing arrangement that we discussed. For gate to bulk voltage more than a value known as a threshold voltage, you have inversion layer of mobile electrons at the interface in an N-channel MOSFET. Beneath the inversion layer, you have a depletion layer from which all carriers are depleted out. Now for sufficiently large value of VGB or VTB, you have a significant current flowing from drain to source if VDB is more than VSB.

The inversion layer charge progressively decreases from source to drain as indicated here and the depletion layer charge increases from source to drain as indicated here. Now how does this happen? This is what we need to explain in our qualitative model. To explain the charge conditions in a MOSFET, which has all the 3 biases namely VGB, VDB and VSB. What we do is we proceed in the following steps.

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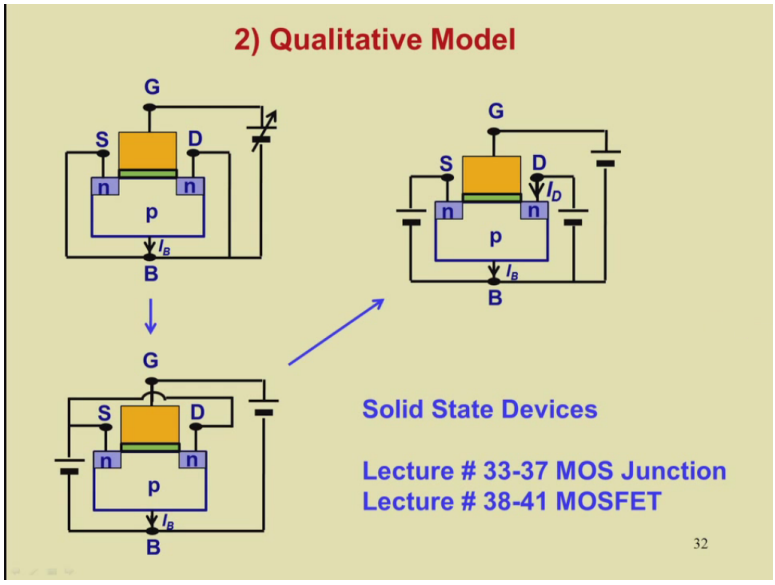

First we analyze the charge conditions in a MOSFET in which only VGB is applied. VSB and VDB are shorted. This is a simple situation. So after this analysis, we move on to analyzing a device in which there are 2 biases VGB and VSB. The VDB = VSB as shown here so drain and source are shorted therefore there is no drain to source current in this case.

So in other words we have VGB and then we have introduced another voltage VSB that is reverse biased source and drain with respect to bulk and then we analyze how the charge conditions get modified. In the third step, we separate the source and drain and bias the drain positively with respect to bulk as shown here and if you have VDB more than VSB then you have a drain current flowing. So then we analyze this structure.

Now in a previous course title solid state devices which is available in YouTube, I have discussed details of charge conditions in all the 3 cases here in to following lectures. So lecture 33 to 37 titled MOS junction discusses the charge conditions in a MOSFET for these 2 biasing arrangement and the lecture 38 to 41 titled MOSFET discusses the charge conditions in this biasing arrangement.

In other words, a first level model of the MOSFET is available in this basic course titled solid state devices available in YouTube. So I would encourage you to view these lectures before proceeding further. However, for the sake of convenience I am going to summarize some important points from these lectures in the present lecture so that we can proceed further and develop a more complete model of the MOSFET.

In the first level course on solid state devices, we have a fist level model of the MOSFET. This is an advanced course so we would like to go beyond what we discussed in the first level course.

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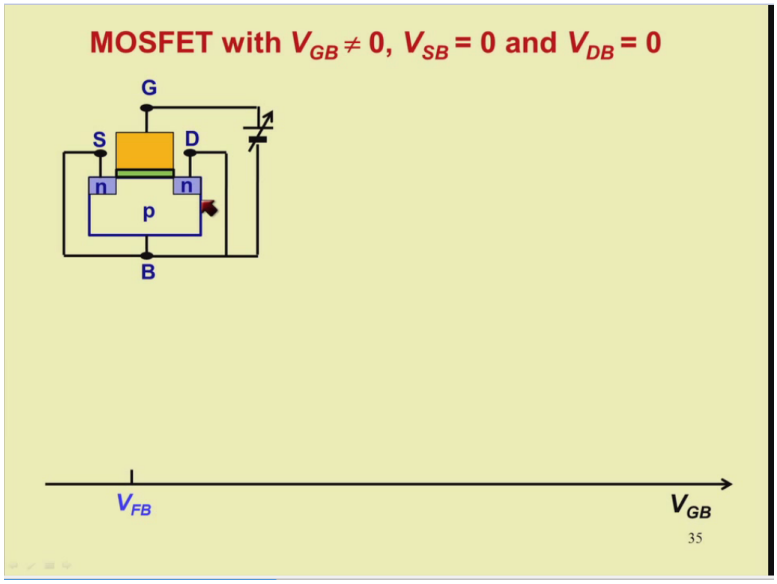

Now here is the summary of this important features. Let us begin with a MOSFET with VSB and VDB = 0, but VGB != 0. Let us draw a line indicating the VGB axis, the first important point we get on this axis is the so called flat band condition and the voltage corresponding to that is the flat band voltage. Now let us explain what is this condition? In our explanation, we shall be concentrating on this central part of the device okay here which means we will be ignoring the source and drain junctions and the associated depletion regions here.

This is because it is a large MOSFET and the distance between the source and drain is very much large compared to the depletion widths in the substrate from source and the depletion width in the substrate from the drain.

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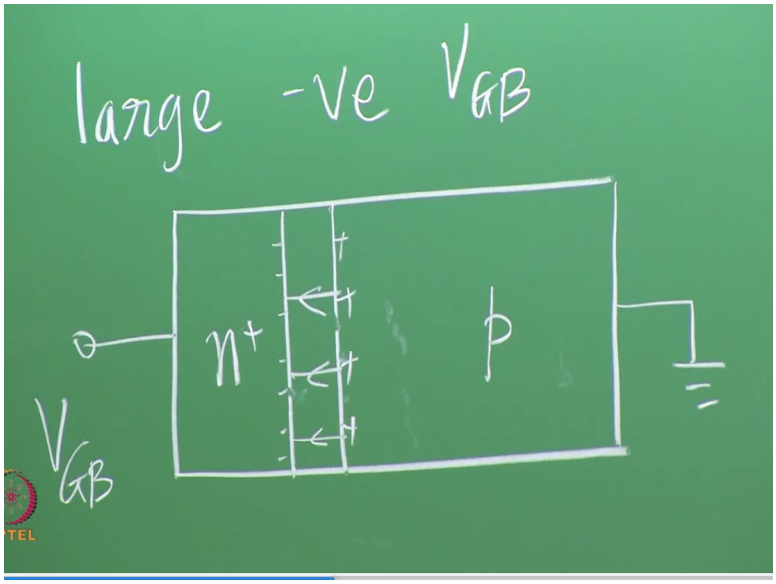

Now we will draw the MOSFET in such a way that your gate terminal is to the left and the bulk is to the right. In other words, as compared to this diagram here, I am going to turn the MOSFET 90 degrees, move this gate to the left so that the bulk comes to the right. The reason for that is we would like to plot various charge-field conditions in the device and those conditions are best plotted with one axis, the spatial axis the distance horizontal.

Now consider the case of large negative VGB. If VGB is very large and negative, you have a negative charge here because of electrons and positive charge because of holes. See you have a field directed like this.

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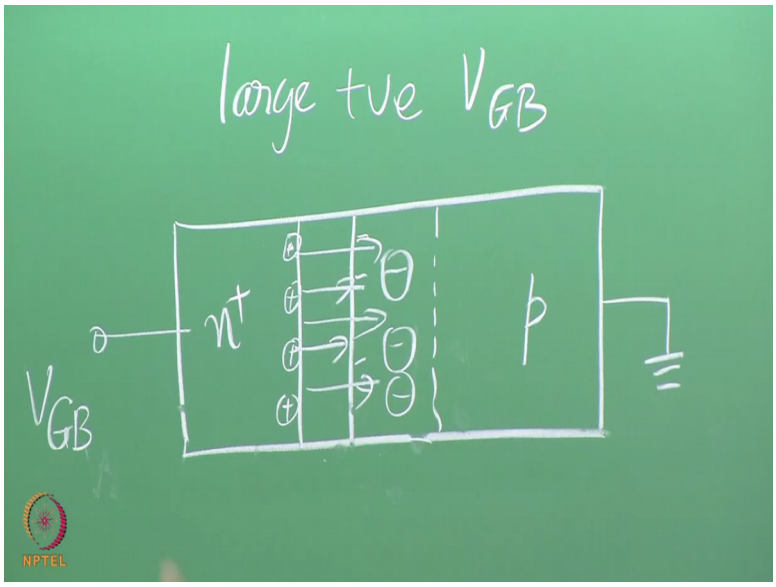

If I consider large positive voltage, then the conditions would be as follows. So here you will have a positive charge on the gate, the positive charge can be created by removing some

electrons from here and exposing the ionized donors and here you can get a negative charge by attracting the electrons to the surface, but electrons are minority carriers so you can get a negative charge by depleting the holes, moving away the holes because the field is like this.

This field can drive away the holes leaving behind a region of no holes and electrons can be attracted to the surface. So you can have a negative charge in this case. So evidently between large positive VGB and large negative VGB you have a condition when there is no charge in the substrate. Let us show that here.

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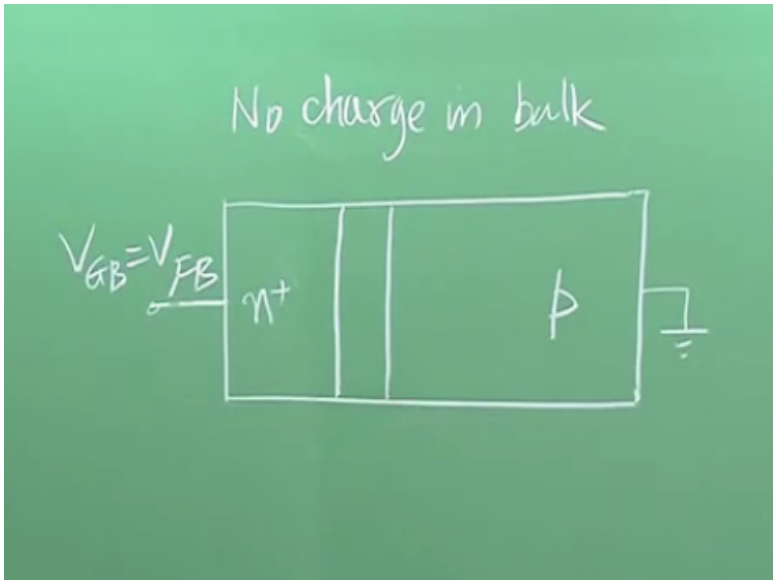

So this is VGB = VFB. So here no charge in bulk or substrate. Now does it mean no charge in the gate? We will come to that point shortly. Let us first talk only about no charge in the substrate. Why should this condition be called flat band okay? For that we have to draw the band diagram in the piece of state for this condition.

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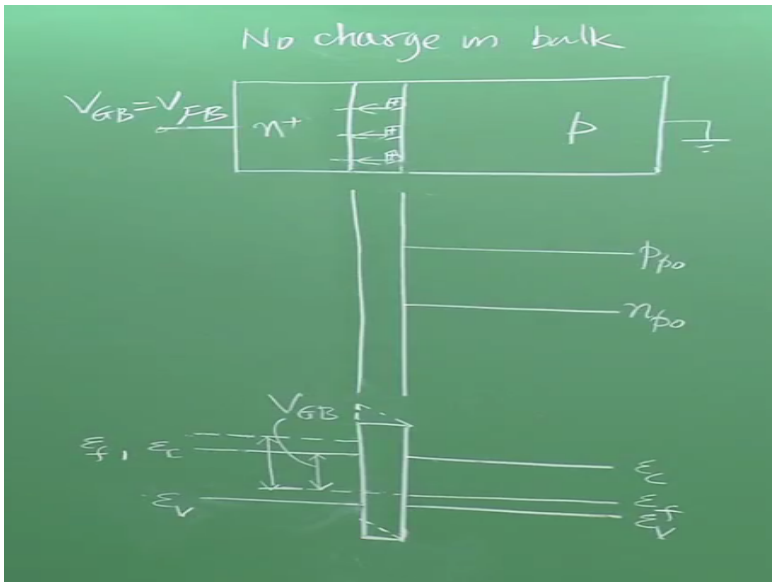

Now before that let us draw the concentration. So if I am going to draw the concentration, if there is no charge that means the hole concentration remains = Pp0 and electron concentration remains = Np0 because the substrate is uniformly doped no charge means that the carrier concentration is constant. Please note, that if this is non-uniformly doped, carrier concentration would not be constant even if there is no charge okay.

Because hole concentration and electron concentration will change according to the doping. Now let us come to the band diagram. So this is your Ec and this is your Ev and this is your Ef, it is a p-type substrate so bands are flat. Because the bands are flat it is called a flat band point right. If the concentration is constant then Ec and Ev levels are all constant because Ef is constant under equilibrium, no current is flowing here right.

Because there (()) (26:14) oxide in between n+ and p, no current flows this under equilibrium. Now let us complete this picture and draw the bands on the n+ side. On the n+ side, the bands would look like this. This is Ec and we will assume that the doping here is so heavy that the Fermi level coincides with Ec. So this is your Ev and this line should be exactly next to this because energy gap is same for both substrate and gate.

Now this is the band picture in the n+ region. Now this picture will tell you why the flat band voltage can be non-zero. So you see the Fermi level in the gate is not at the same level as Fermi level in the substrate. Let me also show the conduction band and valence band in oxide for the sake of completeness. This diagram is not to scale okay. So this is your Ec in oxide and this is your Ev.

So evidently to achieve this condition, you have applied a voltage equal to the difference in the Fermi levels that is this. So the gate to bulk voltage for this condition is equal to the difference in Fermi level for this condition, which is this, which is the flat band voltage. So this is your VGB. So please note how did we come up with this condition? First we said that we want condition of no charge in the substrate and no charge in the substrate means bands are flat, it is like this.

Then we drew the corresponding band picture in n+ side, here also the bands are flat and then because the doping here is different from doping here Fermi level here was different from the Fermi level here. Then from the difference of the Fermi levels, we concluded about the gate bulk voltage to be applied to achieve this condition. So this explains why VFB can be non-zero.

Another reason VFB can be non-zero is because of the fixed charge in the oxide substrate interface. Now because of this fixed charge what happens is the following. If I do not want any charge in the substrate for some gate to bulk voltage it means that this positive charge cannot terminate on negative charge in the substrate. So where will the field lines from this positive charge terminate in that case?

They have to terminate on the gate. Now this means there is a field in the oxide. Now here we have drawn the conduction band of the oxide flat, there is no field in the oxide. This is very interesting please remember. In the absence of this positive charge, though we have applied a gate to bulk voltage there is no field in the oxide because there are no charges. Now however there is a field, this field is directed from substrate to gate.

Substrate is positive, I mean the interface towards the substrate is positive and interface towards the gate is negative you can see that from here. This means in energy band picture, your energy band in the oxide will be like this, something like this right. This band bending indicates the field and you know that in energy band diagram, the higher you move the more negative you go because these are electronic energies.

So the lower end is positive, the higher end is negative okay. So you can now complete the same thing for valence bandage. Now for this case if you want to draw the band picture in n+

when the positive charge is there, then I must lift this Ec up by the same amount as this because the difference between the conduction bandage in the oxide and the conduction bandage in poly are difference between the conduction bandage in the oxide and the conduction bandage in the substrate.

These differences are decided by the difference in materials. They do not change with bias. So for this case if I want to show, my Ec will go up, this Ec, Ef line would be here. Now since this has moved up, the amount of gate to bulk voltage you have to apply to get this condition is this. So you can see that the gate to bulk voltage has increased now to provide negative charge okay to compensate for this positive charge with increase in the negative direction whatever.

So this is the new flat band voltage including the Fermi level differences in the gate and substrate and the effect of the positive charge. I have not drawn the Ev here, you can draw it to avoid cluttering. The Ev will be exactly Eg below this Ec and Ef. Now this also called flat band condition okay.

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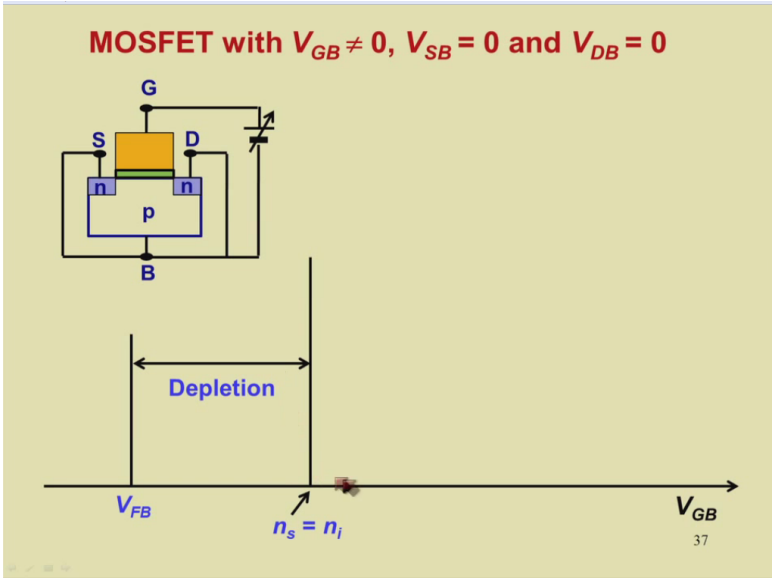

Now that is the condition we have shown here. To the left of the flat band, you have condition called accumulation where there will be positive charge accumulating at the interface. On the other hand, on this side if you go which is of interest to us, you have accumulation of negative charge okay. Now as you increase VGB beyond VFB, we will encounter a state where the surface constant of electrons = ni and the region between VGB=VFB and the value of VGB for which ns=ni is normally referred to as depletion.

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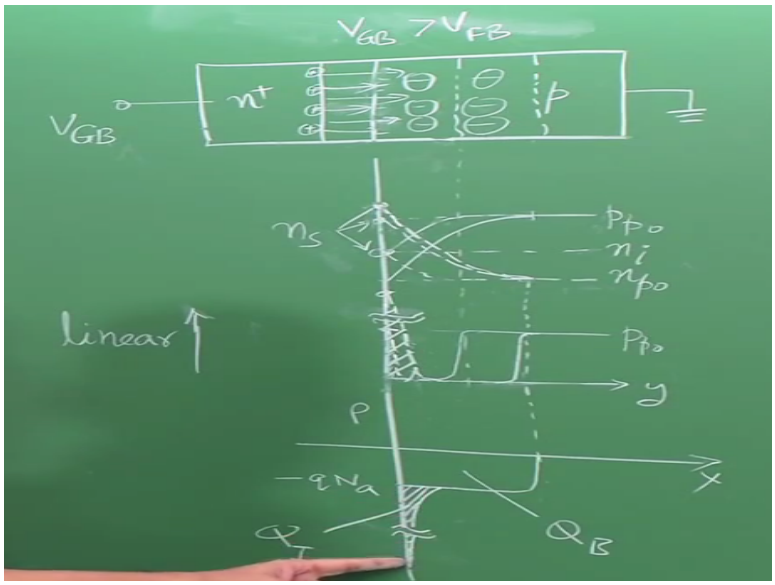

Let us see why? Now let us consider this case because your VGB is more than VFB. So instead of large positive VGB we will say VGB >VFB. Now let us see the condition when you have a small VGB > VFB. Now how do you get the negative charge? So you can drive away holes and attract electrons both. Let us show that. So this is your Pp0, this is your Np0.

For some voltage you have this condition gate voltage. This is ni. We are plotting concentrations on a log scale, so ni is in between Pp0 and Np0 exactly in between on the log scale. This is your ns, surface constant of electrons, so you see what is happening, electrons have been attracted to the surface that is why the concentration is rising, holes are being driven away from the surface so their hole concentration is falling.

So that is the condition, ns=ni for some value of voltage. Now why is this region called depletion? Because you can see here if I were to sketch the same concentration on the linear scale, this is my Pp0 and this is your y axis right, let us say this is this direction. We calling it y because in the diagram here our MOSFET is shown with gate on the top and bulk at the bottom therefore this direction from gate to bulk is vertical and this is y.

So we have plotted Pp0 on the linear scale here this was on the log scale. Note that on the log scale, difference between Pp0 and Np0 is many orders of magnitude. For example, if Pp0 is 10 power 17, Np0 would be 10 power 3. So 17 to 3, 14 orders of magnitude increase in carrier concentration when you go up. Therefore if you move even a little bit, your carrier

concentration would have fallen by a factor of 10 that is on the linear scale it will appear very rapid fall. So let us emphasize this fact and say this is linear.

It is understood that this is log because otherwise I cannot show Pp0 and Np0. Now what about electron concentration? You see ni is of the order of 10 power 10, this is suppose 10 power 17, 10 power 10/10 power 17 is 1/10 power 7. So if I want to show this ns here, concentration here is 10 power 7 times less than this. I really cannot show. So on a linear scale I cannot show this electron concentration.

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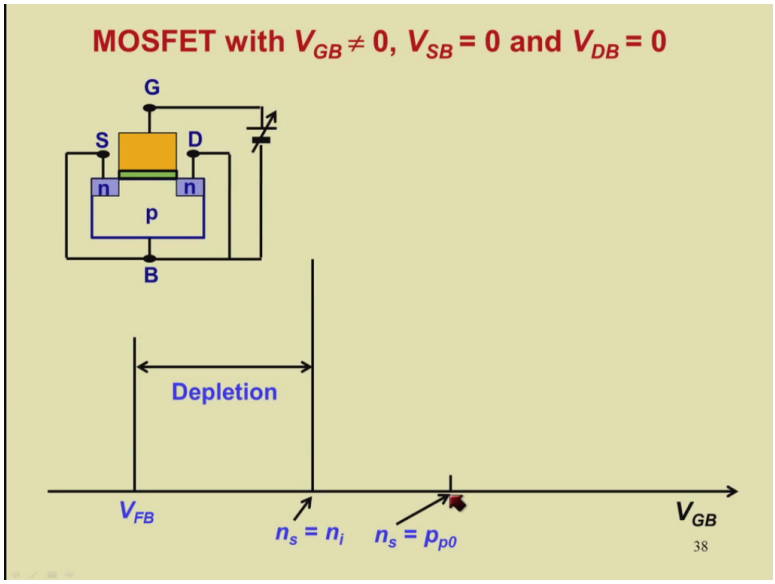

That is why you can see we can regard this region as depleted of both holes and electrons as you can see from here, hole concentration is very small, electron concentration also very small that is why this is the depletion region and that is why this region here is referred to as depletion. Suppose we increase VGB further, we will encounter a situation when the surface concentration becomes = Pp0 that is the concentration of holes in the bulk.

Did I show that here? So this is the case when ns=Pp0. Both these are ns. Now if you try to show this picture here how would it look. Now ns=Pp0 so you have ns, but then once again here this variation in electron concentration is several orders of magnitude even if I move a little bit inside my electron concentration would have fallen by a factor of 10 right because this is 14 orders of magnitude variation and therefore on the linear scale this concentration would look something like this. This is your ns.

So you do not have too many electrons. The whole picture would look something like this. So in other words, your depletion region has expanded. Depletion charge has increased. If I were to show the hole concentration here, it would be like this. So when ns=Pp0 this is your hole concentration, this is your electron concentration, this is the same thing on a linear scale.

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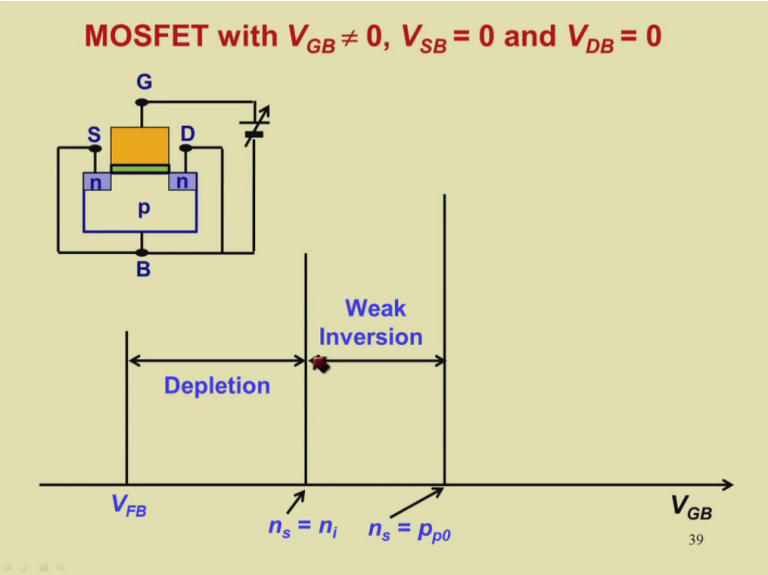

Now this region is referred to as weak inversion region from ns=ni to ns=Pp0. It is inversion because you can see here that once ns becomes more than ni, you can regard the surface to have become more n-type right. Now the interface becoming n-type in a p-type substrate means the surface has got inverted. So inversion starts here. So this inversion, but then if you take the amount of inversion charge you see when you plotted on a linear scale beside that for ns=ni I cannot show the electron concentration at all.

For ns=Pp0 I can show some concentration and this is your inversion charge. However, if I compare this inversion charge that is area under this curve shown by the shaded line with the depletion charge which is equal to this area amount of holes removed, amount of holes depleted that is this area. So this shaded area is very small compared to this area. Therefore, the inversion charge is really very small therefore it is referred to as weak inversion.

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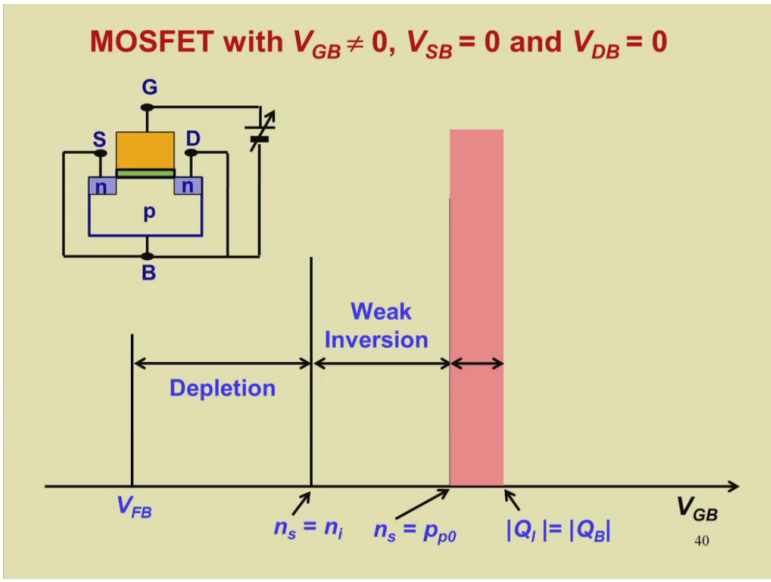

If you increase VGB further, you will encounter a situation where the inversion charge will be equal to the depletion charge. Now let us sketch that here. You increase VGB further, so inversion charge now this in electron concentration will be increased further. It turns out that the depletion charge does not increase much beyond this point. This has been proved by numerical calculations also.

That is why the starting point of this rise in electron concentration is being shown approximately at the same point okay for ns=Pp0 and ns more than Pp0. So for this case, if I were to plot the electron concentration here note that small increase on a log scale means a high increase on a linear scale because this may be even 100 times increase so I really cannot show it to scale because 100 times increase means from here to you know much above

So what I do is I put a break here and then your electron concentration would be something like this on the linear scale. Now this is your ns. Similarly, this is your ns. If I now take the inversion charge for this case that would be this shaded area, which is now quite a bit. For some condition, this shaded area will become equal to the holes depleted that is this area okay. So that is when you say QI=QB. Now let me show that by plotting the space charge.

I will plot the space charge only for this condition when ns is more than Pp0. So this is the depletion charge this is -qNa that is because of this and because of electrons here if I want to show the charge that would be going up like this. Again here I have to show a break because this is really electron concentration is very high compared to this and this is the shaded area.

That is the space charge because of electrons inversion so this is QI, this is QB this region. So we are saying this area is equal to this shaded area that is QI=QB that is the condition. Evidently, here if I want to show this here it would be something like this depletion region has expanded and you will have a large number of electrons coming here so this field will be more you know if you are going to hire an hire voltages for this case and this case if I want to show the conditions here the depletion region will be more and more electrons will come here.

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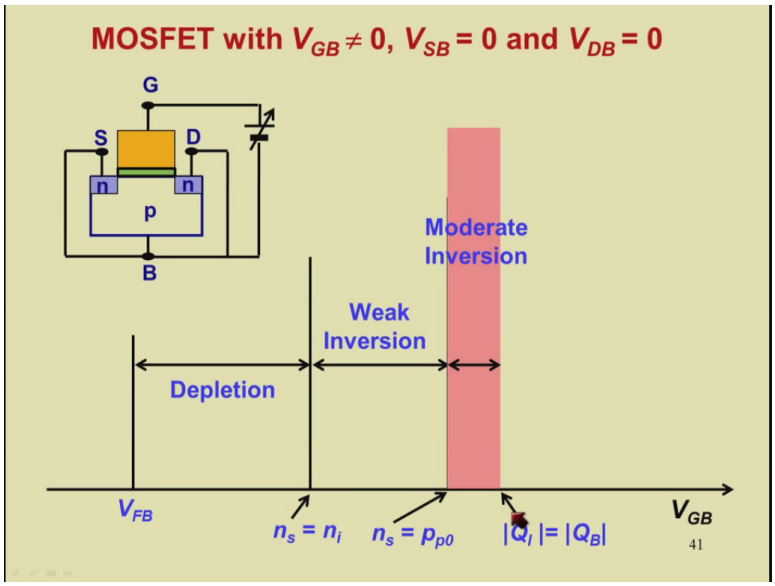

Now region between these 2 points when ns=Pp0 and QI=QB is referred to as the moderate inversion region. Note that this point is expressed in terms of the volume concentration of electrons at the surface whereas this point is expressed in terms of the area concentration of electrons inversion charge okay this is important to note. So ns is the volume concentration of electrons so it is the volume concentration of electrons at a point, but QI is the area under the distribution okay it is an area.

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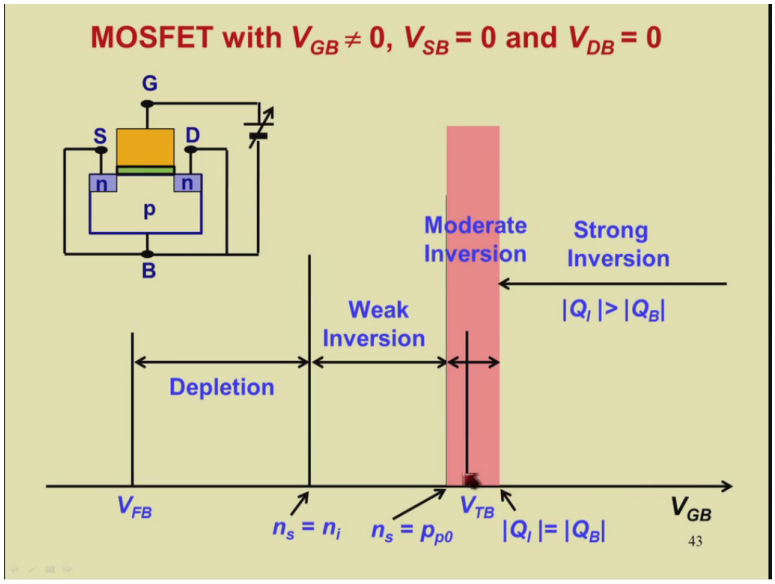

Now this region is called moderate inversion and when QI is more than QB, the range of VGB here is referred to for this range of VGB the device is referred to be in strong inversion because the surface has become strongly n-type as compared to the bulk, which is p-type. In the moderate inversion, you have the voltage called the threshold voltage. Now we are putting a suffix B here because the gate voltage is with respect to bulk.

Let us see what is this threshold voltage? If I plot this inversion charge that is this area shaded area or this area, as a function of the VGB, the picture would look something like this.

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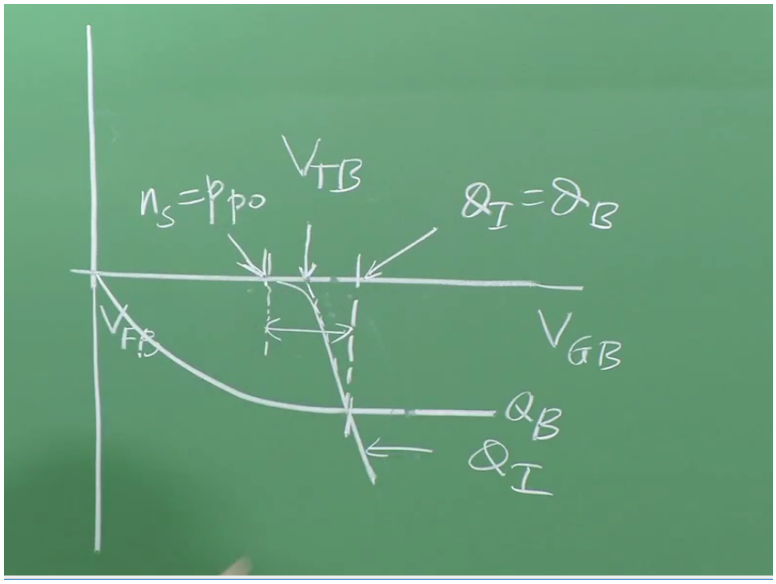

So the inversion charge will be very small for VGB beyond VFB so this is let us say VFB. This point is VFB and beyond some voltage, it will start rising and the rise will have a linear part. If I extrapolate this linear part, so this is QI they are showing on a negative side because

QI is negative. This voltage extrapolated voltage VGB is referred to as the threshold voltage. To see the location of this threshold voltage clearly let me also show the QB variation on the same graph. So this is QB. You can say this is the point where QI and QB are becoming equal. If I were to sketch the condition when ns=Pp0 that is this condition Pp0 the inversion charge is there, but is very, very small that would be somewhere here.

So this condition is ns=Pp0 and this condition is QI=QB. So this is the so called moderate inversion region. So you see that the threshold voltage falls in the moderate inversion region and is located as the gate to bulk voltage obtained by linearly extrapolating the QI versus VGB graph to the VGB axis.

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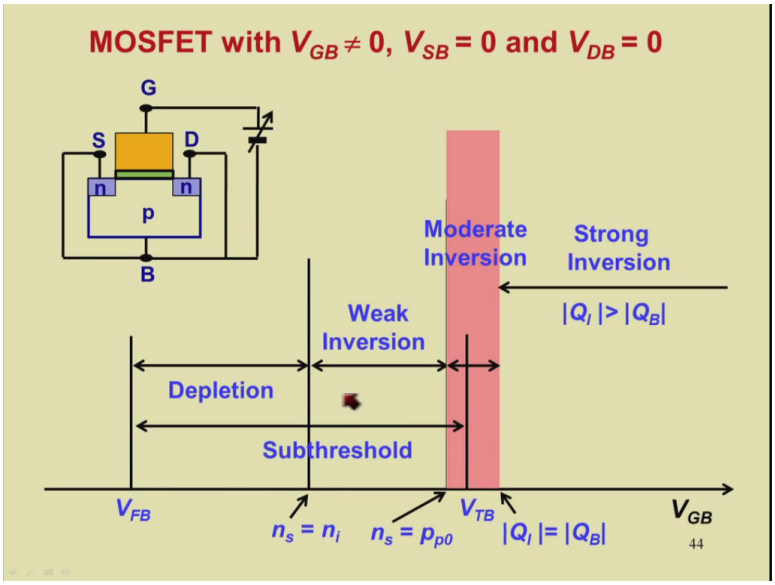

The region from VG=VFB to VG=VTB is referred to as subthreshold that is below threshold. With that we have come to the end of the lecture so let us make a summary of the important points.

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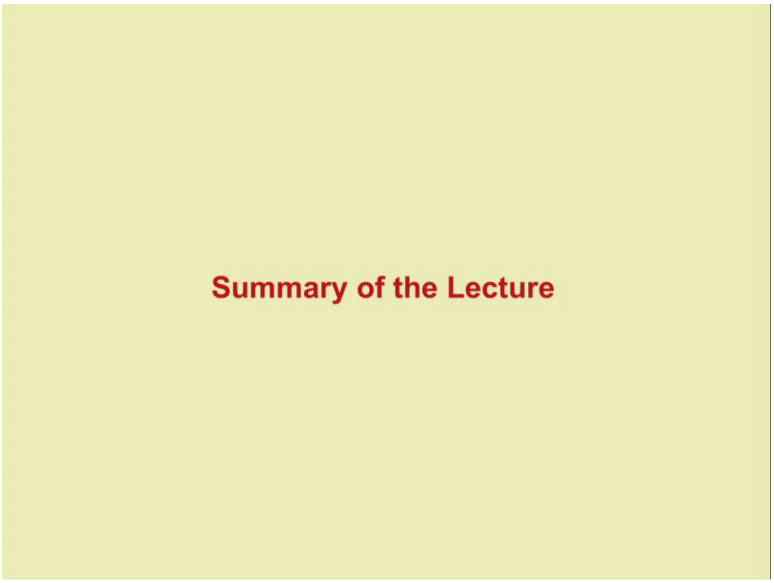

In this lecture, we have begun a discussion of the qualitative theory behind the DC characteristics of a large uniformly doped bulk MOSFET. We remarked that while this device is used with source as a common terminal in a circuit in other words the voltages to the various terminals of the device are applied with respect to the source in a circuit when you want to develop a device model starting from device physics biasing this MOSFET with respect to bulk as a common terminal is more convenient.

Then we said that in practice a MOSFET is biased with 3 voltages. One between drain and source, another voltage between gate and source and at times a voltage between bulk and source. A model for this biasing arrangement is developed starting from the simple case of a MOSFET to which only a bias is applied between gate and bulk, source and drain junctions are shorted to the bulk.

So in effect this becomes a 2 terminal device so we understand the charge conditions in a 2 terminal device. Then we try to understand the charge conditions in an effectively 3 terminal device in which 2 voltages are applied, one between gate and bulk, another one between source and bulk. We assume the drain to bulk voltage to be same as source to bulk voltage.

After understanding the charge conditions in a MOSFET for this situation where you have 2 voltages applied we move to the MOSFET with all the 3 voltages applied. We remarked that in an earlier course called solid state devices, which is available on YouTube we have discussed various charge conditions in a MOSFET and the theory underlying the MOSFET operation at a very fundamental level or level 1 in lectures 33 to 41.

So you are encouraged to go through those lectures before proceeding further. However, for those people who are already somewhat familiar with MOSFET theory what we have done is we summarized in this lecture some key points from this previous course. So that we can move further and develop a more advanced model of the MOSFET. The key points we summarized related to identification of the accumulation, depletion, weak inversion, moderate inversion and strong inversion regions.

So we identified the gate voltages, which help us to delineate these various regions of operation. The important gate to source voltages or rather gate to bulk voltage because we said that we discuss a device with bulk as the common terminal. So we identified important gate to bulk voltages, which help us in delineating the MOSFET regions like depletion, accumulation, inversion and so on.

The important voltages are the flat band voltage and the threshold voltage. In between, you have some other voltages also which we discussed. In the next lecture, we will consider the effect of a bulk to source reverse bias and then discuss the case when you have bulk to source, source to bulk, gate to bulk and drain to bulk voltages.