Semiconductor Device Modeling
Prof. Shreepad Karmalkar
Department of Electrical Engineering
Indian Institute of Technology – Madras

Lecture - 40
MOSFET: Device Structures and Characteristics

In the previous lecture, we began a discussion of modelling of MOSFET. First we briefly mentioned how the MOSFET structure evolved out of a patent which was filed in 1925 and subsequently another version of the patent filed in 1934. We outline the various types of MOSFETs which are available today. So that various MOSFETs which are available today can be classified into n-channel and p-channel devices, and each of this n-channel and p-channel devices can further be classified into surface and buried channel devices.

Further another classification of MOSFETs is in terms of the location of the source, drain and gate. So you can have the planar devices in which the source, drain and gate are all situated on a single plane, or you can have non-planar devices such as the nanowire, gate all around or surrounding gate MOSFETs in which the source, drain and gate are not on the same plane. Next we considered classification of MOSFETs based on the method of isolations.

So we looked at bulk MOSFET and we said that bulk MOSFET can be classified into either an isolation type which is based on a local oxidation or LOCOS or shallow trench isolation. Now the planar MOSFETs can be either bulk MOSFETs or the other variety is the silicon on insulator on SOI MOSFETs. In SOI MOSFETs, you make the various MOSFET devices in islands of silicon deposited over an insulating layer such as that of silicon-di-oxide.

And finally you can classify MOSFETs in terms of their power handling capability. So you can have small signal MOSFETs or power MOSFETs. After describing this classification, we mentioned that in this course we will be focusing on the bulk MOSFET. We discussed the device structure, doping profile and dimensions of a bulk MOSFET realised using shallow trench isolation.

As we have remarked in an earlier lecture on device modelling procedure, there are 9 steps in modelling of a device, in which the first step is the discussion of the structure and characteristics of the device to scale.

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Module 9

MOSFET: Device Structures and Characteristics

- Output characteristics
- Transfer characteristics
- Substrate current characteristics

So in this lecture we shall be looking at the output characteristics, the transfer characteristics and the substrate current characteristics of a bulk MOSFET.

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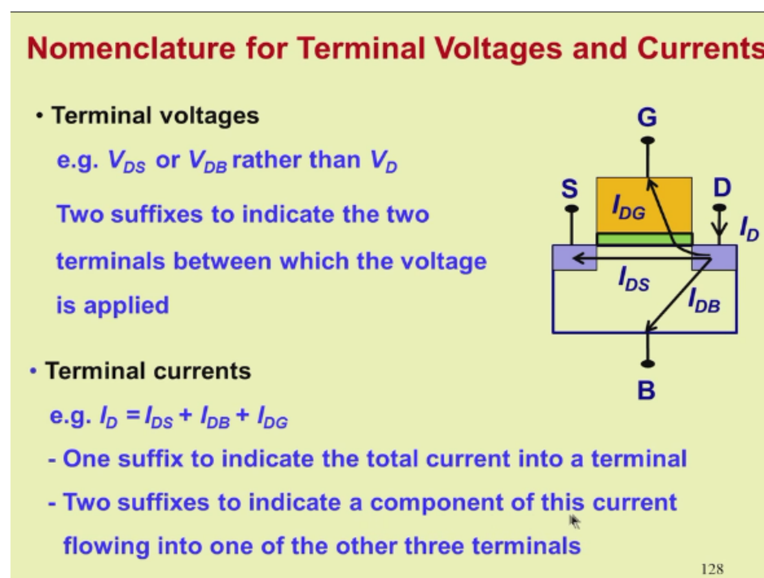

Let us begin by mentioning the nomenclature used for terminal voltages and currents. Here is a schematic of a MOSFET with 4 terminals namely the source, gate, drain and the bulk. A voltage source is always connected between 2 terminals and therefore a symbol for a voltage has 2 suffixes corresponding to the 2 terminals. So in general a terminal voltage will be specified with the symbol V with 2 suffixes representing the 2 terminals.

Note the problem with a single suffix such as V suffix d, V suffix d would imply the voltage of the drain, but it is not clear whether this voltage is with respect to source, gate or bulk. In

other words, the reference terminal is not clear if you have only 1 suffix. So the 2 suffixes indicate the 2 terminals between which the voltage is applied. Let us look at specification of terminal currents.

Here we are specifying the drain current flowing into the drain terminal. So there is only one suffix here representing the particular terminal into which or out of which the current is flowing. You can also have a current specified using 2 suffixes, in which case it would indicate the current flow between 2 terminals. In this case for instance IDG means the current flow between drain and gate, IDS means the current flow between drain and source and IDB means current flow between drain and bulk.

Now this is the relation between the terminal current and the currents between terminals. So for instance, I suffix D = IDS+IDB+IDG. Thus we have 1 suffix to indicate the total current in to a terminal and we have 2 suffixes to indicate a component of this current flowing into one of the other 3 terminals.

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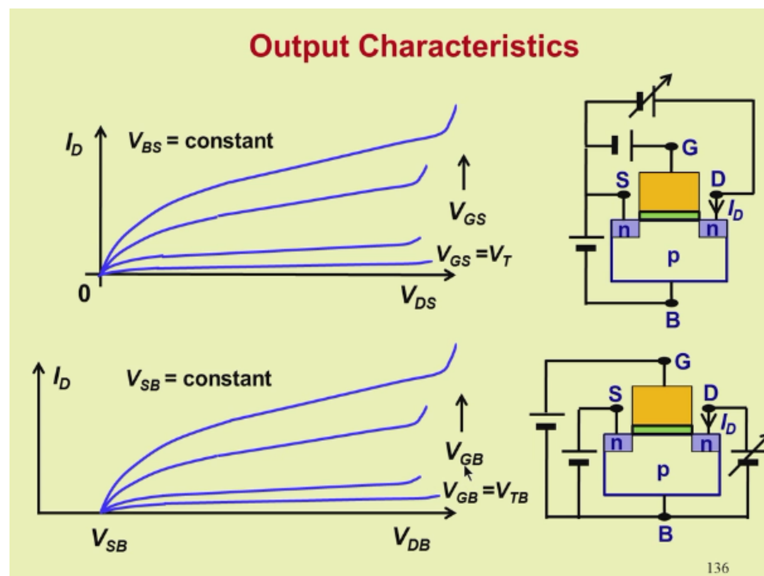

Now let us look at the output characteristics of a MOSFET. Output characteristic indicate the behaviour of the drain current as a function of the drain to source voltage. So you vary the drain to source voltage and see how the drain current varies. The gate to source voltage and bulk to source voltage are kept constant when you want to vary the drain to source voltage. The result is normally plotted in a graph of this form where the y-axis indicates the drain current and the x-axis indicates the drain to source voltage.

VBS is kept constant and VGS is a parameter. In other words, you keep VGS constant and sweep VDS, see how the ID changes, then shift the VGS to another value and repeat the process. For instance, if you maintain the gate, source voltage constant at a value more than the threshold voltage of the device for which a channel is created between source and drain, then when you sweep the drain into source voltage from zero onwards, you get a curve of this type.

So you see that the current rises rapidly in the beginning, but then these rise tappers off until you reach a high value of VDS beyond which it rises rapidly again. For various values of VGS, the ID VDS curve would look something like this. For VGS = threshold voltage you have a very, very small current flow, and for higher values of VGS the current increases. You can also plot output characteristics as ID as a function of the drain to bulk voltage VDB instead of the drain to source voltage VDS.

In other words, we can apply the voltages with respect to the bulk rather than with respect to the source. It turns out that in circuit applications you always use the MOSFET with source as the common terminal whereas when you want to develop a model for the MOSFET from device physics, it turns out that if you use bulk as the common terminal and apply the various voltages with respect to the bulk the analysis of the device becomes simple.

The reason for that is the inherent symmetry of the device with respect to the bulk, for instance you can see that I can interchange the source and drain. Now let us see how the ID VDS characteristics look like when you plot them as ID versus VDB. Now in this case the source voltage with respect to bulk would be kept constant. Similarly, the gate voltage with respect to bulk will be kept constant when you are sweeping the drain to bulk voltage.

Now the smallest value of drain to bulk voltage, you will start with would be VSB, that is the voltage that you are maintaining constant. For VDB =VSB the drain and source are at the same potential and therefore there is no current flow between drain and source. That is why your drain current is zero here. Now you might say that will there not be a current between drain and gate or between drain and bulk, what about these components.

Right now we are regarding these components to be very, very small and we are mostly concentrated to the drain to source current. And therefore the terminal current is the same as

drain to source current. So when VDB = VSB, the drain current is zero. And thereafter as VDB is increased the current rises and the behaviour here is same as the behaviour considered for ID VDS characteristics.

The only difference here is that the threshold voltage with respect to bulk is in general different from the threshold voltage with respect to source. Normally the threshold voltage with respect to source is represented using the symbol V suffix T. You do not put the source here, in the symbolism. So whenever you come across the symbol V suffix T from threshold voltage it is to be understood that it is with respect to source.

When you are talking about the threshold voltage with respect to bulk then you introduce the symbol B here to specify that you are regarding the threshold voltage with respect to bulk. So for VGB = VTB you have very, very small current flowing and as you increase your VGB you currents increase.

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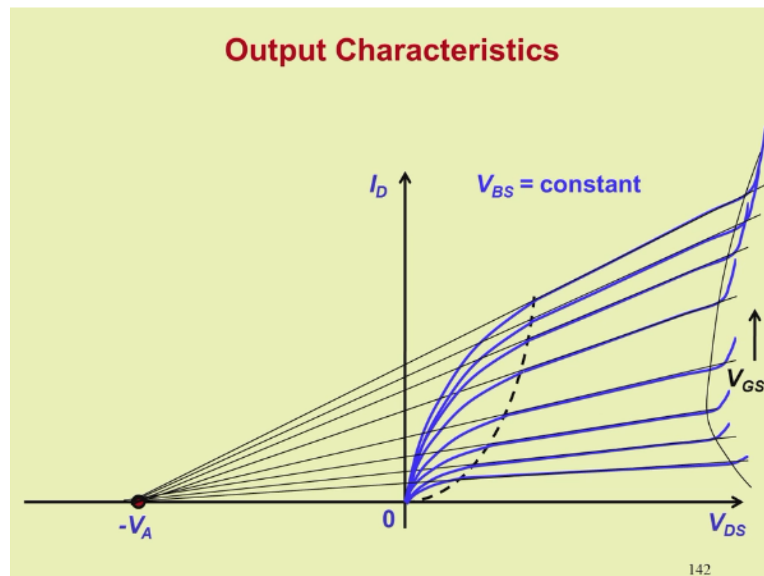

Let us look at some of the finer aspects of the ID VDS or output characteristics. You can divide these characteristics into 3 regions broadly. In this region towards the left of the dotted line the current rises relatively rapidly. In the region between this dotted line and the solid line here, the rise is tapering off a little bit and beyond the solid line you have a very rapid rise in current.

Now these 3 regions are normally represented or called following name, the region to the left of the dotted line is referred to as non-saturation region. The region between the dotted line

and the solid line is called saturation region because the characteristics tend to appear to be saturating here. And the characteristics to the right of the solid line are referred to as the breakdown region, because here the current rises very rapidly, there is a breakdown between drain and bulk.

The drain to bulk junction is breaking down which is responsible for the rapid rise in drain current. If you extrapolate the current in the saturation region back to the VDS axis, it is interesting to note that all this extrapolated lines seem to emanate from a common point. This point is referred to as the early voltage denoted by the symbol V suffix A. There is a negative sign here because this voltage is negative.

Let us clean up the slide little bit and look at the increments in the current. The increments in the drain current for equal increments in gate to source voltage. It is clear that for equal increments in gate to source voltage the increment in drain current is small for small values of VGS it increases progressively and then for high values of VGS the increments again go on decreasing.

There are various phenomena which are responsible for this kind of a behaviour, which we will be looking into. At this point, we are highlighting the important features which need to be captured in our device modelling.

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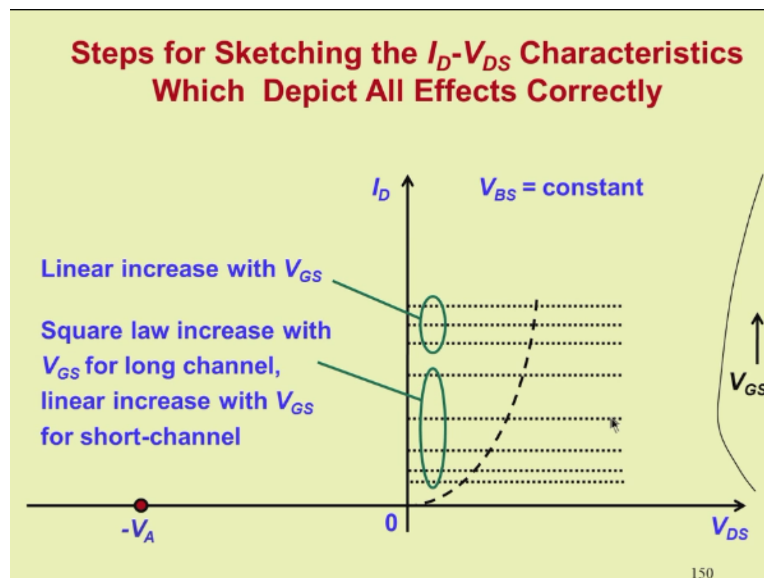

Now it is important to know what are the steps in sketching the ID VDS characteristics in such a way that the various effects that we just now spoke about can be depicted correctly.

Now generally it is found that students would not pay much attention to the finer nuances of the MOSFET characteristics, when asked to sketch the output characteristics would do something like this.

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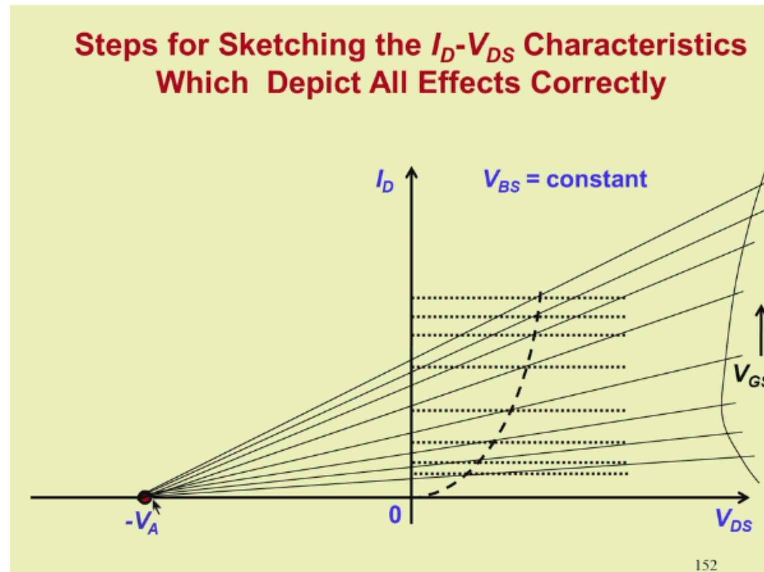

This is ID and this is VDS, and they would sketch the output current something like this. Now note here it is not clear what is happening to the slopes of this current in this region, right, is the slope increasing as you increase your VDS decreasing or remaining same it is not clear. Further it is not clear which is the region in which the characteristics increase rapidly for low VDS and which is the so called saturation region.

Similarly breakdown region is not shown at all. Now for this reasons, let us lay out the sequence of steps in which you must sketch the output characteristics of a MOSFET. The way to go about doing it as follows. First draw the VDS axis and the ID axis and leave sufficient space on the negative as well as positive side for the VDS. Then you mark the non-saturation, saturation and breakdown regions using these boundaries.

The boundaries will be as shown the breakdown voltage is high for low values of VGS and it decreases and then for high values of VGS it tends to increase again, reasons for which we will discuss later. The locus of the point at which the current tends to saturate it goes on increasing, right as shown here. Next let us clean up the slide little bit, and sketch the current in saturation.

So here we are showing the current in saturation by horizontal line which is not the way the actual current would be, but these horizontal lines drawn here tell you the increments in the drain current in the saturation. They are not the lines corresponding to the saturation current itself, so they should be viewed as indicating the increments in the drain current in the saturation.

So as we have remarked the increments are small to begin with then they increase and then they decrease, there can be some variations in these increments. Now it is important to note that these increments in current are shown for equal increment in VGS. Now generally in this region, you find a square law increase of the drain current with VGS if the device is a long channel device.

That is if the distance between the drain and source is large, then it is a long channel device, the channel length is large. On the other hand, the increase is linear with VGS if it is a short channel device, if the channel length is small. So for a short channel device, you will not see the increase in this spacing as shown here. The incrementing current would be more or less equal for equal increments in VGS.

For high VGS you generally have whether long or short channel device a linear increase in VGS in other word the increment in drain current is more or less uniform for equal increments in VGS. Next you sketch the early voltage on the negative axis from which all the current lines in the saturation region would appear to emanate. Let us clean up the slide and then draw straight lines joining the early voltage to the point of intersection of the horizontal lines with the locus separating the non-saturation and saturation region.

Now using these lines you can sketch the current voltage characteristics as follows. For one value of VGS for instance, for highest value of VGS shown here, you can draw the non-saturation region characteristics as follows. You join the origin to this point using a line which is curved like this, because ultimately the current should tend to saturate or the rise should taper off, so that is why the shape of the curve is this way.

Then you extend it as a straight line which falls on the same straight line which is drawn from the early voltage point to this point of intersection of the horizontal line and this locus separating the saturation and non-saturation region. And once you enter the breakdown region

your current should rise rapidly. You can repeat such line for all the other cases, and your picture would look something like this.

Now if you remove the lines used for construction namely the horizontal lines and the straight lines emanating from the early voltage, you are left with the output characteristic showing the drain current as a function of the drain to source voltage for equal increments in VGS. Now these characteristics contain the various features depicted correctly. So let me do that exercise once more for you on the board.

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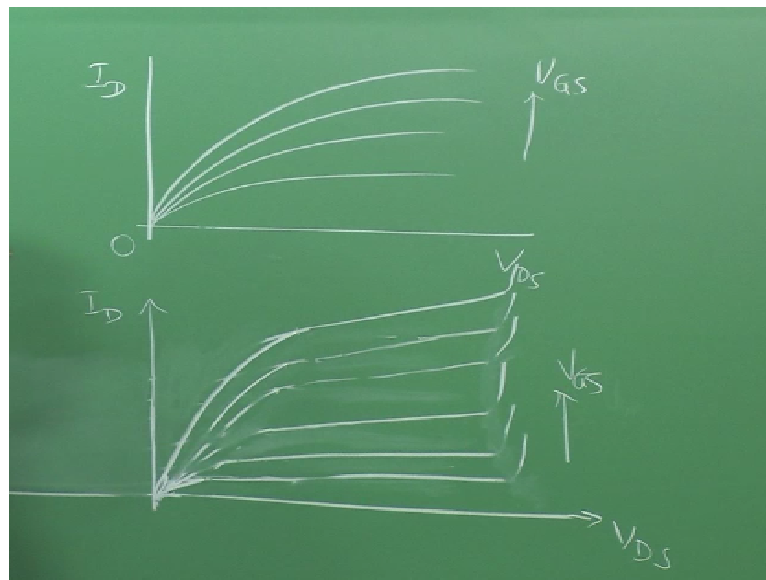

So instead of drawing the characteristics the way students normally draw it, here this is origin the way to go about doing is as follows. So you draw ID VDS, you draw the locus separating non-saturation and saturation regions and breakdown region, then you show the lines, horizontal lines correspond to equal increment in VGS. So they show the current increments for example, maybe long channel device so your increments in currents go on increasing with voltage and then ultimately the increments taper off for high VGS.

Then you locate the early voltage here and then you join this voltage to the lines like this. So this should be drawn as straight lines, and here your currents increase, because you are entering breakdown. So now you can join this to complete the non-saturation portion and if you rub off all these lines, then you are left with the current voltage characteristics with all features depicted correctly. So this is your diagram for ID VDS current with VGS as the parameter.

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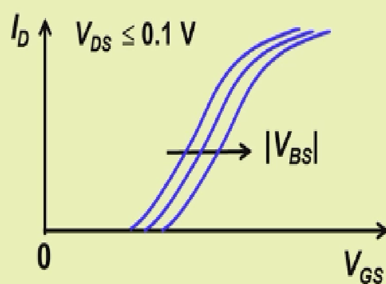
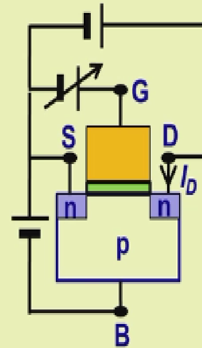
Transfer Characteristics





Now let us look at what are called the transfer characteristics. In this case again you are plotting the drain current, however this time the drain current is varied using the gate source voltage, rather than the drain source voltage. The drain source voltage and bulk to source voltage, they are kept constant. So this is your map. ID is a y-axis and VGS is x-axis. Generally the drain to source voltage is maintained at a very small value < about 0.1 volt keep the VBS constant at some value and sweep your VGS to get a curve something like this.

This point here indicates the threshold, so beyond threshold voltage when your VGS increases beyond threshold voltage your current rises, below that the current is really very, very small. If you increase your VBS your threshold voltage shift to the right and so you get curves which are shifting to the right as your VGS increases.

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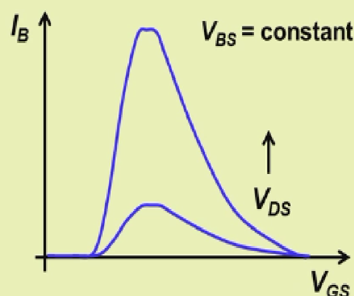
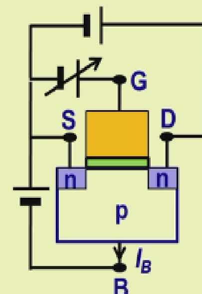
Substrate Current Characteristics





Device operating in saturation region near breakdown

Next let us consider the substrate current characteristics. So in this case again you are varying the VGS keeping VDS, VBS constant and monitoring the current through the bulk terminal, that is the current IB. In an n-channel MOSFET the current IB flows out. This is not difficult to understand, because suppose for example you consider the reverse bias current between the drain to bulk junction, n-p junction, this drain is positive and therefore the reverse bias current would flow from n to p and it will come out.

So that is how you get this direction of the IB. Now the IB is not merely the reverse bias current between the drain and bulk as we will see this current results from the channel region also. Right now, let us plot the characteristics, we shall explain the characteristics later. Generally the substrate current characteristics are considered for device operating the saturation region near breakdown, which means that your device is operating near this point.

These are breakdown points, because only for that condition the saturation current is significant. This is IB versus VGS map, VBS is kept constant, and you fix your value of VDS and then sweep VGS. So here VDS is a parameter, then you change to another value of VDS and again sweep your VGS. So the current behaviour is something like this.

The current is very, very small up to some value of VGS and beyond this VGS once the channel is created your current rises reaches a peak and then for higher values of VGS the current again falls back to very small value. If your VDS is increased the bulk current increases as shown here. As we have said, we are right now not explaining how this kind of a behaviour arises.

We are only pointing out the variations that takes place, and we shall be explaining the variations later. Now let us set out a strategy to model a modern bulk MOSFET. A modern bulk MOSFET is a device of a small size with considerable variations in locations of the dopant atoms, so dopant atoms are randomly located.

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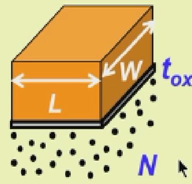
A Strategy to Model a Modern Bulk MOSFET



Modern bulk MOSFET is characterized by

small L, W, thin t_{ox} and randomly located dopants (N)

The condition in a modern MOSFET is depicted using this diagram. Note that we are only showing the essential features here and this is a schematic showing the important aspects, which needs to be considered while modelling a modern MOSFET. A modern bulk MOSFET is characterised by small values of L and W, that is the channel length is small and W is also small.

And thin T-ox the oxide is very thin of the order of nanometers, and randomly located dopants. So you can see the location of the dopant atoms is random, the dopant atoms are not located at uniform positions. Now the way to model this device would be as follows.

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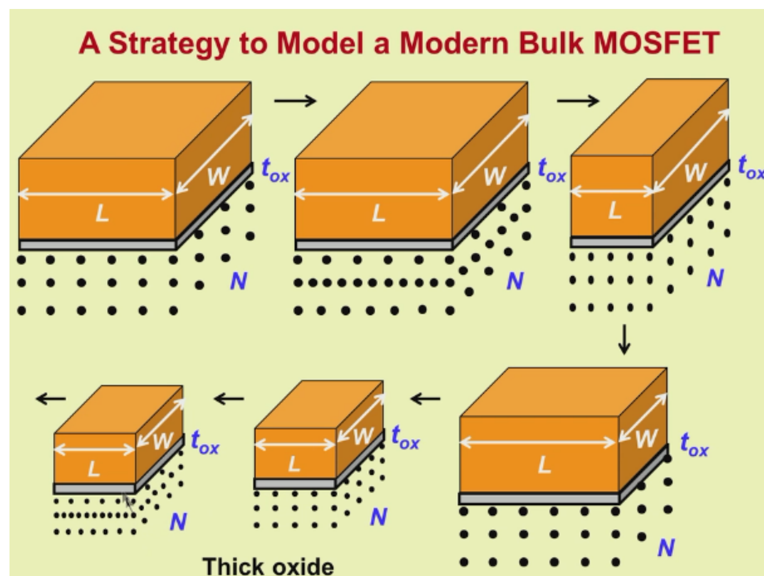

First we model a large bulk MOSFET with thick oxide. So we start with a device where L is large W is large, T-ox is large and the dopant arrangement is very regular. Next we consider a

MOSFET in which L, W, T-ox are large, but the dopant arrangement is such that your doping is non-uniform in vertical direction and may be even in horizontal direction. So for instance here doping is low at the interface it increases reaches a peak and then as you move down it decreases further.

Then you consider a device with a short channel. W and T-ox remain large and the doping remains uniform, following this you model a device using a narrow width, W is small, L and T-ox are large and doping is uniform. You can then combine your understanding of short channel and narrow width devices and model a small geometry device the oxide still remains thick, but L and W are small and doping is uniform.

Next stage you consider the case of a non-uniform doping with small L and W but T-ox large. Following this set of devices are these set of structures, we move on to structures with thin oxide. So we start with a MOSFET having a thin oxide but large L and W and uniform doping. Next we change only the doping of the substrate to non-uniform and model the device.

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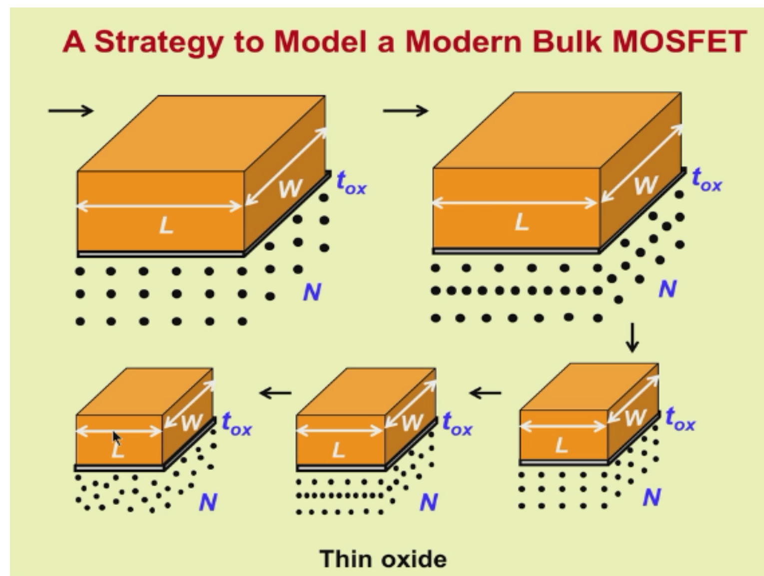

Next we consider a small geometry MOSFET with thin oxide but uniform doping. Then we consider a small geometry MOSFET with thin oxide and non-uniform doping. And finally we arrive at a modern MOSFET which has small geometry, that is small L and W, thin oxide and randomly located dopants. So this is the strategy for modelling a modern bulk MOSFET. So the starting point of modelling a bulk MOSFET is a device with large L and W, reasonably thick oxide and uniform doping. This is what we are going to begin within our course.

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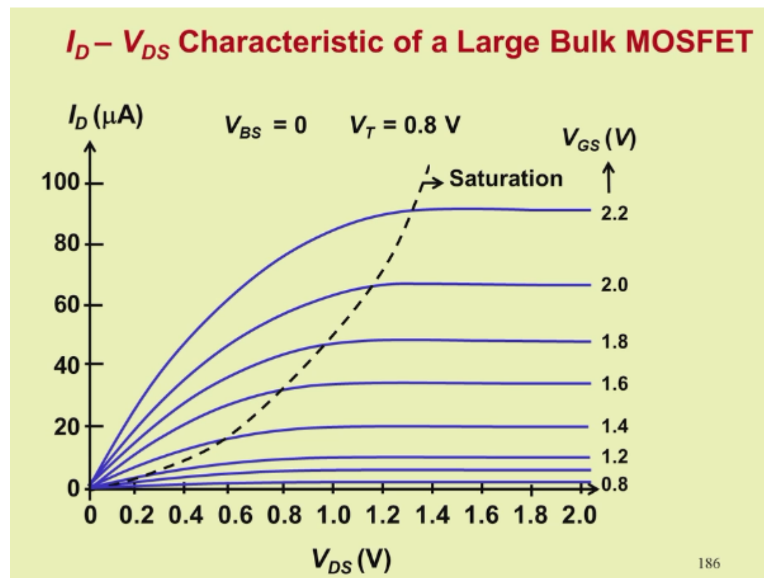

So let us consider the ID VDS characteristics of a large bulk MOSFET. Now you recall, we have said that we must look at the characteristic to scale. So we must have an idea of the magnitudes of voltages and currents involved, that is why these characteristics are shown with values of current and voltages mapped here. We are showing the characteristics for zero VBS. These ID VDS characteristics are nothing but the output characteristics.

The VGS as a parameter you can see here we are trying to make equal increments in VGS. Now except for the value shown here which is 0.8 volts which corresponds to the threshold voltage of the device, you can see that the increment is 0.2 volt, starting from 1.2 volts, so 1.2, 1.4, 1.6, 1.8, 2 and 2.2. The currents are of the order of tens of micro amperes and the voltages, drain to source voltage is a few volts maximum.

Now let us separate the saturation and non-saturation regions, this is how the curve for the ID VDS characteristic look like. For a large bulk MOSFET, you find that in the saturation region the slope of the current voltage characteristic is really very, very small. The characteristic look almost flat. That is the sign of a large device. Further you can see that the increments in the drain current, for equal increments in gate to source voltage are increasing as increase the gate to source voltage, over the range considered.

Let us sketch the same ID VDS characteristics in which the drain current is plotted on a large scale, the gate to source, the drain to source voltage axis remains for a linear scale. But the drain current alone is plotted on a large scale. The reason for this is that when you consider

the drain current on linear axis for gate to source voltage less than threshold voltage your currents are so small that you cannot show the behaviour.

So if you want to expand the region of operation below the gate to source voltage = threshold voltage point, then the plotting of the current on the large scale helps. Now the locus separating the saturation and non-saturation regions in the linear scale looks something like this, as we had seen in the previous graph, the same locus when ID is plotted on the log scale, looks something like this.

A line, which appears like this on a linear plot looks like this, when the y axis is changed to log. Now in the linear plot, the region below VT was not evident at all. Now that region is evident here. These are the currents, very, very small currents, which corresponds to gate source voltage below VT. So you find here that the locus separating the saturation and non-saturation regions is almost a vertical line around VDS = 3 times the thermal voltage.

Let us remove the locus corresponding to the linear graph and then show the characteristics. Now these are the characteristics beyond VGS = 0.8, which is the threshold voltage. Now we have plotted the current on a log plot mainly to see the region below 0.8. Let us see how that looks like.

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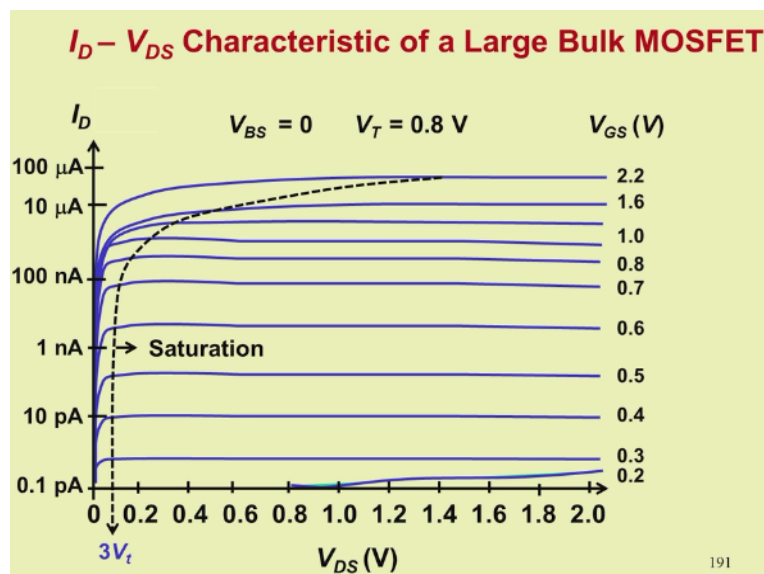

So you find here that for equal increments in VGS, for example here the increment is 0.1 volt, 0.3, 0.4, 0.5, 0.6 and so on starting from 0.2. When the ID is on a log plot, the increments in ID on the log plot appear to be uniform for uniform increment in VGS. For VGS < 0.8. Now

this means that the ID versus VGS behaviour, for VGS < VT is exponential. Because an exponential behaviour when you take log, would appear to be equal increments in ID for equal increments in VGS.

So that is the important thing that comes out of this graph. Now let us look at ID VGS characteristics of a large bulk MOSFET. These are the transfer characteristics.

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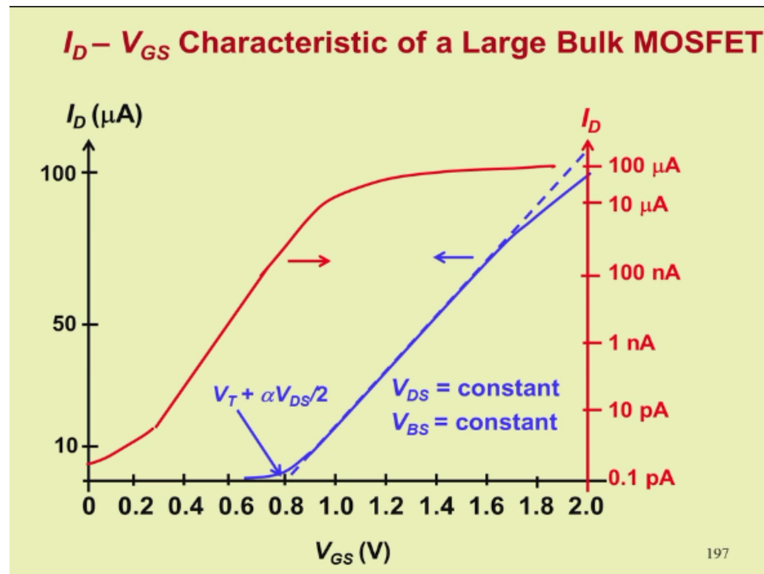

First let us sketch the ID VGS characteristics with ID on a linear scale. So recall your maximum current in the drain terminal was about 100 microns. Now this is what the behaviour looks like, threshold voltage is about 0.8 here. The current increases linearly in the beginning and then the increase seems to taper off a little bit for higher values of VGS. Similarly near VT and below VT, you have the current decreasing along a shape, which looks somewhat exponential.

Now this part of the behaviour can be expanded if you plot the ID on a log scale, which is what we will do later. Now, let us emphasize the point that if you extrapolate the linear part of this ID VGS curve to the VGS axis, the voltage you get here would be the threshold voltage + a contribution from the VDS. Alpha is fraction.

When we write the expression for the drain current, it will be clear, how you get this factor. Now since we generally plot ID VGS graph for very small values of VDS, for VDS values such as 100 millivolts or 50 millivolts, this contribution is really very, very small. So roughly

we could say that linear part of the ID VGS curve when extrapolated to the VGS axis represents the threshold voltage.

Now let us replot the same graph with ID on a log scale, because we want to emphasize the small current region. So you can see from here that on a semi-log plot, the ID versus VGS appears like a straight line for gate source voltages less than threshold voltage. This again points to the exponential relation between drain current and gate to source voltage for gate source voltage less than threshold voltage.

Now this is how you get insights into the behaviour of the current as a function of voltage by plotting the current voltage characteristics on both linear as well as semi-log plots. These insights will then help you to derive a proper model for the device current in the various regions of device operation. It is important to look at all these features of the graphs, the slopes of the curves and so on to get a good qualitative understanding of what is happening in the device.

If you increase your VDS, then your current increases both for high VGS as well as for low values of VGS. This region is as we will see the region where you have leakage currents flowing.

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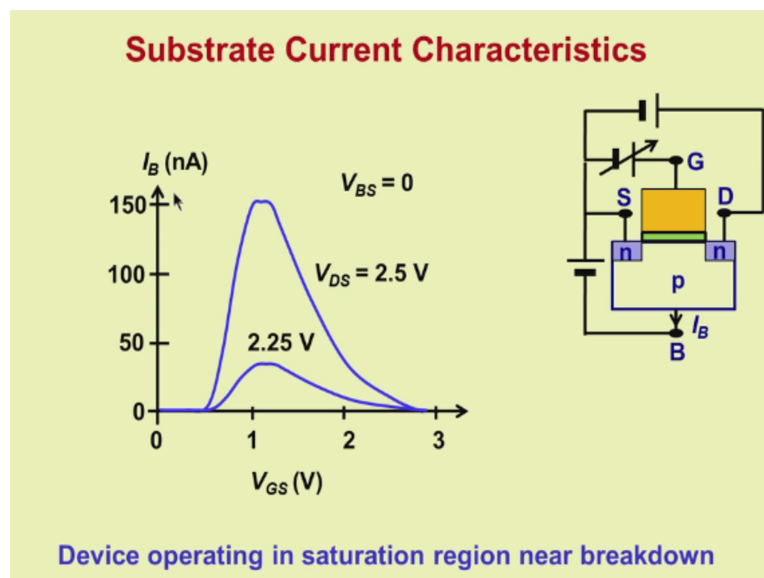

Now let us look at the substrate current characteristics of a large bulk MOSFET. What are the magnitudes of the currents and voltages involved? This is a biasing arrangement in which the substrate current characteristics are measured. So you are plotting this current ID as a

function of VGS keeping VDS and VBS constant. The shape of the curve was introduced to you already for various values of VDS.

From this graph, you can see that the substrate current or the bulk current, I suffix B, here B stands for bulk, is of the order of tens of nanoamperes going upto about 150 nanoamperes.

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Now with that we have come to the end of the lecture and also end of this module on structures and characteristics of MOSFET. So let us make a summary of the important points. So in this module, we first stated the evolution of the MOSFET, starting from an idea introduced in a patent, then we discussed about the various types of MOSFETs, which are available in modern times.

We decided to focus on the bulk MOSFET for modelling. In an earlier module, we had introduced 9 steps in which the module for any device is derived.

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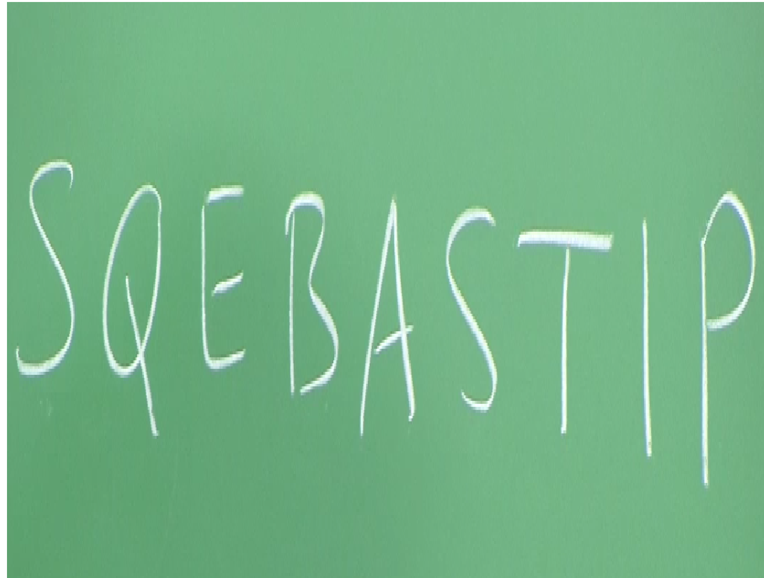

These 9 steps are S, Q, E, B, A, S, T, I, P, structure and characteristics to scale, qualitative understanding, equations, boundary conditions, approximations, solution of the equations, testing of the solution, improvement of the solution and parameter extraction. So in this module, we discussed the first step namely the structure and characteristics to scale for a bulk MOSFET. In the present lecture, we described the various nuances of these characteristics.

So we said that you can identify what are called output characteristics, transfer characteristics and substrate current characteristics for a bulk MOSFET. The output characteristics are the behaviour of the drain current as a function of drain to source or drain to bulk voltage. If you are plotting as a function of drain to source voltage, then the bulk to source voltage and gate to source voltage are kept constant when you sweep the drain to source voltage.

So ID VDS characteristics with VGS as a parameter and VBS maintained constant is a way of representing the output characteristics. Another way of representing the output characteristics is ID as a function of VDB with VGB as parameter and VSB maintained constant. We remark that in circuit applications, the MOSFET terminals drain, gate and bulk, voltages to these terminals are applied with respect to source.

So the source is taken as the common terminal for application of voltages to the MOSFET. Whereas when you want to derive a device model from device physics, the analysis of the device becomes simple if you look at the MOSFET with bulk as the common terminal and apply various voltages with respect to bulk, because this approach exploits the inherent symmetry in the MOSFET.

The drain and source terminals of a MOSFET can be interchanged. After talking about the output characteristics, we talked about the transfer characteristics. Transfer characteristics are nothing but the behaviour of the drain current as a function of the gate to source voltage with drain to source voltage maintained constant usually at a very small value and bulk to source voltage is used as a parameter.

So we increase the reverse bias between the bulk and source, then the threshold voltage increases and your ID VGS characteristics shift to the right. Then we talked about the substrate current characteristics in which we plot the current through the bulk terminal as a function of the gate to source voltage with VDS as a parameter and VBS maintained constant. It is important to state that we laid out a step by step procedure for plotting the output characteristics correctly showing the various features.

It is necessary that students commit this step by step to memory so that whenever they draw the output characteristics, all features of the ID VDS curves are shown correctly. Finally, for a large bulk MOSFET, we gave specific examples of output characteristics, transfer characteristics and substrate current characteristics to give you an idea of the magnitudes of the currents and voltages involved.

For example, for the characteristics that we discussed, the maximum drain current was 100 microamperes. The maximum drain to source voltage was about 2 volts, gate to source voltage was also about 2 volts. In other words, the supply voltage for the MOSFETs for which we showed the characteristics was about 2 volts. Further in the saturation region, for large bulk MOSFETs, the current almost shows a flat behaviour with drain to source voltage.

The slope of the ID VDS curve in the saturation region for a large bulk MOSFET is small. The order of magnitude of the substrate current in our graphs was more than about 100 nanoamperes. So that is the order of magnitude of the substrate current. Now with this, let us list out again the learning outcomes of this module.

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Module 9

MOSFET: Device Structures and Characteristics

At the end of this module, you should be able to do the following for a modern **bulk** MOSFET

- sketch the cross-section, top view and 3D view of the device
- state the key fabrication steps and values of structural parameters
- sketch the output, transfer and substrate current characteristics

At the end of this module, hopefully you should be able to describe the evolution of the MOSFET, state the classification of MOSFETs based on their structures. You should be able to do the following for a modern bulk MOSFET. Sketch the cross section, top view, and 3D view of the device, state the key fabrication steps and values of structural parameters, sketch the output transfer and substrate current characteristics.