Semiconductor Device Modeling
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Lecture - 39
MOSFET: Device Structures and Characteristics

In this module, we start the discussion of modelling of the MOSFET.

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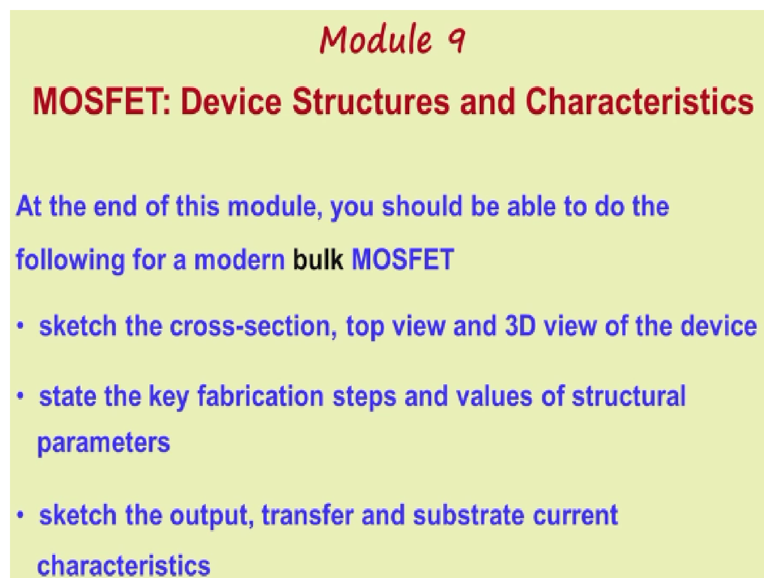

At the end of this module, you should be able to describe the evolution of the MOSFET, state the classification of the MOSFETs based on their structures. Then you should be able to do the following for a modern bulk MOSFET, sketch the cross-section, top view and 3D view of the device. State the key fabrication steps and values of structural parameters. And finally sketch the output, transfer and substrate current characteristics.

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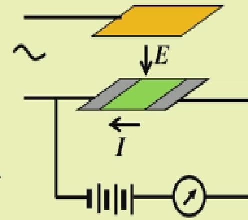
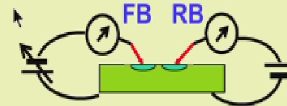
Evolution of the MOSFET

- 1925, 1934 Patents on the concept of a Solid-state or Field-effect Triode by Lilienfield, Heil

  e.g. figure in Heil's patent →



- 1948 Discovery of the BJT by Bardeen, Brattain, Shockley



Let us begin with an evolution of the MOSFET, the MOSFET has evolved over a few decades of time. Let us see the important events in this evolution. In 1925 and then in 1934 patents on the concept of a solid-state or field-effect triode where filed by Lilienfield and Heil. Their idea was as follows, here is a figure from Heil's patent, take a bar of semiconductor and connect a power source to it, you will have a current flowing through this bar.

Bring an electrode close through this semiconductor bar, so that by applying a voltage between this electrode and this semiconductor bar you can modulate the electric field between the 2, just as it happens in a parallel plate capacitor and this electric field in turn controls the charge carriers in the semiconductor bar. So when you vary the voltage here the charge carriers in the semiconductor bar will undergo variation.

And therefore this current would also undergo variation. In this manner you are able to control the current between these 2 terminals using a varying voltage between these 2 terminals. In simple terms, we are controlling the current by a transfers electric field, this was the concept of solid state or field effect triode. Now after this idea was introduced as a replacement for the vacuum tube triode, which was prevalent at that time people started realising this idea in practice.

So you know the vacuum tubes where big in size and the vacuum could only be created in a glass bulb. So the entire structure was brittle also heat dissipation was an issue and reliability was also an issue. Therefore, people were trying to realise this vacuum tube in a solid state,

and this particular structure shown here was considered as an analogue of the vacuum tube in solid state.

Now when people started realising this idea in practice, they encountered lot of difficulties and they were trying to overcome these difficulties through a number of scientific investigations and studies. While doing so accidently in 1948, the scientist Bardeen, Brattain, Shockley discovered what is called the bipolar junction transistor action. What the scientists were doing is trying to study the surface of semiconductors.

Because when people try to realise this idea in practice they found that they were not able to get much modulation of this current by this voltage. And they believe that is because of a poor surface of the semiconductor, the electric field that was impinging on the semiconductor was not able to control the charge carriers there. So trying to study the surface phenomena, these scientists made 2 junctions side by side.

And one of the junctions was forward biased using a power source while the other junction was reverse biased for some studies. They found during the study that if the current in the forward bi-junction was modulated by varying the voltage source here. The current in the reverse bi-junction which was placed nearby was also getting modulated. Now they realised that this kind of a structure is actually what can do amplification.

So in place of this original idea of the field effect triode they decided to use this particular idea of a bipolar junction transistor and make amplifiers using this. So they abandoned the original effort of realising this field effect triode using semiconductors and instead started perfecting this bipolar junction transistor.

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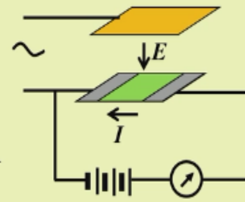
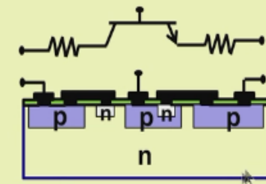
Evolution of the MOSFET

- **1925, 1934** Patents on the concept of a Solid-state or Field-effect Triode by Lilienfield, Heil

  e.g. figure in Heil's patent →



- **1960** Invention of the IC by Kilby and Noyce



In 1960, Kilby and Noyce invented what is called the integrated circuit, where the idea was to put together the bipolar transistor that was being used for building amplifiers and resistor and so on the other parts of the circuit all on a single substrate. So here we show the example of a structure in which you have a bipolar transistor in series with 2 resistors, realised on a substrate, this p region gives you this resistance.

This p region here gives you this resistance and this is an npn bipolar transistor shown here. The top view of the circuit was something like this. This photograph is taken from a website that is, whose details are all given here. Now after the invention of the integrated circuit it was realised that, the original idea of the field effect triode, a device made based on this idea would be more suitable for used in integrated circuit than the bipolar junction transistor.

And therefore people reverted back to the field effect triode. In a very short time, because of the amount of knowledge that was gained about semiconductor surfaces and so on, while studying the bipolar junction transistor and some of the other things, the MOSFET could be realised very quickly by Kahng and Atalla.

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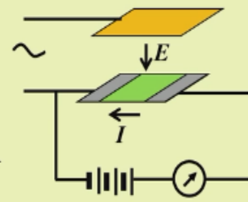
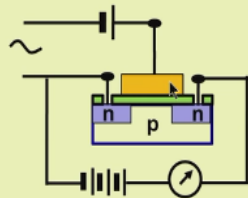
Evolution of the MOSFET

- 1925, 1934 Patents on the concept of a Solid-state or Field-effect Triode by Lilienfield, Heil

  e.g. figure in Heil's patent →



- 1960 Fabrication of the first MOSFET by Kahng and Atalla



They fabricated the first MOSFET whose structure was something like this one can see the analog of this analogy between this structure and the original idea which is given in the patent. This electrode here is realised using this region, which is either polysilicon or metal. The distance between the metal electrode and the semiconductor bar is filled with an insulator that is a silicon-di-oxide here.

This p region is a semiconductor bar and these 2 n regions are the 2 contacts shown here. The voltage applied to the gate creates an inversion layer of electrons, for example if you apply positive voltage to the gate, it will attract electrons from the p-type substrate towards the channel or the interface and this layer of electrons would then allow a current flow between the 2 n contacts.

And the current flow between the 2 n contacts can be modulated by modulating the electric field from the gate by varying the voltage here. A top view of this structure that was realised is shown here. This is the source and this is the drain or you could regard right end as the source, left end as the drain, you see that this is a symmetric structure, and this is the gate, once again this photograph is taken from the website whose details are given here.

Now this is how 1960 onwards the MOSFET has been one of the dominant devices in the field of semiconductor technology.

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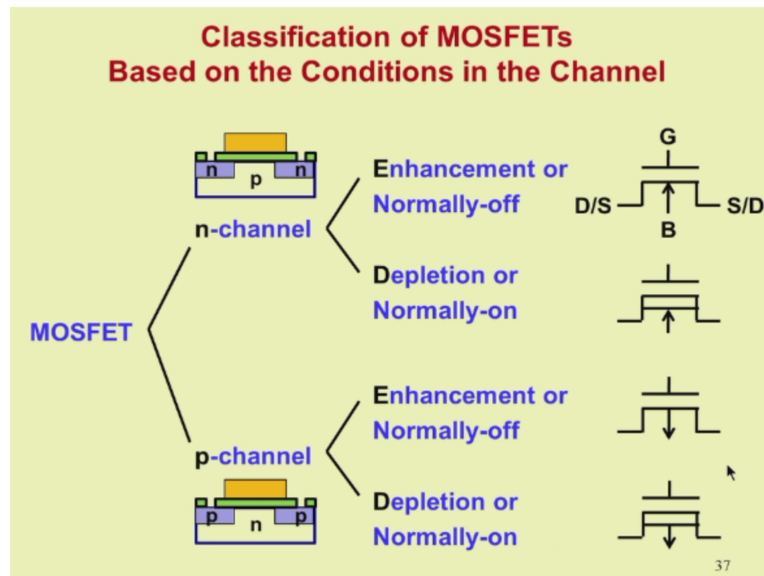

Let us look at the classification of the MOSFETs available at this point of time a wide variety of MOSFETs are available. First let us consider the classification based on the conditions in the channel. You can have an n-channel device or a p-channel device. In an n-channel device, the conducting layer at the interface is made of electrons, the conducting layer incidentally is called the channel. In the p-channel device on the other hand it is made of holes.

A p-channel device is made using n-type substrate and an n-channel device using p-type substrate. The reason for this is that between the 2 n contacts there should be no current flow if there is no channel, because a current flow via the substrate cannot be controlled by the gate. So current should only flow when a channel is created, that is the reason why the polarity of the substrate is opposite to the polarity of the channel. Similar comments apply to a p-channel device.

Now each of the n and p-channel devices can be either an enhancement type another word for which is normally-off, or the depletion type which is also referred to as a normally-on device. So in a normally-off device if you do not have a gate voltage applied, there would be no current flow. On the other hand, in a normally-on device even when there is no gate voltage applied a current flow can be there.

By applying the gate voltage, you can further modulate the current flow. Now how can a device be normally-off or normally-on, well it all depends on the structure of the gate and the substrate and the structure of the interface, more about which we will learn later. Now here is

a symbol of an n-channel enhancement type or normally-off device. Let us understand the elements of this symbol, the 2 ends here constitute the source or drain.

This is the gate which is at a distance from the channel, this line represents the channel. Now the polarity of the channel is indicated by the arrow here, this arrow can be recognised to be the junction between the substrate and the channel. As we have remarked the channel is of opposite polarity to the substrate. So the channel is n-type and the substrate is p-type, we essentially have a pn junction between the substrate and the channel.

Now that is what is shown here by this arrow, so when you represent a diode you know that the arrow which is used to represent the diode it terminates on an n-region. Now that is how an inward arrow towards the channel means the channel is n-type, and the substrate is p-type. In normally-on or depletion type device is represented using a thick channel, so double lines here essentially represent a thick channel.

And this is what means the channel is already present even in the absence of gate voltage. Now I leave it to you to work out the symbols for enhancement type and depletion type p-channel devices which are shown here.

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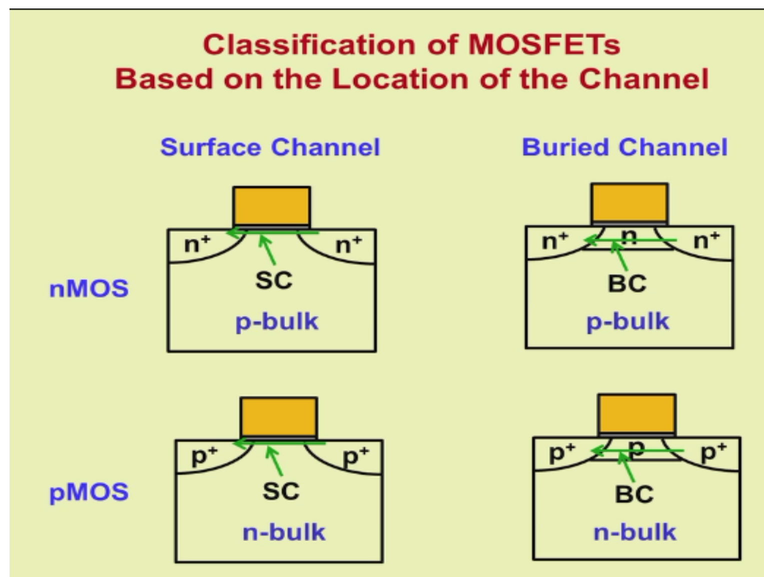

Let us look at classification of MOSFETs based on location of the channel. You can have 2 types of devices namely surface channel and buried channel. Let us take the example of an n-channel MOS device. You can create a thin DOP region near the interface which can be used to pass current between the source and drains. Such a device is referred to as buried channel,

because the current flow is not restricted to the interface, but extends to a small depth from the interface, therefore the current is said to be buried under the interface.

On the other hand, in a surface channel device the conduction happens through an inversion layer, or a layer of mobile carriers attracted to the interface by the gate voltage. So in this case for example electrons are attracted to the interface when you apply a positive gate voltage of sufficient magnitude, and the current flow happens right next to the interface and therefore this is called a surface channel device.

These are the examples of p-channel devices with surface channel and buried channel.

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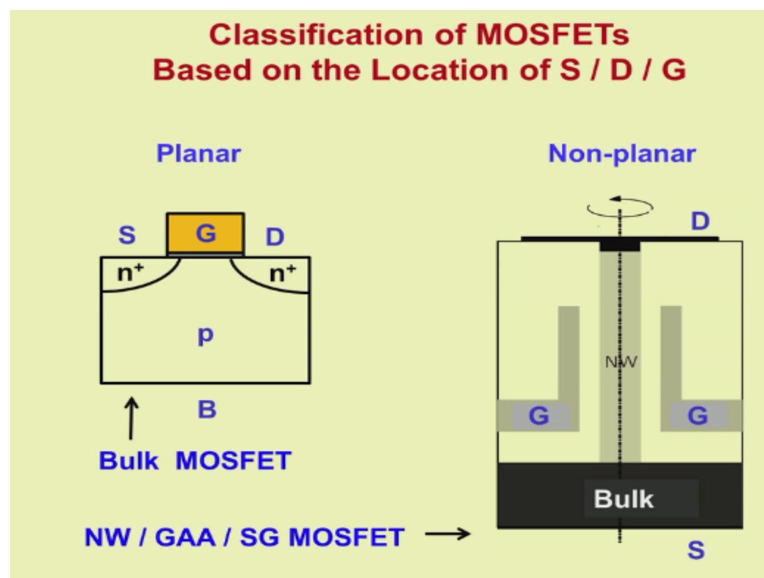

You could classify MOSFETs based on location of the source, drain and gate. Based on this 2 varieties are available, one is called the planar MOSFET and other is called the non-planar MOSFET. In a planar MOSFET the source, gate and drain are all on the same plane, in a non-planar MOSFET an example of which is shown here the drain and source are on 2 opposite phases of the silicon, and the gate is on the side.

In this case, the thin region here of semiconductor constitute the channel that is controlled by the gates, which is present on the sides. What is shown here is the cross section of a cylindrical structure, the arrow here shows that the structure is cylindrical. Now the planar device here is referred to as bulk MOSFET, on the other hand the non-planar device shown here is referred to as a nanowire or a gate all around or surrounding gate MOSFET.

A nanowire MOSFET, because this thin region is like a wire of small size and therefore it is referred to as nanowire. You call is gate all around, because the gate is all around this wire, if you visualise the cylindrical structure. Another name is the surrounding gate, because you can also regard the gate to be surrounding the nanowire. So in non-planar MOSFETs your drain, source and gate are not on the same plane.

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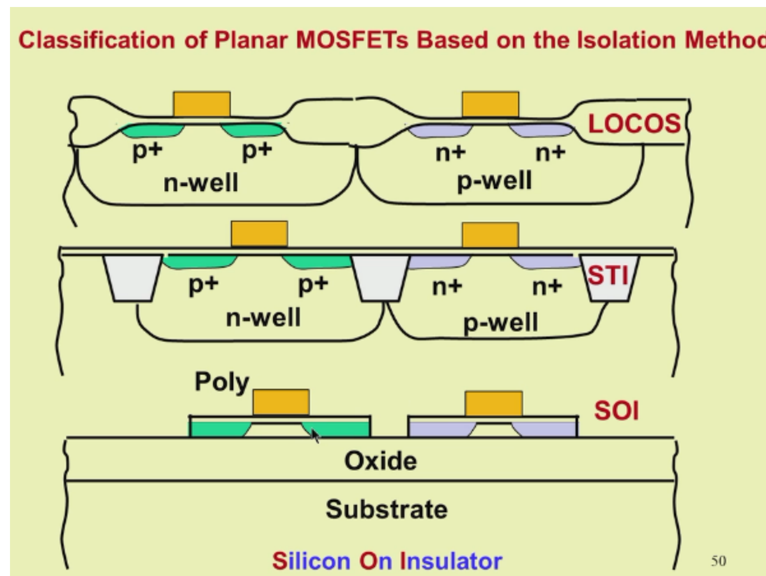

Let us look at one more classification of MOSFETs. Let us stick to planar MOSFETs. Between 2 MOSFETs on an integrated circuit you should have an isolation region so that there is no communication between the 2 devices other than that which is possible by a connecting metal layer over the device. So you do not want any communication between the devices via the substrate and that is why you have what is called an isolation region.

So based on the method of isolation you can have different types of MOSFETs. Here is an example of isolation by local oxidation of silicon. This local region between the 2 devices is oxidised to a thick extent, and therefore this layer is referred to as LOCOS, that is local oxidation of silicon region. This thick oxide layer isolates the 2 devices. How does it do the isolation, well details of this will become clear when we discuss the device operation.

Essentially as we have remarked it prevents any current path between the 2 devices via the substrate. Another method of isolation is the shallow trench isolation or STI. In this case, a trench is etched in the silicon substrate between the 2 devices and filled up with an insulator such as silicon-di-oxide or silicon-nitrite. The third variety is the silicon on insulator or SOI, conceptually the isolation method here is different from LOCOS and STI.

The difference is in LOCOS and STI you have the silicon substrate in which isolation regions are created using small regions of thick insulator. On the other hand, in the SOI method small islands of silicon are created on an insulating oxide layer. So automatically since the islands are separated from each other there is an isolation. In this example for instance the insulator has been created on a silicon substrate, and this insulator provide isolation between the islands of silicon devices.

The LOCOS and STI structures are normally referred to as bulk MOSFETs, because these devices are made in bulk silicon or substrates. Now the STI provides you a higher density of devices of LOCOS as you can see from here the width of the region shallow trench isolation regions is less, than the width of the local oxidation region. So evidently you can pack more devices in a given area.

As compared to the bulk MOSFETs the SOI provides even higher device density, because you can bring 2 islands of silicon closer to each other than you can using the STI or LOCOS methods. It is important to know these various types of devices, because there are certain idiosyncrasies associated with each of the device and therefore differences in some of the phenomena.

So when you discuss the modelling, while there is definitely lot of modelling features which are common for all types of MOSFET there are also a large number of features which are different for different types of MOSFETs.

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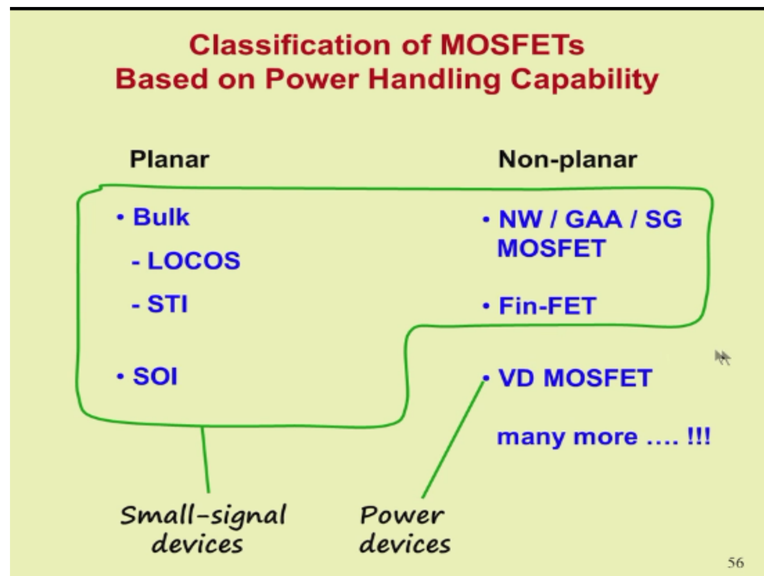

Finally let us classify the MOSFETs based on power handling capability. You can have small signal devices or power devices, in small signal devices you are managing currents of the order of hundreds of micro amps or may be up to millions, and few volts of voltage, whereas in power devices you are handling current of tens to hundreds of amperes and voltages from tens to thousands of volts.

The planar devices of the bulk and SOI variety which we discuss so far are examples of small signal devices. Similarly, the nanowire, gate all around or surrounding gate MOSFET is an example of a small signal device of the non-planar variety. Fin-FET is a small signal device of the non-planar variety. On the other hand, the vertical double diffuse MOSFET or VD MOSFET is an example of a power device and its structure is non-planar, you have many more types of MOSFETs.

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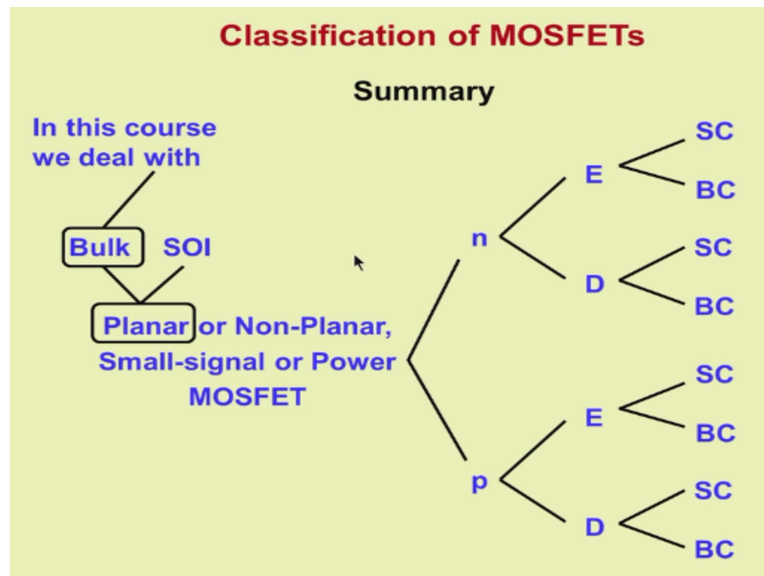

Let us summarize the various types of MOSFETs we discussed so far, a MOSFET can be planar or non-planar, small signal or power and each of these devices could be either n-type or p-type and an n-type or p-type device further could be enhancement or depletion type and an enhancement or depletion type device further could be a surface channel or a buried channel device based on the location of the channel.

As we discussed a planar MOSFET could be of the bulk variety or SOI variety. Now in this course, we are going to deal with bulk MOSFETs. So now onwards we shall focus on the bulk MOSFETs. Now let me put down a slide from the device modelling procedure, we discussed a couple of modules ago. The first step to modelling any device in the present instance it is the bulk MOSFET would be the following.

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1) Structure and Characteristics to Scale

- Have an idea of the steps in which the structure is fabricated
- Visualize the following to scale
  - the cross-section, top view, 3D view of the real device
  - the doping profile
  - the characteristics

The above information helps in developing qualitative understanding, making approximations and parameter extraction

We should look at the structure and the characteristics of this device to scale. Let me recall what is involved in this step, from the previous module. Have an idea of the steps in which the structure is fabricated and visualize the following to scale, the cross section, top view and 3D view of the real device, the doping profile and the characteristics. As we have remarked the above information helps in developing qualitative understanding, making approximations and parameter extraction which are the later steps in device modelling.

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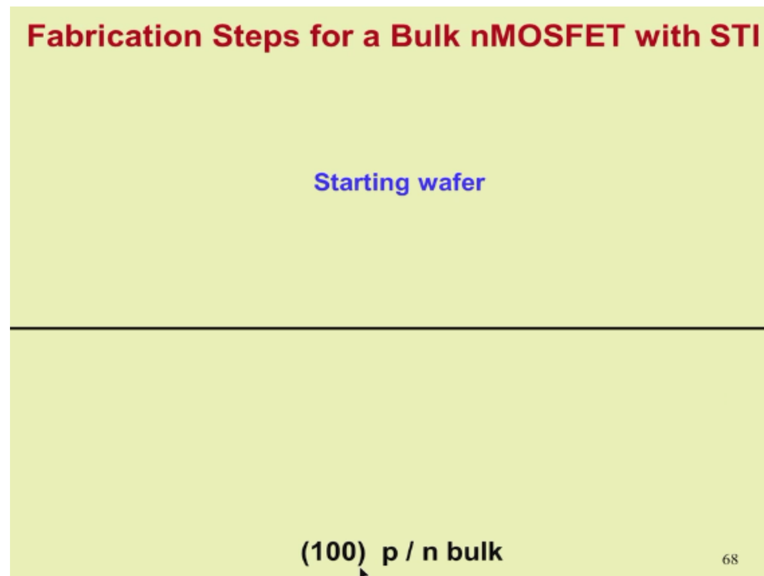

Let us begin with the fabrication steps for a bulk MOSFET with shallow trench isolation. The same fabrication steps would apply to a p-channel MOSFET for example with shallow trench isolation. We start with a n or p-type thick silicon wafer called the bulk, 100 here represents the orientation of the silicon wafer. Now depending on the orientation of the silicon crystals, the surface may have different density of silicon atoms.

For a good MOSFET operation, we require that the density of atoms on the surface be as small as possible, because the surface atoms can give rise to what are called interface charges. And the density of interface charges is related to the density of the surface silicon atoms. The interface charges is something that really we do not want in a MOSFET, though we have to live with it.

We would like ideally the MOSFET charge in the channel to be controlled by the gate and we do not want any other extraneous factor to control the charge, interface charges are some extraneous factor, which try to control the charge in the MOSFET and therefore we would

like to reduce its inference as much as possible. So 100 represents that orientation of silicon wafer which gives you the minimum density of the silicon atoms over the surface.

Now why is the orientation called 100. That is beyond the scope of this particular course, you can refer to lectures on VLSI technology for example, to understand what is the meaning of these numbers 10 and 0.

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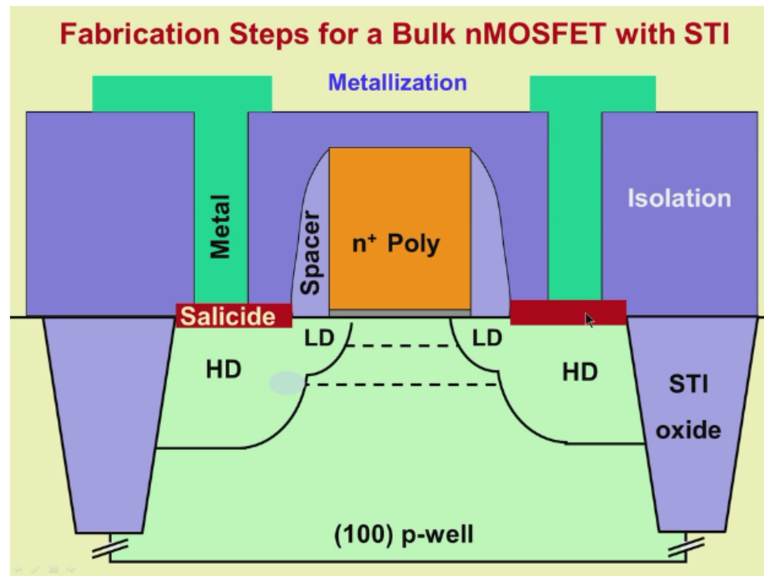

How do they represent a particular orientation of silicon? The first step is to dig a trench or etch a trench in the silicon. This trench is then filled up with an insulator such as the silicon-di-oxide. Next we would like to create a region of very controlled doping so that the threshold voltage of the MOSFET can be controlled precisely.

To make such a well controlled region, we implant boron into silicon to a small depth which is next driven inside to the required depth which is a little below the depth of the trench, using a high temperature process for a sufficiently long time. This region is then referred to as a well, since this is doped with p-type material such as boron, it is called p-well. Next you try to control the doping near the surface even further.

So there are 2 regions near the surface, one is called the region which tries to correct the threshold voltage to a required value this is called a VT correction implant. And a deeper inside there is a doped region which is meant to control the punch through effect. Now let us understand what is this punch through.

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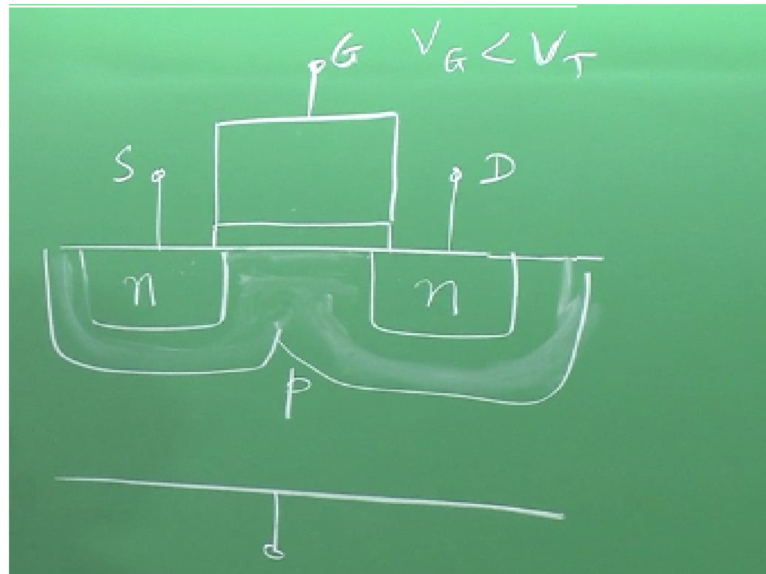

Now this is your schematic of a bulk MOSFET, these are your source and drain regions, we have not yet discussed how these regions are created, but I am just trying to explain what is the meaning of the punch through phenomenon. You know that you will have depletion regions extending in the bulk, p-type region near either junction.

Let us show the situations for drain voltage more than the source voltage. Therefore, the depletion region near the drain is more than that near the source. Now this is the gate region and this is your bulk. These 2 depletion regions from source and drain should not merge with each other. So from basic level course, you might recall that an inversion layer here conducts the current between drain and source.

So if you want the MOSFET to be turned off for some gate voltage, no current should flow, for gate voltage below that voltage, which is called threshold. Now if there is a punch through meaning this depletion region touches this depletion region for some reason, that could be because the 2 n regions are very close or because the doping is less, in which case you know from penetration theory that depletion region would be more.

So if these 2 depletion regions were to touch each other, something like this, now what would happen is, one can show that you can have a current between drain and source flowing even when there is no gate voltage applied. So you want to prevent this kind of a situation where even without a gate voltage, you have current flow between drain and source and this current then is not controlled by the gate.

So to avoid such a situation, you try to dope this region heavily, so that the depletion regions here would be reduced at least in the channel region. Now you might say that why not increase the doping throughout the well. Well increase of the doping throughout the well has other disadvantages, such as if your doping here is more, depletion here would also be small and a consequence of that would be the capacitance associated with this junction here would be large.

These parasitic capacitances would increase. You do not want the capacitances due to the source entering junctions to affect your high frequency performance of the device. Also the breakdown voltage between drain and source, which is reverse biased when the MOSFET is operating in the active region would be reduced if the doping is more. So in order to control the parasitic capacitances have a reasonably high breakdown voltage.

You would like the doping in most of the well to be as low as possible. So doping in this region should be as low as possible. Whereas doping near the interface where the channel is present, you would like it to be high so that depletion region from source and drain do not touch each other near the interface. So this is how you achieve low parasitic capacitance and high breakdown voltage and at the same time, you avoid punch through by controlling the doping near the channel, rather than through the entire well.

Next step is to grow a gate oxide, which is a thin oxide of high quality. After that, you deposit polysilicon. Polysilicon should be conducting and generally is heavily doped n type. Then you deleanate the gate by etching out polysilicon in regions other than the gate. Then, you remove the gate oxide as well in the regions other than the gate. The next step is to create the source and drain regions, that is this regions, which are shown here.

Now LD here means low doping. Let us see why you need the low doping in the source and drain regions near the channel. We have just now remarked that you would like the depletion regions from source and drain to be sufficiently small so that they do not touch each other in the channel region. For that purpose, you are increasing the doping in the channel region. Now another way, you can reduce the depletion width in the substrate is to reduce the doping of the n region.

You know that in a Pn junction, the lightly doped region takes the most part of the depletion layer. So you can reduce the depletion layer part in the P type substrate by decreasing the doping of the n type region. So that the depletion region would fall mostly on the inside, here as well as here. Now that is why you are reducing the doping of the source and drain regions near the channel.

As we will see in the next step, we will however, increase the doping of the source and drain in the other parts. We would like most of the source and drain regions to be heavily doped because a low doping would mean a high resistance of the current flow from this edge to the contact. So this is the source resistance and this is the drain resistance. We would like the resistance of these regions to be as low as possible.

For that purpose, you need heavy doping. Now that heavy doping will be created in a later step. After creating the low dope drain and source regions, you realize what is called the spacer. So this is an insulator layer deposited all over, which is etched out in regions other than those next to the gate. These spacer regions now insulate the gate region from the contacts created to the drain and source.

You now create the heavily doped and deep source and drain regions, which have low resistances. This is done using phosphorous implant. To reduce the contact resistance between the metal and the semiconductor, you create an in-between layer called the salicide layer. Now you do make a contact to the gate poly also. However, the contact to the gate poly will not be seen in the cross section.

Because the contact is not made right above the channel, but away from the device and so the location of the contact will be seen on the top view, which we will show shortly. The next step is to create an isolation region, which tries to separate the metal contacts so that there is no short circuiting of the various contacts. This isolation region is made of oxide into which you open contact windows above the salicide regions.

The next step is to create the metal that will interconnect one device to another device.

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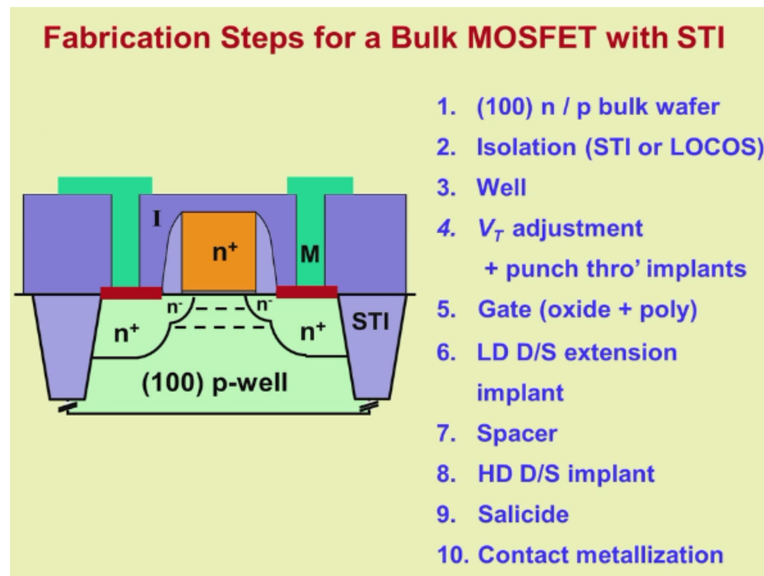

Let us summarise the fabrication steps for a bulk mass with shallow trench isolation. These are structures that is realized essentially in these 10 steps. The first step, you take a silicon wafer, next you create the isolation, which could be shallow trench isolation or low cost, that is you are creating these regions, then you create the well, that is this region, then you create the threshold voltage adjustment and punch through implants.

That is these 2 regions, then you create the gate, which consists of the oxide and the polysilicon. Next is the low-doped drain and source extension that this n minus regions, after which you realise a spacer layer, that is these 2 regions. Following the spacer layer, you create the n + heavily doped source and drain regions, that is the 8th step. After that you create the contact regions by depositing salicide material.

And finally you make the metal contacts, so that is the final step. Now in practice a bulk MOSFET structure has many additional features that we have not discussed. One such feature is what is called a hallow implant region right next to the low doped source and drain. This implant is used for a couple of reasons, one of which is prevention of punch through. Let us look through the top view and 3D view of the MOSFET. So far, we have been concentrating on the cross section.

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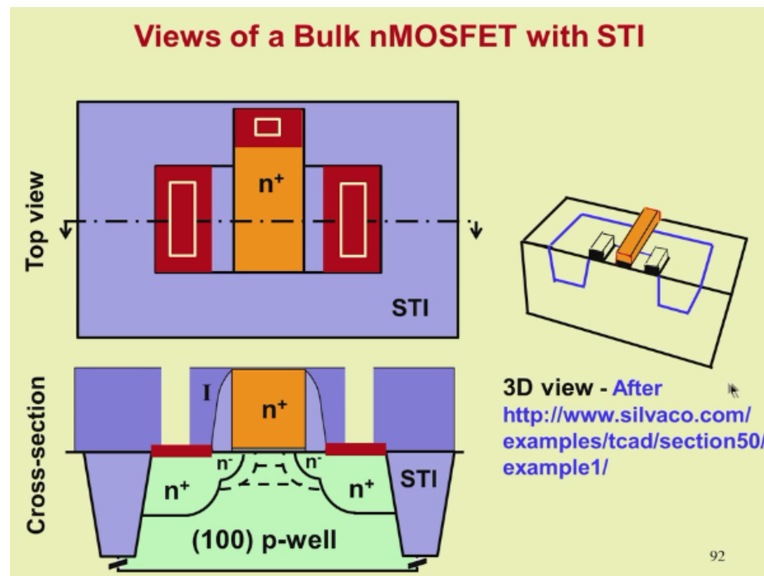

Let us remove the metal and isolation regions of the MOSFET and see what would be the top view of such a device. For this cross section, the top view is shown here. So you have a trench surrounding the device region, which is this. In this device region, you have the source and drain contact regions, which are the salicide regions here and here you have the polysilicon gate.

Now we have remarked earlier that the contact to the polysilicon gate is made away from the device area, so somewhere here. So you can see that this is the region for making contact to the n + polysilicon gate. Now if you add the contact windows to this structure, then the top view would look something like this. So a part of the contact region is the contact opening. Here is the 3D view of the same device.

You can see that you have a thick bulk silicon, in which you have a shallow trench, but whose width is somewhat comparable to the size of the device itself and then in the device regions, you have this pillar like structures, which represent the source contact, drain contact and the gate polysilicon contact. So this should give you the relative sizes of the various parts of the device in different views.

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Dimensions of a 40 nm STI nMOSFET

Visualization of a device structure to scale allows one to develop an estimate of all the critical dimensions of the device from a knowledge of just one or two of them.

Now let us look at the dimensions of a 40 nanometer shallow trench isolated nMOSFET. The 40 nanometer refers to the length of the gate. Now before we look at the dimensions, let us make a comment, visualization of a device structure to scale allows one to develop an estimate of all the critical dimensions of the device from a knowledge of just 1 or 2 of them and that is why visualization of the device to scale is very important.

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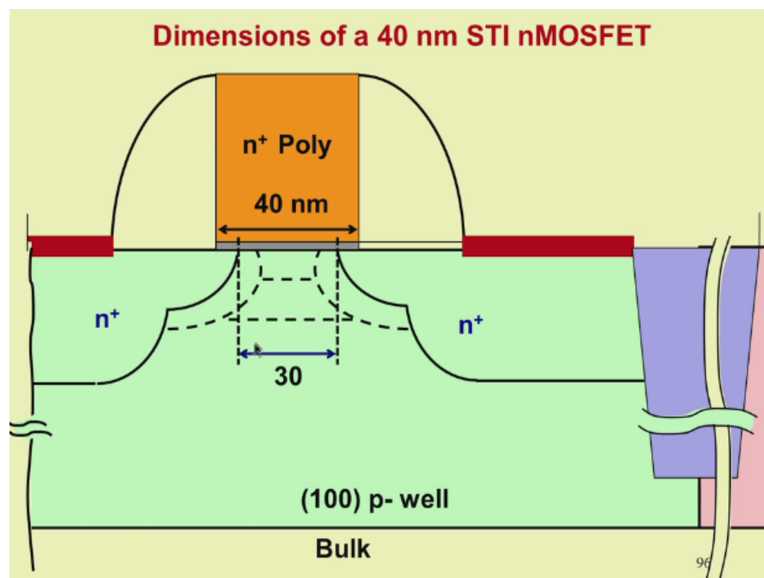

Now here is a cross section of a 40 nano meter STI MOSFET 40 nanometers is the length of the gate here. As compared to that length of the channel is 30 nanometers, which means you have 5 nanometers of regions here, in which the gate overlaps with the source and drain. The channel is the distance between the source edge and the drain edge. That is the edge of the doped regions. The gate pitch is 170 nanometers.

The gate pitch represents the minimum distance between the gates of 2 adjacent transistors. So this gives you an idea of how close can you make the 2 devices on an IC. The thickness of the oxide is about 1.2 nanometers. The depth of the low doped source and drain regions is 15 nanometers and the depth of the heavily doped source and drain regions is 40 nanometers. The height of the polysilicon gate or the thickness of the polysilicon layer is 70 nanometers.

The depth of the trench isolating the devices is 300 nanometers and the depth of the P well is about 500 nanometers. The thickness of the spacer between the source and drain contacts and the gate is 35 nanometers and the width of the trench isolating the devices is 80 nanometers. The length of the source and drain contact regions is 60 nanometers.

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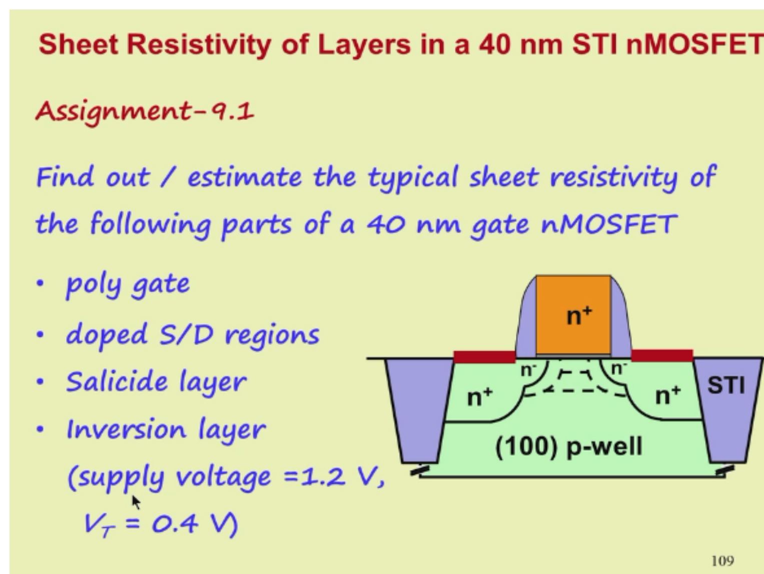

Now here is an assignment for you, which is related to the sheet resistivity of layers in this device. Find out or estimate the typical sheet resistivity of the following parts of a 40 nanometer gate and MOSFET. The parts are a polysilicon gate that is this region, dope source and drain regions that is these regions, and a salicide layer, that is these regions. Finally, you also have to determine the sheet resistivity of the inversion layer assuming that you have a supply voltage of 1.2 volts and a threshold voltage of the device is 0.4 volts.

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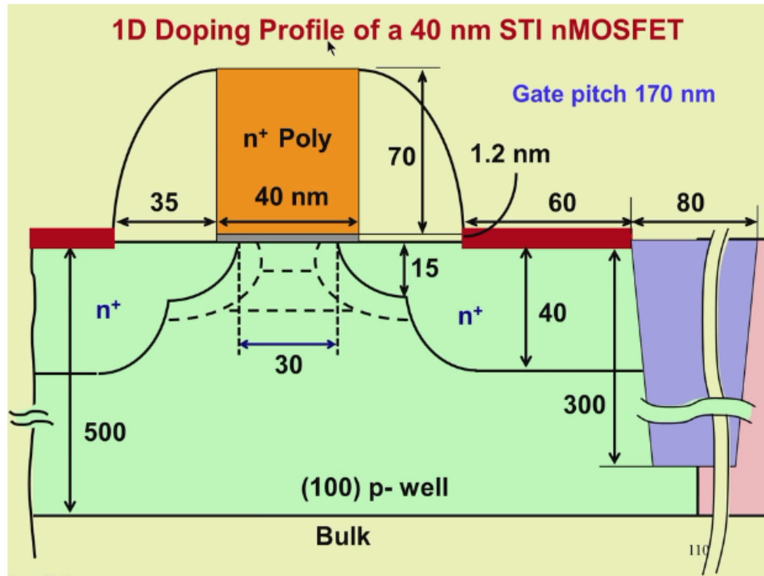

Next, let us go to the doping profile of a 40 nanometer MOSFET. We shall show the doping profile in 1-dimension, both vertical dimension as well as horizontal dimension.

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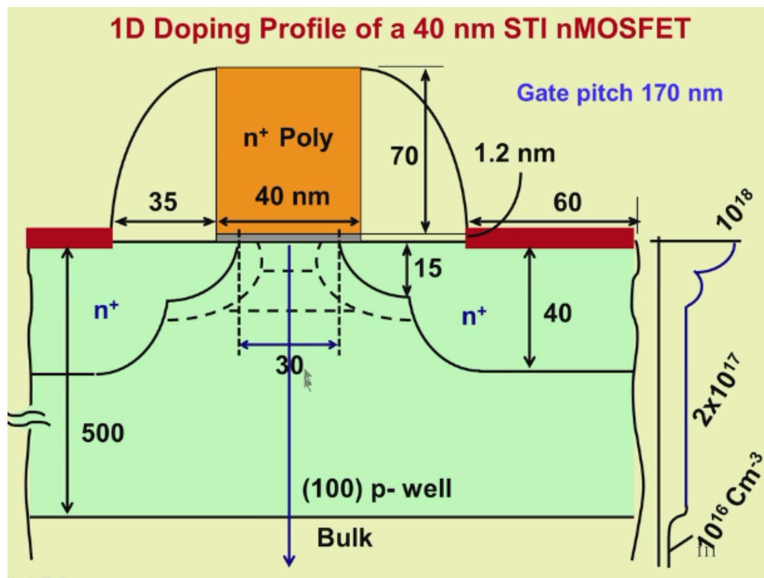

First let us look at the vertical doping profile, which controls the device characteristics to a significant extent. The threshold voltage correction region has a doping of about 10 power 18, the maximum doping here at the surface is 10 power 18. Then, it reduces to a fraction of 10 power 18 when you reach the punch through implant region, that is this region. In the well region here, the doping is about 2 into 10 power 17 per centimetre cube.

And in the substrate or bulk beneath the well, the doping is about 10 power 16 per centimetre cube. We are looking at the doping profile in the vertical direction at the center of the channel. Next, let us look at the doping along the interface from source to drain regions. Here

you find that the region between the hollow implants, these 2 are called hollow implants. This region here the doping is about 10 power 18.

In hollow implant region, it increases to 5 into 10 power 18, that is in these regions. In the low doped source and drain regions, the doping is 10 power 19, here. While in the heavily doped region, the doping goes up to 10 power 20.

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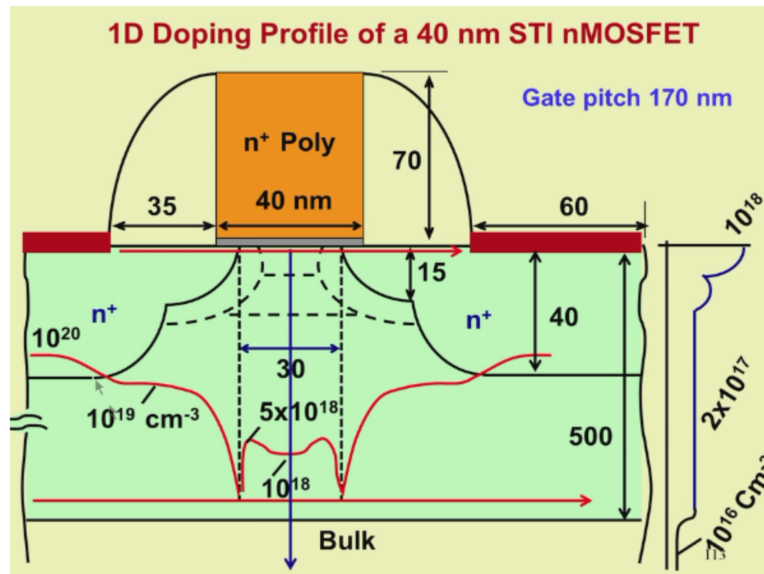

To show the complete doping picture, we have added the vertical doping profile also along with the horizontal doping profile in this slide. Now before we move on further, we want to remark that we have shown the dimensions and doping profile in the cross section. Now the width of the MOSFET can vary from a micron to several microns depending on how much current you want to draw from this device. So this will depend on the circuit design.

That is why the width of the MOSFET has not been shown here. So width of the MOSFET is in the hands of the IC designer. Whereas the cross section that is shown here is not in the hands of the IC designer. It is in the hands of the process designer.

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Doping Profile of a Bulk nMOSFET

Assignment-9.2

Figure out why the vertical doping profile should be realized before the lateral doping and not vice-versa, during fabrication of a bulk MOSFET.

Let us look at an assignment related to the doping profile. Figure out why the vertical doping profile should be realized before the lateral doping and not vice versa during fabrication of a bulk MOSFET.

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Summary of this lecture

Now with that, we have come to the end of this lecture. Let us make a summary of the important points. So we began a module on MOSFETs where we are going to discuss about the structure and characteristics of this device. In this lecture, we first gave a brief account of how this device evolved over several years from about 1925 to 1960. What are the various stages of evolution and how today we have a variety of MOSFET structures.

So we mentioned the classifications of the MOSFET structures based on the condition in the channel whether it is because of electrons or holes, based on location of the channel, whether

it is surface channel or buried channel, then we classified the MOSFETs based on the location of the source, drain and gate. So you have planar MOSFETs in which source, drain and gate are all on the same plane and non-planar MOSFETs where these 3 contexts may be on different place.

Next we discussed bulk and silicon insulator type SY MOSFETs. Bulk type MOSFET, you can have the isolation region created by shallow trench isolation or by local oxidation of silicon. Finally, we also discussed about small signal MOSFETs and power MOSFETs. It is important to be aware of the various structures of the MOSFET because the modelling of different structures, there are significant differences, just as there are some common features as well.

After discussion of the types of MOSFETs, we focused on the bulk MOSFET because we said we are going to derive a model for this device. For the bulk MOSFET, we discussed fabrication steps and we gave an idea of the dimensions and doping profile of a modern bulk MOSFET. In the next lecture, we shall discuss the various characteristics of a bulk MOSFET.