Analog circuits and Systems through SPICE Simulation
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Lecture - 08
Basic Analog Design Part III (Contd.)

Good afternoon everyone and welcome to our second session on analog basic signal design. I hope all of us connected now. And we will begin with where we left yesterday.

So, yesterday we well through detailed discussion on MOSFET as a device. We looked in to the dc characteristics. We looked into the small signal analysis, small signal model, how does this small signal parameters come into picture. How do they make physical sense, what is the dependencies on device parameters or the sizing parameter that we have in hand as designers. We also looked in to the high frequency model that is related to the frequency response of these devices. And we understood the concepts of parasitic capacitances what is their origin, and how they play very important role in determining the performance of the circuit is.

Following that we looked into another very important concept that is noise and we incorporated all these 4 analysis. Dc analysis, small signal analysis, high frequency analysis and noise analysis, into analyzing simple common source something for with register load. We also looked into a few issues related to design optimizations just a small example where we are trying to maximize or increase the small signal gain by tweaking some the parameters like R D or the I D, while maintaining some other parameters like the signal swing. And the bandwidth and we got a test that a way what kind of design complex we are going to face when we look for practical circuit design issue when we are trying to meet certain specs in terms of power in terms of gain bandwidth, noise, swing and so on.

We see that there are so many different parameters coming together, and so many different specs coming together. And that is the beauty of analog design, we need to come up with holistic solution close to the best freezable solutions using our understanding and knowledge of the circuit operation, and how does it you know, depend upon the device parameters and how does it link to the high level specs. So, continuing from where we left. We will be looking in to common source amplifier with active load.

Yesterday we did it with resistive load; we are going to do it now with active load. And that is going to be linked with our discussion on front end because, in the front end we will be using differential amplifiers, 2 stage amplifier in form of op-amp and ultimately whatever analysis is required for those amplifiers boils down to common source amplifier with active load.

So, whatever we will be doing today it is ultimately going to be linked directly with hover front end amplifier design. Once again staring with dc operating point, small signal analysis, frequency response and noise analysis along with that you know, the peripheral circuit like current mirror we are going to look in to design of these and all these 4 analysis are going to be applied to the common source amplifier with active load. And once we are done with this process we are we will ready to go into differential amplifier and multistage amplifier which is going to be the building block for our low noise front end amplifier for the, analog front end.

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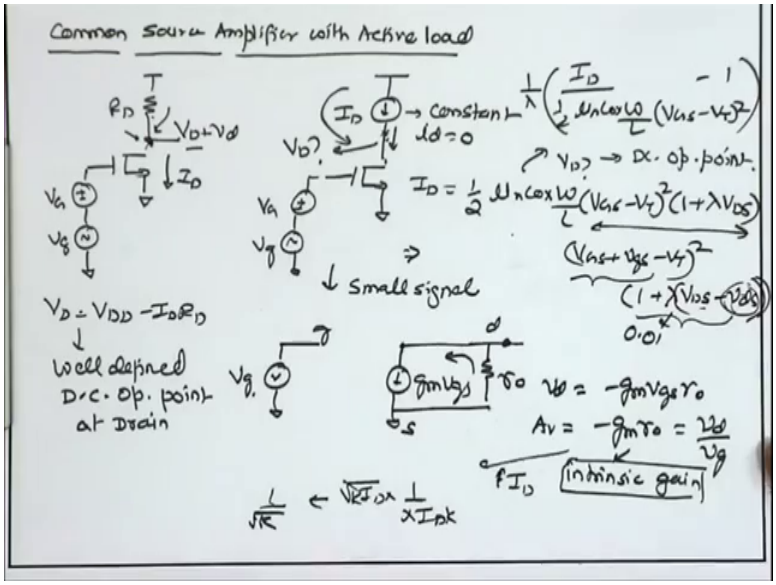

So, let us start our discussion common source amplifier with active load. So, yesterday we have discussed a common source amplifier with resistive load, where we took a simple example capital V G is a dc voltage on the top of that we are applying a small signal V G. And we are looking at the small signal V d produced, and we noticed some techniques so which we can include the gain. So, one of the possibility was increasing R D.

And we mentioned that whenever we trying to increase R D it directly couples with the V D. So, if you are trying to increase R D the dc voltage V D is going to come down, and as a result we are not going to get the maximum possible swing that we want. So, signal swing is directly related to the R D. Larger R D means lower dc point for a given current and as a result the gain over here can trained of directly with the signal swing. So, this is one of the disadvantages of using passive load. Another issue is the area of this passive element that is to be implemented on a integrated circuit.

Then we are talking about integrated circuit, passive registers can be implemented in several ways and in general they take good amount of area. As compare to the active devices of MOSFETs the area consume by this passive registers, capacitors can be pretty large. And as a result we can if we can avoid the use of these passive elements and use active loads that is employing CMOS transistor either PMOS or NMOS directly as load elements, probably that can be advantages.

What is the mean motivation behind using active load in presence in place of this passive component R D? So, let us talk about an ideal active load which is a current source. So, what happens to the circuit if I replace this R D with a ideal dc current source I D and then do a same analysis? So, what is the property of a of an ideal dc current source? This must remained constant therefore, there is no ids small signal I D is 0 this current flowing into the drain will never change.

So, how does this give us any gain? So, if we now look at our current equation of the MOSFET I have I D is saturation region. So, we have these 2 terms, combine together these 2 terms should remain the product of these 2 terms should remain constant. And now if we are trying to increase V GS; that means you are trying to increase the first term V GS plus small V GS; that means, in order to counter this the second term must reduce must have V DS if I call it a positive quantity. So, V DS is a positive quantity. So, taking together the second term should reduce if I will increase the first term. So, that the product remains constant.

And now, if we see the dependency in saturation region this lambda is very small right. So, it may be for 180 nanometer may be 0.01, 0.02 and therefore, in order to counter this small change in V gs which is having qualitative dependence, I may need a very large change in V DS to balance this increase. So, the increase in the first term has to be

balanced by the reduction in the second term in order to counter this increase is a arising from this quadratic term, I must have pretty large reduction in the V DS. That is, this small V DS must be large because this is getting multiplied by lambda and then resulting in the overall term. So, that mandates large reduction in V DS to have compensation for the first term. So, that the product remains constant.

So, that is a basic mechanism for obtaining gain in this circuit. So, when we are trying to reduce V GS same thing will happen this first tern reducing I need a large increase in V DS So, that the increase in the first term is compensating the reduction in the second term. So, here if we want to do the small signal analysis this is a dc current source. So, how does this small signal model look like? So, once again V G is set to 0 capital V G we are only going to deal with the small signal V G we have gm V GS. The current source is ideal dc current source, there is no small signal current flowing it to this. And we do that for ideal current sources, ideal dc current sources, we open circuit then is small signal analysis because there is no small signal current flow.

If there is the no current flow in any branch; that means, that branch can be open circuited. So, this is there is no small signal current flowing this branch I can open circuit this in my analysis. And therefore, the drain terminal we disconnect the dc current source and we know that r o is just going to come between the drain and the source. Source is grounded and we have the g. So, here we get an overall gain because of the applied V G, gm V GS flows in to r o or remember that when we say that gm V GS flows in to r o we should remember that it is not that we have a physical r o existing in parallel with the NMOS.

It is just the physical characteristics of the device which is giving raise to this r o and the basic mechanism is over here. So, this is that just compact mathematical representation of what is happening physically using this equation. So, we should always have this in mind that this is a small signal equivalent parameter which is capturing the large similar behavior, which is capturing the you know effect of this large signal equation, when we are applying a small signal. So, this r o is of course, not a physical physically existing quantity it is just capturing the behavior of the MOSFET. In this case we say that this gm V GS flows in to r o and therefore, V d is going to be equal to minus gm V GS times r o therefore, the gain is minus gm r o which is V d upon V g.

This is call the intrinsic gain of the MOSFET. So, if you are having ideal current source connected in the drain we get maximum possible gain of out of this common source amplifier which is equal to minus gm r o. Once again we can look at what is going to happen to this small signal gain if we are trying to play with these parameters. So, if we are trying to increase the gain what are the options that I have. So, suppose I increase my I D what do we expect. So, we know that if I increasing my I D gm is going to go up by root I D, but r o is dependent upon one upon lambda I D. So, my gain will go up if I am increasing my I D the gain will go down by a factor of root K suppose I increase the I D by K times the gain will go down by root k, if I am reducing my I D by K times the gain will go up by root k. So now, how do we implement this ideal current source or at least a current source which is close to this ideal current source in our actual circuit is so that we can achieve this kind of relatively large gain in our circuit.

Before I proceed that the one of the important point that we would like to emphasize here, in case of passive load we knew what is the dc operating point at the drain. This is V D where V D is equal to V DD minus I D R D. So, we have a very well defined dc operating point at drain. So, remember in order to have a well defined dc operating point, we need well defined dc at the gate, well defined dc at the drain and hence a well defined I D dc current. So, the drain voltage gate voltage and the I D should be well defined. And on the top of that we can superimpose some small signal to get my amplification. And a well defined dc operating point ensures that for the entire range of the input signal my transistor is going to remain in saturation that is a purpose. So, here what we can say about the gate voltage.

Once again we do have the facility or freedom to choose V g we are using a current source, suppose you have a current source available with you. So, again we have the facility of providing this I D, but what about V D. So, here what is the equation of V D that I can write if it is an ideal current source. So, one of the ways is to solve this equation for a particular lambda right. So, here if I just solve this equation considering the effect of lambda V GS minus V t square is known to me. I D is known because this is thicks by this ideal current source.

So, basically the V DS from this equation, if I want to find out this will be I D upon this constant factor which is one upon 2 mu n cox W by L V GS minus V t square minus 1 upon lambda. So, that is the value of V D that I expect. So, remember here what we are

saying is V GS is being fixed we have the freedom to choose V GS. We have used a current source ideal current source. So, we have chosen I D, therefore this gives us that the V D is dependent upon this lambda 1 upon lambda. And in general lambda is not a very well defined very precisely defined quantity. It can vary a lot from device to device on a single chip. And as a result this is not a very well defined V D. V D as a result can vary a lot. Some device can have lambda of 0.01 some other device can have a lambda of 0.03. So, V D can have 100 to 200 percent variation, and as a result we are not sure whether the transistor over here is going to be in saturation region.

So, it is seems like we do have a problem with respect to dc biasing how do we set the dc operating point of this MOSFET. That is the problem with active load. So, it seems like yes gain point of view we can get a large gain minus gm r o, but from the point of view of dc operating point we are having a problem. So, we are going to see how can this problem be addressed. So, let us first talk about quickly how to implement this I D.

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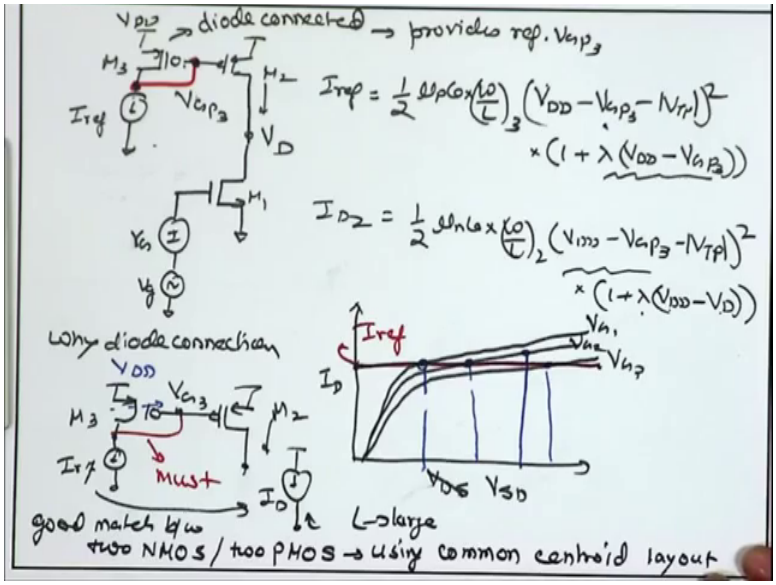

So, once again in general on an integrate circuit if we are talking about an analog IC we may have a certain mechanism of producing a relatively precise, stable current source which is going to be independent of supply independent of V DD. So, there are mechanisms through which I can produce an i ref a reference current which is independent of V DD. So, if time permissible we go through some basic techniques

through which we can generate well defined reference current, which is quite controllable.

And using this reference current I can create current source I can form a current source which is going to provide the bias current to my NMOS transistor. So, this is once again my earlier device. I had the capital V G on the top of that small V g. And here I am trying to form a current mirror. So, this is a diode connected MOSFET if I call this n one n 2 and n 3, n 3 is diode connected drain and gate are shorted.

Why do we call it diode connected? Because transistor is a 3 terminal device here we have shorted the 2 terminals drain and gate now it has become a 2 terminal device it is become a something like a diode. So, if you control the voltage at this point the current is going to increase in a square law fashion, the curve may look like similar to a diode. And since the gate and drain are always shorted it will shows that as long as the V g is greater than V t the V sg is greater than mod V TP in this case the transistor is going to be in saturation region. So, first purpose is that it keeps the transistor in saturation region.

Therefore, depending upon this is i ref I can find out what is the V sg of this MOSFET. So, I can just write down the equation i ref equal to 1 upon 2 mu t c o x W by L, call it W by L 3. V sg is V DD minus V G t 3 V GP 3, minus mod V TP square if I ignore the channel length modulation for this device, from this equation I can find out what is the V GP required to establish this i ref. If I do have to include the channel length modulation I can do that. So, this will become 1 plus lambda V DD minus vs this is lambda V sd, So one thing vsd is nothing as the V GP. So, this is again V GP 3.

So, in general here we see that the V d is equal to V G and therefore, the V SD is not going to be that large. So, we can in general ignore this lambda while circulating the dc condition. So, from this equation I can find out what is the value of V GP required. So, that the n 3 is having sufficient V sg to support this i ref. So, direct connected branch provides as a reference V g V GP 3, provides reference V GP 3. So, it is developing a reference voltage which is now applied to the gate of m 2 and thus and since, this m 3 and m 2 they have the same source same gate. So, once again for the m 2 if I ignore channel length modulation I can say the I D 2 in m 2 that is once again going to be one upon 2 mu n c o x W by L 2 same equation V DD minus V GP 3, which was this is common n V TP square.

If I assume that V TP of this transistors are almost similar; that means, these 2 transistors are well matched I can ensure that the current in m 2 is going to be a copy of current in m 3. Because this term is constant this is same in both and of course, you have the dependency on output voltage 1 plus lambda V DD in this case it will be V D, let me call this is V D, so 1 plus lambda V DD minus V D because, this is the V SD for m 2. So, as long as this lambda is small and V DD minus V D is no not too large we can approximate this total current as just the pause term quadratic term and therefore, it is just going to mirror the current in m 3 mirroring ratio being given by the ratio of W by L for m 2 and m 3 right.

Now, one of the question is that, why do we need direct connection over here? Why cannot we just, why cannot we just do this? Is this going to work? Same thing I am not connecting the drain and gate of m 3. So, what is the problem here? So, in general in an integrate circuit or even in discreet MOSFETs if you do not have a direct dc connection for any circuit node or high impedance circuit load like the gate, we say that it is the floating node. In this case this gate terminal of these 2 MOSFET are the floating point, we do not know what is the DC voltage over here.

And as a result this can take any random value between V DD ground depending upon some spurious current pass or the leakage current that is flowing through the MOSFET. So, there can be some leakage path ideally the oxide should not conduct, but there is some leakage path as a result there can be some you know voltage any voltage between V DD and ground can appear over. Here we do not have a control on this voltage, and as a result we do not have the control on v g.

And therefore, if you are given we showing that this is the ideal current source very good reference i ref is the good reference it is remaining constant. So, what do we expect from the characteristics of n 3? So, if I draw I D V DS of n 3, they are these are different-different curves for V G 1 V G 2 V G 3. So, this is how the I D V DS characteristics of a MOSTFET look like. So, if I am drawing these characteristics for m 3 where my V G 3 is not defined in a proper way. So, let me call this V SD because it is for PMOS; so I D versus V SD.

So, these are my V G 3 is not very well defined, as a result if I draw a straight line my current is somewhere over here. So, if I draw a straight line this is the i ref that I am

putting for this i ref I do not know where is going to be my V d it can be here, it can be here, it can be here. I do not know where is my V SD, is of the is not well defined. So, since V G can take any value it is floating node it can take any value between 0 and V DD as a result if I look at this curve the V SD can take widely different values we do not have any control on the drain voltage at this node either

And therefore, this can be in triode region, we do not have any control on the operation of this transistor. Therefore, it is necessary to connect the drain and gate of m 3. So, that we make sure that the V G and the V d value are equal. And then we have a unique point in this plane once we make this diode connection then we have a unique point, a unique curve only an a unique point only then satisfy this equation. Because in that case the V d and is equal to V G we are forcing that condition. Then we do not have that un deterministic behavior. Now another question that generally comes up what happens if you have a diode connection for m does rather n 2? Does the current mere operation still remain?

So, once again if you look at the current whereas, behavior we are trying to implement an ideal current source the n 2 is suppose to mimic the behavior of an ideal current source which is copying i ref. And what is the property of an ideal current source? The small signal resistance should be very high, ideally infinite; that means, if the voltage at this node is changing; that means, if the drain voltage of n 2 is changing significant. Why keeping n 2 in saturation? The I D should not change much, it should remain constant.

And that is going to happen when we are having the output characteristics, such that the gate voltage is constant and we are observing the drain voltage. So, this is the curve when we have the gate voltage constant and then we are steeping the drain voltage, right. V SD is changing, in that case the change in I D will not be very high because as long as the transistor is in saturation gate voltage is constant and then you change drain voltage then you do not have much change in the current.

That helps it behave like a good current source or an ideal current source, close to ideal current source. If the lambda is very small in the curves in the saturation region are very flat, it becomes all the better right this is becomes more closer to the ideal current source. If lambda is large then the curves slope will be large and then for a given fixed V G also

you will get significant not change in current even when the transistor is in saturation. So, then the current mirror becomes a bad current mirror.

So, such thing is we should have direct connection for this and in order to have relatively flatter curves there are certain options that we have discussed. Lambda is a parameter that is not available to the circuit design, lambda is a process parameter. So, a particular fab will give you the a device which is having the certain lambda that is not in our hand, but we have seen another parameter that can help us in keeping this curves flatter, that is L. So, if you use larger L, delta L by L goes down and as a result the curves becomes flatter and you can have a more constant slope in this region. That can help us in getting current source or that can help the m 2 behave closer to an ideal current source.

So, later we will discuss some techniques where, we can have even better small signal output impedance even flatter curve without increasing the L. That is the concept of cascade current where probably we will look in to it today if time permits. Another important point that another important point that I would like to mention is, the 2 PMOS transistor in a integrate circuit environment. They can be match to a good extent.

So, in the beginning I mention that in this device we have a problem. The V d is not very well defined because you know the parameters of m 2 and m 1 they are all very well matched. So, we will try to derive what is the relationship or V d in this case we just did it for the case when we have a ideal current source, but now if I have this m 2 then how do we obtain the expression for V d that is another question.

So, let us let us do that, but the key point is that m 1 and m 2 are 2 different kinds of transistor, PMOS and NMOS. Their parameters, their threshold voltages cannot be very well matched. But in an indicated circuit environment, threshold voltages even effectively the lambda of 2 PMOS transistors or 2 NMOS transistor they can be pretty well matched. And there comes the concept of layout, how do you do a physical layout of 2 PMOS transistors that you want to matched.

Likewise, if you are having a differential amplifier there will be going towards very soon you need to match the NMOS transistor for the differential pair. So, there we have the concept of layout or the common centroid layout through which we can ensure good matching between 2 PMOS transistor or 2 NMOS transistor.

But we cannot have we can ensure good matching between NMOS and PMOS transistor. There is another important point we should keep in mind. So, we can have good matching between 2 NMOS or 2 PMOS using common centroid layout. I hope this will be covered in little bit more detail later in this course, but this is another distinction that we should always have in mind.

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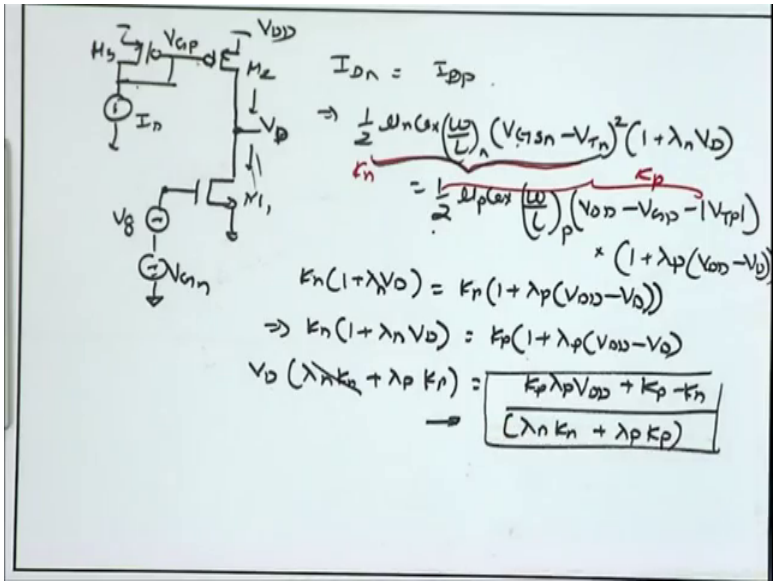

Now if I try to, as we did it for the earlier case and we have an ideal current source, if I just try to once again see; what is the dependency of the drain voltage in case of this non ideal current source, and try to derive the relationship. Just to confirm what is going to happen if we are having this current mirror based biasing. So, we are trying to make m 2 mimic the current source, and then we have the m 1 which is the input device on the top of that we are applying the small signal, we have the dc bias V G and so on.

So, what is the relationship of V d in terms of the device parameters and the dc voltage that we are having? So, here V GP is fixed because of this reference current source we just saw how to calculate V GP for a given I D and likewise the capital V G n is also fixed. So, the dc condition or dc gate voltage of m 1 is also fixed. Now we want to find out what is the relationship between the V D and device parameters, I can just equate the current through NMOS and PMOS. I can write down I Dn is equal to I DP.

And there once again if I just put in the equation which is V GS n minus V Tn square 1 plus lambda n V DS n. Now V DS for m 1 is just V d which is equal to 1 upon 2 mu t c o

x W by L t. V sg which is V DD minus V GP minus mod V TP times 1 plus lambda p times V SD, V SD is once again V DD minus V D.

Now, here what are the constant term? So, this entire first term is a constant term. V GS n is fixed by the dc bias, v t is fixed. So, this entire term is a constant term likewise here V DD is fixed, V GP is fixed, V TP is fixed, and this is another constant term. Based on these 2 constant terms I need to find out what is the resulting V D. V D is the unknown that we are trying to find out. So, I can represent, I can call this entire term as K n I can call this entire term as K p, and then I can try to solve for V D. So, K n times 1 plus lambda n times V D this should be equal to K p times 1 plus lambda t V DD minus V D. And then we can take the K n on the one side and we have the equation for V D. So, if I express V D in terms of these device parameters I can bring this constant at a down over here. And therefore V D becomes lambda n K n plus lambda p K p.

This is the expression for V D that I obtained in terms of K p K n lambda n and lambda p. Once again if you look at what is K p n, K p n is V GS n minus V Tn likewise, V DD minus V GP minus mod v t p. So, here we have the term V Tn V TP which are which can vary the threshold voltages of NMOS PMOS they are not very well defined, their ratios they can vary. As we said 2 PMOS or 2 NMOS we can ensure good matching between the v t of 2 PMOS or 2 NMOS, but not between the v t of 2 one NMOS and one PMOS.

Therefore, in this case the ratio K p upon K n we cannot ensure a good matching now stable value. It will depend upon the process parameters in the variations. And on the top of that we have the lambda n lambda p directly coming in the denominator. So, this whole thing is scale by lambda n and lambda p which is once again highly process dependent it can vary very significant from device to device.

Once again the purpose of doing this analysis is to very clearly understand that V d is going to be highly sensitive to process parameters of m 1 and m 2 on, which can vary significant from device to device and we do not have much control, we do not have very well way of very good way of specifying the ratio. It can have 20 to 30 percent variations and as a result the V D can very, very significantly because it is strongly dependent upon lambda. So, once again we cannot ensure that m 1 as well as m 2 will be in saturation region either m 1 can enter into triode, or m 2 can enter in to triode. V d can go very high or it can go very low depending upon all these parameters. Even if you ensure K p equal

to K n by tuning then we have the lambda n lambda p terms left, which are not very controllable.

The key message here is whenever we are having active load we are having this problem of biasing the output node voltage V d, we do not have much control over the V d; so now, here if I want to go back and do the small signal analysis.

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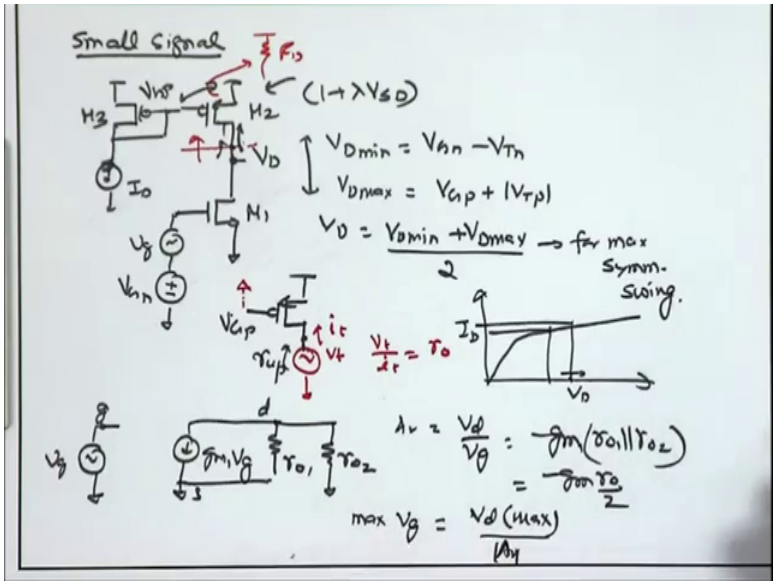

This is regarding the dc analysis. So, we are facing one problem which is related to the appropriate biasing of V D. So, we will see how to solve it, when we come to the differential topology. So, whatever we are doing now we are building the base for our differential amplifier and op-amp analysis. Whatever we are doing here will be applicable there. So, here also there are certain mechanisms through which V d can be fixed.

One example is, you can just use a very large resistor over here, R g this can help us in establishing and appropriating dc bias for V G. You can think of it why? Because in this case the dc voltage at the gate is going to be same as the dc voltage at the drain provided you having ac coupling over here. Probably we will solve some example from this and we will see whether it is possible to establish a good dc bias in this case by using large R g.

But in general here we are trying to just do the analysis which will be carried further in the analysis of differential amplifier. Where establishing a well defined V d is relatively simpler and we will see how to do that. Now how do we go to the small signal analysis for the amplifier that we just discussed? Now once again we drawing the circuit quickly, current mirror branch, assume that somehow you have been able to fix V d to the required value and you have the dc. Now when talking about the small signal we are changing the gate voltage increasing or decreasing by small amount.

And as a result we expect the output to reduce or increase by a large amount because of the phenomena we just discussed right. We are trying to increase this gate voltage and therefore, V GS is increasing and in order to establish current this m 2 will try to have try to maintain the same current because for this V sg is fixed. And therefore, the only way m 2 can increase the current is by reducing the V D. So, that the V SD of m 2 goes large. So, if you are trying to increase the V G of m 1 this has quadratic dependence. So, I D 1 should increase, but for m 2 V sg is fixed. So, how does it increase the current because if current in m 1 increases, current in m 2 must also increase?

So, the only mechanism for increasing the current in m 2 is to reduce V d. And therefore, increase the 1 plus lambda V SD term for m 2 that will enforce V d going down whenever you are increasing the v g. So, that is the basic mechanism how we get gain in this circuit with active load. So, before we do any small signal analysis, we draw that ac model it is important that we visualize what is happening in the circuit physically what is happening in the circuit. Because this gm and this R o they are they are small signal parameters mathematical models derived from the real device phenomena. So, it is important to understand; what is the real device phenomena first, and if this is clear then other things like the small signal ac noise everything will be relatively more clear.

Now, before we draw this small signal model another important consideration is the signals field. So, we have discussed in the case of resistive load also. What is the maximum and minimum possible drain voltage that I can have over here? That leads to the maximum signal swing that I can have at the output node V D. So, here once again in order to maintain these m 1 and m 2 in saturation region so that we are having large you know impedance provided by here m 2 and also the m 1 is in saturation region giving us large region and large gain. We must make sure that now the drain voltage is ensuring saturation region operation for both m 1 and m 2.

So now, towards the lower side when the V d is going down because of an increasing v small V G the n 1 will be in trouble because the moment V d goes down below V G n by V Tn, that n 1 will be entering in to triode region. We can write V d min is going to be equal to V G n the dc voltage over here V G n minus V Tn. If the V d goes below this n one is going to enter in to triode region. Here we are ignoring the small V G n and compare them with the capital V gm the dc condition, that is the fair enough assumption provided the gain of this stage is pretty large larger than 10.

So, for given V G a n if the V d goes below V G n minus V Tn, n 1 is going to enter in to triode region. This is the minimum V d allowed likewise, what is the V d max n? So, the again if your drain voltage is going more and more positive the PMOS will enter in to trouble, right? Because in order to make sure that n 2 in saturation V d must be less than V GP, call it V GP plus mod V TP, that is what we had discussed earlier yesterdays class. So, V d max is going to be V GP plus mod V TP. The moment V d goes higher than V G t plus mod V TP once again we are in trouble.

This is the range of V d max to min. Now once again if we have target that we want to have maximum symmetric swing and therefore, we want to bias the V d, we want to have V d exactly midway between these 2 extremes so that the signal can go up and down by same amount. That is call maximum symmetric swing condition and under those conditions you would like to have V d equal to V d min plus V d max by 2. That is the ideal you know best possible swing for max symmetric swing at the output. So, this is about you know dc analysis and the swing.

Now let us look at the small signal and try to analyze the small signal model or small signal equivalent circuit for this amplifier. So, one of the strategy you should do small signal analysis in this case would be to look at the drain of m 2. Below m 2, we just have a common source amplifier, m 1 is just acting like a common source amplifier only thing is earlier we had R D we had some resistance over here R D and that has been replaced by PMOS. So, if we can find out what is the small signal resistance looking into the drain of m 2, I can replace n 2 with that small signal resistance.

In case of R D remember it is a passive resistance there is no difference between the small signal and large signal resistance of a passive resistance. Both small signal as well as large signal are R D just simply R D. But in case of a MOSFET definitely we are

talking about the small signal resistance which is not same as the large signal, if you define if you are force to define large signal resistance as capital V DS upon capital I D that is not the same as the small signal resistance. So, we need to look in to the small signal resistance at the drain, whenever we are talking about the small signal model or small signal amplification.

So, what is the small signal resistance looking in to the drain of m 2? That we have already seen yesterday. If you are looking in to the drain of a PMOS transistor or an NMOS transistor with gate voltage fixed to V GP. V GP is being provided by this reference branch remember the purpose of this diode connected branch is to produce a reference V GP which is applied to the gate of m 2. So, this V GP is at a constant dc voltage there is no signal over here. And therefore, in terms of ac I can put it at ac ground.

And therefore, if you are having the gate of a MOSFET at constant voltage and looking in to the drain you are trying to inject some v t and trying to find out what is the I t we had seen it is going to given by r o. So, V t upon I t the small signal resistance is given by r o. So, we should always have that output characteristics in nine. So, if I am fixing the V d and we are trying to change the V D by little bit in this case, we are going to get small change in the current and the slope of this curve is going to give me the inverse of small signal resistance. So, we should always have this in mind that the small signal resistance looking in to the drain of MOSFET that the gate voltage constant is going to be r o.

So, I can just replace this by the small signal resistance r o. And in that case I can draw the small signal model for the MOSFET as gate voltage is having small V G, drain to source we are having gm V GS which is just V G because s is grounded. So, gm V G for m 1 we are going to have the r o of the m 1 coming between the drain and the source of m 1 which is ground. And once we had just seen that the small signal resistance of m 2 looking in to the drain of m 2, we can call it r up, r up is just going to be r o 2 of m 2. That is coming between the drain and ac ground because that is the small signal resistance looking in to the up drain upward that is between the drain and the ac ground.

So, once again r o to comes between drain and ground, and therefore r o 1 and r 2 are in parallel I can write down the small signal gain av is equal to V D upon V G that is this entire gm V G if flowing in to the parallel combination of r o 1 and r o 2. Therefore, this

becomes minus gm times or rather gm 1 times r o 1 parallel r o 2. If r o 1 and r o 2 are equal, which is not going to be the case usually, but just for getting the expression that assuming gm 1 gm 2 are equal r o 1 r o 2 are equal. So, what is the order of the gain? So, we can say it is the order of gm r o by 2.

So, once again very close to the intrinsic value gm r o, only thing they reduce by factor of half. So, expression is similar to what we obtained in case of a ideal current source, but by a factor of half because now, you have to account for r o 2 also. In case of ideal current source the small signal resistance looking upward was infinite therefore, r o 2 are infinite therefore, only minus gm r o 1, but now you have r o 1 parallel r o 2 that is a only difference. So, once again we have seen the dc analysis we have seen the swing what is the maximum signal swing I will, I will have at the output and we are looking in to the small signal gain.

Now, from this swing and the gain information I can also figure out what is the maximum input signal swing that can be allowed in this case. So, max V G that is the input signal can be written as max V d max that is the maximum output signal peak to peak output signal that we have just found out divided by the gain magnitude of the gain. So, that is in this case gm r o by 2. So, the max output signal we already seen, maximum value V G plus mod V TP minimum value V G minus V Tn.

And therefore, the maximum input signal that I can have is max of the signal divided by gain of the circuit, mod of the gain of the circuit. And once again if we want symmetric swing if we want to exploit that maximum possible signal then the V d should be biased close to the midpoint of these two extreme values. So, this is regarding the small signal operation and freq of the active load common source amplifier.

Now, let us talk about the frequency response how do we deal with the frequency response of this active load.