Analog Circuits and Systems through SPICE Simulation
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Lecture – 06
Basic Analog Design Part III (Contd.)

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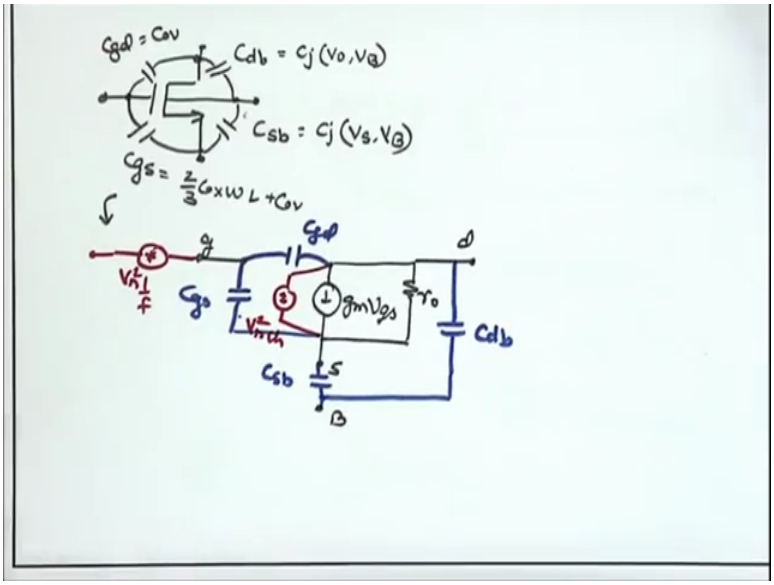

Welcome back and now we have the basic recipe I device table already. We have gone to the basics characteristics of the MOSFET from there we have understood how to arrive at the small signal parameters of the MOSFET at lower frequency. Then we have looked into the parasitic capacitance they are physical origin, how do they affect the signal propagation through the device? And finally, we have added the noise source to the device looking at the physical origin and also incorporating them in the small signal model.

Now, we are ready for analyzing circuit is using the model that we have developed. So, let us start with our discussion on a simple circuit, video common source amplifier with a resistive load and try to carry out these basic operation. Remember if start with we discussed 4 basic operation, first is the DC analysis. The first is the DC analysis, second is small signal.

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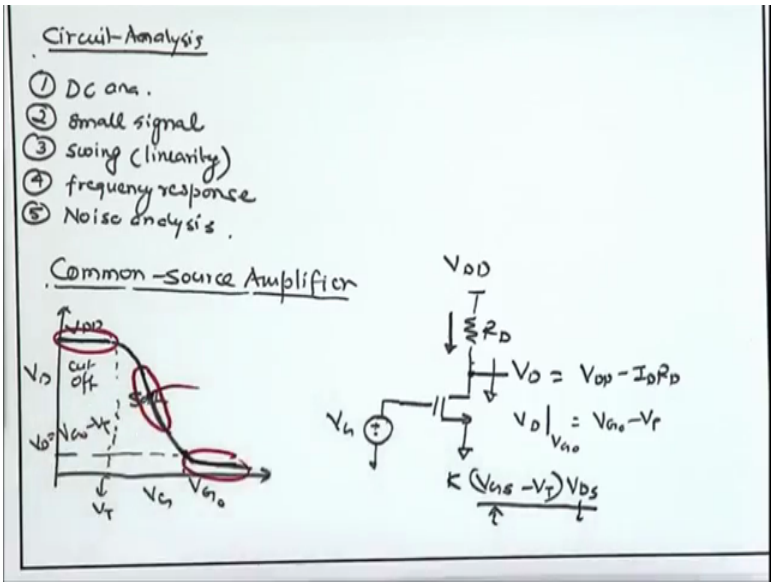

We also need to take care of linearity of swing, signal swing or linearity. We will discuss you know what is the significance of swing and what do we mean by linearity. Linearity in itself is a more involved concept here we will go for a slightly cruder definition which is signal swing and finally, frequency response and at the end noise analysis.

So, using the concept we have developed so far at the wise level we are in a good position to be able to do all this analysis, carry out all this analysis for a given circuit. So, let us start with a simple circuit which is a common source amplifier with resistive load and carry out all these analysis. So, first we will be looking at the DC characteristics. Here applying a grid voltage V G, you have some R D and you are looking at the V D. So, if we try to plot V D versus V G. So, what kind of curve do we except? We know that as long as V G is lower than V D of the MOSFET there is hardly any current, the current is negligible I D is 0 therefore, the V D is going to be just equal to V DD.

So, we start with V DD it will remain clamped to V DD till we reach V G equal to V T. Beyond that point if I go on increasing the grid voltage further, our current is going to increasing and the V D can be written as V DD minus I D R D. So, this is cutoff region right? Because MOSFET is cut off, V G is lower than V T there is hardly any current. Beyond this point if I see the drain voltage is starting to fall as the current is increasing and V G is increasing beyond V T, but still V D is much larger than V G minus V T, right? So, for saturation region operation the condition is the V D should be greater than

V G minus V T. It is just started the fall down and will go on falling in this entire region will have saturation region operation of the MOSFET.

So, you will have a steep curve as you are increasing the V G the I D is increasing as per square log and you are going to get a steep increase reduction in the drain voltage. So, we get a steep reduction. Beyond a certain point when you reach a say V G not at this point suppose, the drain voltage after falling so much the condition has reached where V D at V G not is equal to V G not minus V T.

So, beyond that if you increase V G further differently V D is going to drop below V G minus V T and it is going to enter into triode region. And in the triode region your equation is going to be governed by V G as minus V T into V D S if I ignore the small V D S square suppose V D S square by 2 is ignore because of we doing small. So, this is the expression that we get in the triode region. Beyond that point if you try to increase V G further, you are trying to reduce V D S further because if V G s increases I D supposed to increase and it is supposed to reduce the V D S. And therefore, this is trying to increase, but this is reducing, as a result these 2 factors will cancel out each other and the current will saturate it go very small you know value finally, and you are having a triode region operation the voltage over here the approach close to 0.

So, here in this region we have saturation region operation in a large slope and finally, at the point where V D is equal to V G not minus V T is reached, we are hitting the triode region and beyond this point the MOSFET is in triode region. So, you know that if you are trying to operate this as a digital inverter. So, the region of operation happens to be either the cutoff region or it happens to be the deep triode region, where the input voltage sufficiently high.

So, definitely this is you know, probably the first integrated circuit inverter or digital inverter that people had used before the implementation or immention of CMOS technology. Because at that time the only constructor available was NMOS and this is this was invert or implementing the inverter, as a MOSFET of for that those days it should be BJT, but this was the first inverter and this is the inverter characteristics. If you apply input voltage which is very close to 0, digital logic level low output is closed to V DD and if your input is much higher than a certain value close to be V DD, the output is close to 0.

So, this is the inverting operation, and for inverting operation we use these 2 domains. Digital inverter we used these 2 domains, but in order to have another operation we are supposed to get a sufficiently large signal then from input to output; that means, if I am changing the gate voltage over here by small amount, that is I am putting a small ac signal in series with this gate my drink voltage should also changed by a large amount. And that will happen when the V out by V in slope, that is V D verses V G slope is having magnitude larger than 1. And this is the in this curve the central region of course, is having maximum slope and therefore, it is going to me maximum possible gain. Therefore, I would like to bias my transistor in the saturation region, I will try to find out the operating point such that it is in saturation region.

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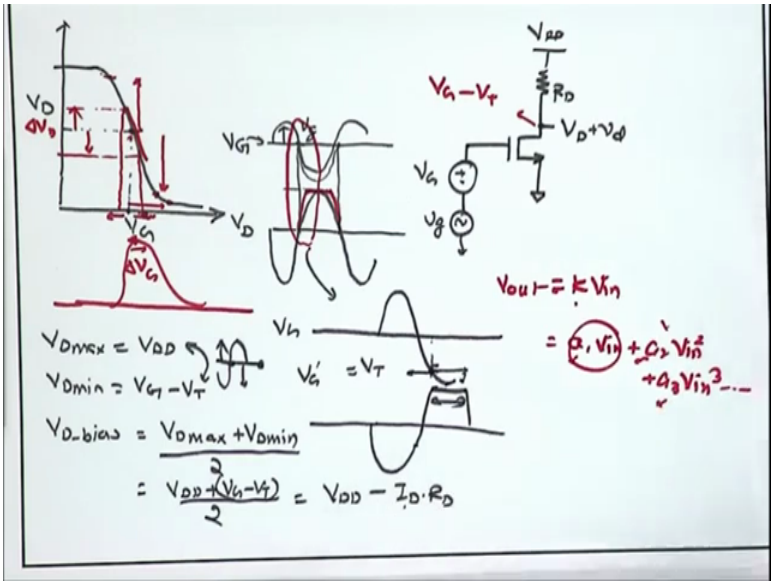

So, let us look at the biasing consideration. Capital V G denotes the DC value small V g the small signal that you are applying on top of this and your R D once again capital V D, the DC and small V D. Now if you talk about the best possible biasing point we need to look at the certain consideration. One is definitely the gain and we see that in the central region we are going to get possibly largest gain. Another important consideration able to be swing, signal swing that is available to us. So, if I look at the DC voltage at the gate that is suppose capital V G we are fixing the DC bias point, in order to operate this circuit as an amplifier the first thing once again is to fix the DC operating point or the DC bias.

So, we fix the V G. So, corresponding to that I also have the V D fix the, the DC voltage at the gate and DC voltage at the drain are getting fixed. And on the top of that I am going to apply a small delta V G plus minus and corresponding to that I accept my V D to change. So, if I reducing my V G the current reduces and the V D goes high, if I am increasing my V G current increases V D goes low. And the slope over here determines what is the changes in delta V D in both directions when I change my grid voltage at delta V G. So, the slope is significanttly greater than one; that means, we are going to significant not gain.

Now, one of the requirements that we have for good amplification and single swing is that, the amplifiers would be the transistors should be always in saturation region. The moment it goes out of saturation region we are going to get poorer gain. We have seen that the moment you are at this find the slope of this curve is almost dead and therefore, if you are biasing the transistor over here the saturation the gain is going to be very poor. Likewise if you are biasing the transistor over here the gain is going to be very poor.

Now, if you are biasing a transistor over here you have certain (Refer Time: 10:48) on the positive side you can increase your output signal to this point without significant distortion likewise, you can reduce your output signal to the corner point over here without significant not distortion. So, this curve tells me what is the maximum room available for my signal on the positive side and on the negative side at the output terminal. So, as compared to the V G if I say my, as compared to the DC gate voltage V G my input signal is going up by small V g corresponding to this I this is the DC level V G corresponding to this my V D is going to you know have the opposite exertion, but magnified. So, what is the maximum value that the V D can take without getting distorted. That is the of course, the V DD because maximum supply available to you in the circuit is V DD. So, it cannot go beyond V DD. So, in case your input signal is going so low that the MOSFET at a particular point hits the output voltage at a particular point hits V DD, when definitely at this point it will become clamp.

So, if I magnify this region, what is happening? If I just look at this region where this clamping is taking place. So, my input signal is going sufficiently low it may hit V T right. So, input signal suppose it goes. So, low that the overall voltage over here capital V G plus small V g is getting lower than V T. In that case definitely whatever point suppose this was your V G and your input signal hits V T over here. So, this is your V G

or you can say the instantaneous V G I can call it V G dash, which is hitting V T at this point. So, at this point my current is almost 0 and therefore, the output voltage over here, corresponding to this point it will hit V DD. And for the rest of the signal which is below this it will remain V DD right. So, you are getting the signal clipped at V DD. Therefore, the maximum output signal that I have it is V D the maximum output signal V D max I can have is V DD. What about V D mean? Or V D mean, what is going to happen if I go on increasing the positive peak of the single? If I go on increasing the positive peak of the signal, we can see this curve what is going to happen, if I increase the delta V G further and further and go on to the positive side ultimately the output is going to be too low and it is going to be triode region. Once again the gain is going to be hampered and therefore, in order to make sure that the transistor is in saturation even for the worst case when the gate voltage as sufficiently increased, I must make sure that the drain voltage is sufficiently or minimum value drain voltage is equal to the voltage required to keep the transistor in saturation.

If I ignore this small signal at the gate which respect to this DC gate voltage, what we have seen is the minimum drain voltage allowed to keep the transistor in saturation is going to be V G minus V T. The moment drain voltage goes below the V G and V T we are pushing the transistor in triode region. So, what we can say is V D means is going to be V G minus V T. Therefore, we have this range from V DD to V G minus V T, by signal can go maximum up to V DD it can go minimum up to V G minus V T.

So, if I want a sinusoidal signal at the output so that it can have symmetric swing on both sides, means the peak to peak signal is symmetric across a DC point, I want equal room for the signal on positive side as well as negative side. With respect to the DC bias point. So, what is the point we will choose? That will be the midpoint between these 2 swings. So, V D I would say bias should be equal to V D max plus V D min by 2 which in this case is V DD plus V G minus V T by 2. And based on this I can decide what is going to be the R D value because this V D bias is nothing is, but V DD minus I D times R D.

So, this DC bias current I D and R D determine what is my V D. So, from this equation I can find out what is the R D value required to get a DC bias point at the drain which is allowing maximum symmetric swing on both side as compared to the DC point. So, if I choose R D according to this equation my output signal can go up and down by the same magnitude without pushing the transistor into triode region or the cut off region. So, that

is the crude definition of signal swing you know, why crude because this is just ensuring to the first order that the transistors going to remain in saturation region it is not going to enter cut off it is not going to enter triode.

But definitely there are more serious considerations related to linearity and distortion that we make our it was the end for the time being we are skipping that discussion in favour of the time. So, remember that for a good amplification what do we really want is that slope should be perfectly linear should be constant. But no way you can get the slope constant in a practical device, if you plot the slope it will be kind if picking in the center if I just take a reading from a device in the lab and try to get this characteristics and plot the slope it something like this. So, the slop picks at the somewhere in the middle and then again dies down. So, the gain or the slope is not constant and the result of which the gain itself the slope which remains the gain itself is dependent upon the V G or it is dependent upon the signal swing.

So, if you are signal swing is only at this point the gain experience will be different the signal is going to little further that part of the signal will experience different gain. So, different part of the signal will experience different gain and that leads to non-linearity this is not a constant function. Ideally I would like my V out to be equal to K times V in ideally K should be constant independent of v in, but here K will not be independent of V in. If the V in is larger magnitude is slightly increasing the small signal magnitude, the slope since the slope itself is dependent upon the absolute input value, this is start depending upon V in and this is no longer be constant. Therefore, V out is not longer linear function of V in where we get all kinds of harmonic come into picture. So, we can more accurately represent it as some, if I just look at this small signal it will be a 1 times V in plus a 2 times V in square plus a 3 times V in cube and so on.

So, if you if you look at this curve you can find out the fitting function which is satisfying this equation and from their you can find out the values of a 1 a 2 a 3 which is repeating the overall transfer function. So, this is the real picture that we get. We want only the first term, but we are getting all kinds of other higher order terms which are not desirable which are distortions and this lead to harmonic distortion. So, if you are inputting a sinusoidal of sin omega t and you should having the second term a 2 times V in square and it is going to lead to sin 2 omega t term, this is going to lead sin 3 omega t

terms and therefore, you are having harmonic distortions. You are having harmonics of the input signal present at the output which is undesirable.

So, this concept of harmonic distortion you know becomes very important when we are talking about high resolution signal processing. So, definitely we will come back to this concept of non-linearity in harmonic distortion when we approach our discussion on the front in amplifier and a DC. For the time being this is we do that will be based on this relatively cruded definition of maximum signal swing at the output where the only justification that, we need is keeping the transistor in saturation region.

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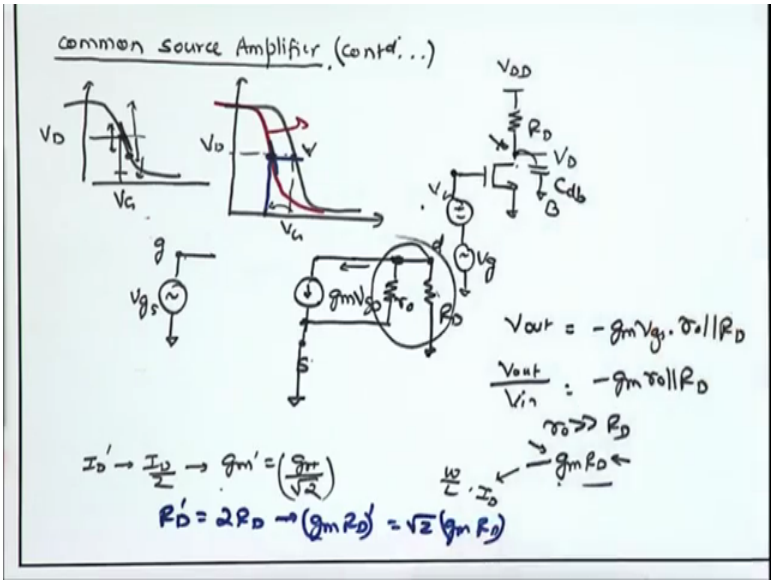

Making sure that the transistor is not going off or it is not entering into triode region for lower and higher excursion of the input signal. So, that is the point we are going to analysis for the time.

The DC biasing or the common source amplifier. So, what we have seen is that we are going to require appropriate twice of V G and V D. For a given V G we are going to get DC operating point and we wanted to set this V D to the midpoint of the extreme allowed voltage of V D, V D min and V D max and how that is determine the R D. That is the first step in the second analysis we are find to find out the DC operating point of the circuit is by appropriate analysis.

Now, let us go further and try to look at the small signal model of this circuit is and figure out the small signal analysis. So, for this circuit is I would say the simplest possible circuit is analog electronics and we are just going through some essential steps, which is going to be repeated for more complicated circuit is like differential amplifier 2 stage amplifiers and finally, the complete analog front end. So, this is just an example case we also need to discuss in detail the common source amplifier with active load that is another important concept that is going to be used in building the front end amplifier that we are looking into. So, once we have appropriately set the value of V G and the V D so that my transistor is biased in the high gain region.

So, I have a certain correct choose of V G corresponding to that I am having a correct choose V D so that I am my DC point is at point in this curve where the slope is large and little bit of change in V G is going to me a large change in V D and therefore, large gain. Now on the top of this if I want to do the small signal analysis I can look at the MOSFET model first. The first step happens to be drawing the MOSFET model here remember that we are ignoring the body terminal. So, I am drawing the body terminal assuming that the body terminal is grounded, somebody pointed out that we should have included the gm b term, but just to keep things simple we are ignoring that effect for the time being

So, assuming that the body terminal is grounded we will be looking at how to include the parasitics also. So, this is the model of the MOSFET that we have, at end 3 terminnals gate source and drain. And now we have to look at the connectivity between these terminals and AC ground. So, first thing is what is appearing at the gate. So, at the gate as we said we have some DC bias which is capital V G on the top of that we have a small V G. And in order to look at the small signal we can set this capital V G to 0 because this is a DC it is not having any small signal I can directly put a small V G over here and that appears between the gate and the AC ground. Likewise at the source we directly have the AC ground in this case, gate is grounded, source is grounded r o appears always between the drain and the source.

So, common mistake in paper that we correct often is that people draw r o between the drain and the ground even if the source is not grounded. So, it should always be taken care that the r o appears between drain and source and not between drain and ground. And then finally, we have R D between the drain and the V DD which is again between

the drain and the AC ground R D. And therefore, in this case it is you know simple to solve we do not even need to solve any K C L K V L. We can see that whatever V G is appearing over here that is effectively V G s because source is grounded therefore, gm V G s is going to flow into the output node. And that is going to flow in this parallel combination of r o and R D therefore, the voltage over here is just going to be gm V G s that is current multiplied by r o R D.

So, this is 0 0 minus r o parallel R D times gm V G s. So, V out in this case is nothing is, but minus gm V G s times r o parallel R D because this is a parallel combination r o R D appearing between drain and the common AC ground. And the voltage here is the total current flowing through r o and R D parallel combination times that resistance. And therefore, V out by V in is just minus gm r o parallel R D. And if r o is much, much greater than R D which is generally the case in the designs R D that we are choosing may be is anything is lower than r o in general, we can just approximate this as minus gm R D.

So, in this circuit is if I say what are the mechanisms that are available for us to increase the gain. Either we can increase the gm or we can increase the R D. So, if we increase the gm again what are the options available to us? Either we can increase the W by L or I can increase the r I D. So, once again when I am for a given R D if I increase I D what we are going to have is the drain voltage a DC voltage as a drain is going to go down. And therefore, we are going to have limited swing available. So, we said that V D needs to be midway between the V DD and V G minus V D so that we have symmetric swing available on both sides.

If you are increasing the I D the drain DC voltage goes down, it can come over here and it can reduce the swing available in the lower directions. Same thing will happen if I try to increase R D while keeping I D constant. So, let us keep gm constant and increase R D. So, once again if you are increasing R D once again the DC drop across the R D is increasing as a result of which the room available will be reduced. If we want to here maintain the, maintain the signal swing one of the possibility is, but I reduce the I D. So, suppose I reduce the I D make it half. So, I D dash is I D by two; that means, by gm dash is going to be gm by root 2 because gm is proportional to root I D.

Now, corresponding to this of course, I am swing that my gm has gone down. So, can it help me in achieving larger gain while maintaining the signal swing at the output? So, here is my I D is reduced to I D by 2 I can increase my R D to twice while maintaining the same DC point at the output. So, I was at this point to begin with I had a certain I D, it was I had a certain V G and V D and therefore, I had you know bias my amplifier the midpoint lower and higher side we have equal room. But now if I reduce the I D by 2, I D to I D by 2 then of course, I can increase the R D by the same factor to go back to the same DC point V D. And what does that mean effectively is, in this curve how will be obtain is how do we you know rationalize this? So, if I look at the original curve, this was the original curve I was at a midpoint of the 2 extremes and I had certain you know, certain V D and a certain V G this was my DC operating point.

Now, what I am saying is I am going to reduce my current by half. So, basically; that means, that for this MOSFET if I follow square law; that means, I have to reduce my V G by some amount. So, that V G is minus V T square is reduce to half or the DC current is reduce to half; that means, of course, I am shifting I, I am going towards lower values of V G, I have to reduce my V G. So, in order to reduce the V G I can parallely you know increase the value of R D because my requirement is that the DC point should be midway.

So, if I increase my R D what happens to this curve. This curve basically becomes deeper. And therefore, for a larger R D once again at the desired V G I will have my new DC operating point and in general this slope will be almost you know similar to, but we have over here. So, what we are trying to do is, we are trying to play bit the DC bias current and the resistance to increase the gain while maintaining the required signal swing. Remember the target is that we should keep the DC bias point midway between the 2 extremes. So, we reduce the current to half and increase the resistor by double so that the DC point at the output is same. As a result what is happening gm is reduce to by root two, but R D has been reduce to R D dash is now 2 times R D therefore, this implies that the gm R D if I call it gm R D whole dash, that is a new value of gm R D that is going to be root 2 times initial value of gm R D.

If we can see that by appropriate choose of R D and the bias current I D we can definitely increase the output gain, while you know maintaining the same signal swing without disturbing the maximum signal swing at the output. Definitely we do have the

dependency of many other circuit is matrix on gm and also R D. So, intuitively speaking we have seen that the MOSFET is having parasitic capacitance, and when you increase R D in t his branch the time constant for example, resulting from the parasitic capacitance between the drain and ground C db which is going to appear between drain. And body, body is grounded therefore, C db is appearing between drain and body. So, if I just look at this capacitance and R D V D that the r c times constant at this node and going to go up as a result the circuit is going to become slower if I go for larger R D that is going to slow down my circuits.

So, although I have manage to increase my gain, but I am suffering with the bandwidth, my bandwidth will be going down because of this capacitance behavior of the MOSFET. Likewise we have also seen that gm can play important role in determining the noise. So, if your gm of the input device is you know going down although you are trying to maintain the similar gain, but once again the input preferred noise can be deteriorated.

So, once again we have stringent trade off with other parameters. You are trying to adjust one of the parameters, trying to increase the gain while keeping the swing same, but other parameter like the bandwidth and the noise they are going to degrade, linearity is going to degrade. So, we have to take care of the requirement in the design, while optimizing one parameter we have to make sure that we are still meeting the other requirements. So, here while you know, reducing the I D and increasing the R D we are managing to get larger gain and keeping the swing same, but at the same time we are going to deteriorate the bandwidth we are going to deteriorate the noise. So, in general this is a general test in the analog design. We are trying to meet a certain aspect you are make sure that all these different aspects gain, bandwidth, noise, linearity, swing, slew rate all of these are getting met. If you are try to tweet with one of them something else will be getting messed up. So, this is a small example regarding the DC analysis of the common source amplifier.

Thanks a lot.