Analog Circuits and Systems through SPICE Simulation

Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture – 03
Basic Analog Design Part – II

Welcome back after the lunch, so we will continue from the point where we left. And I will finish our small signal; model low frequency small signal model.

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So, looking at the concept of channel length modulation I feel; looking at some of the questions that have come up our screen most of the questions I have already addressed. So, questions regarding the significant of few things some gm and ro description of channel length modulation. Also there are some general questions that we have received regarding these concepts and most of them have already been covered.

Another important question that has come up is regarding the difference between NMOS and PMOS; whether they are DC characteristics or the small signal characteristic are significantly different or same how do we capture those in the module. So, this is another question we are going to address shortly. And definitely in between we will have interaction session we will keep it open so that whenever there are good number of questions collected we can try to have interactions with you.

So, let us continue with our discussion. So, this is a equation that which we stopped. The equation which is capturing the channel length modulation the effect of lambda and which is going to give us a finite dependence of the drain current on the drain voltage V DS. So, ideally as we said in saturation region the current should be just dictated by the V GS minus V t, but because of the effect of channel length modulation we have finite dependency V DS and that gives us a finite output impedance; small signal output impedance looking into the drain, that is what we saw earlier.

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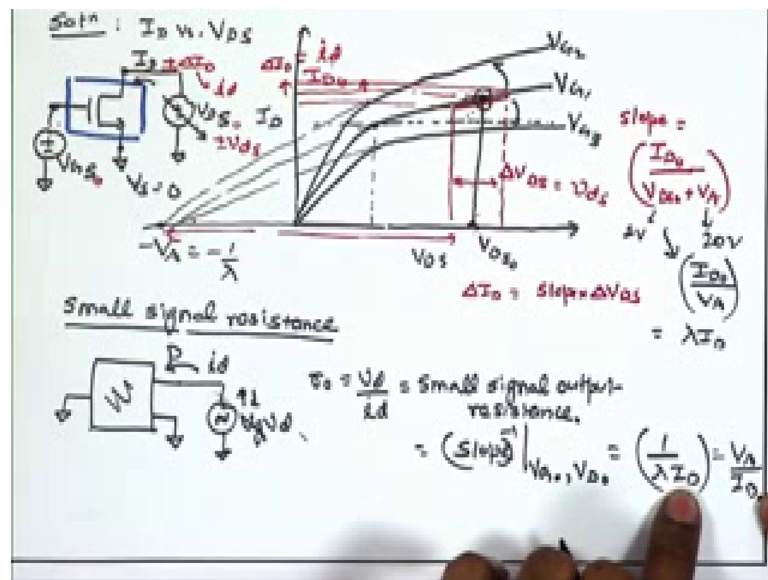

So, if you recall our discussion we were talking about the small signal model where we are applying some six small signal voltage at the drain of the MOSFET and trying to see what is the resulting small signal current.

So, whenever we talk about small signal; that means we have a DC on the top of that DC we are changing the voltage little bit and we are looking into the little bit of change in the current; what is that small change in current resulting from small change in voltage. And in order to define the ro what we did is we looked at the MOSFET from the drain side the gate is constant it has the constant DC. So, we have just assumed that from AC point of view a constant DC source is grounded, so there is no small signal in the ideal DC source that is grounded. Sources at the reference point that is also connected to DC ground, so this is also grounded.

And we are looking at just the third terminal and trying to find out that if at this third terminal I am applying a small signal V D what is the small signal id flowing into the input (Refer Time: 03:03) or into the drain terminal of the MOSFET. And that gives us the small signal resistance. And we have seen from the curve as well as from the equation that is going to be equal to inverse of the slope which is equal to one upon lambda id

So, if you are having smaller and smaller values of id; that is the DC bias current we have smaller and smaller slope and hence higher and higher output impedance. That is evident from this graph also if you see V G1, V G2, V G3 are three different gate voltages for a given drain current. And if we are lowering the gate voltage V G3 the DC gate voltage we see that the slope reduces another result the impedance increases. So, that is evident from this curve also. And like wise if this lambda is also proportional inversely proportional to L, so this is having dependency on L.

So, if your channel length is larger your slope is going to be smaller, because the basic mechanism is that you are getting a fractional change in the channel length as we discussed delta L. So, if your absolute channel length of the MOSFET enlarge the delta L upon l will be smaller and smaller as a result the fractional change in the channel length of the MOSFET will be smaller. And hence the channel length effect will be smaller the curves will be more and more flat.

So, in a design where we need to use relatively longer channel length of the MOSFET or you know in design where we need a higher output impedance small signal impedance of the MOSFET looking into the drain we preferably use longer channel lengths. So, in amplification operations then we are applying this MOSFET for building amplifiers we will see that it is important to have higher output impedance. We will see how it plays a role in determining the small signal gain of an amplifier.

And therefore, in many analog application, many analog design people use people stick to longer channel length. They might be using lower technology node they may be using 65 nanometer even 22 nano meter, but often the channel length that is used in the design maybe close to 1 micro meter. So, despite using scale technology in many of the designs specially the analog front end components which are not operating at such high frequencies people may prefer to use very long channel length of these MOSFETs.

So, this is one of the main reasons or one of the main differences between the analog and the digital use of the device. When we are going for digital use of the device, where the MOSFET is just being used as a switch there we are not really utilizing this saturation region characteristics channel length modulation of the device for or operations. The device is really operating as a switch and it is in triode region.

We will see this distinction between the analog and digital operation shortly, but just to emphasis that the saturation region characteristic on the finite slope is very important for analog operation. And for having larger output resistance smaller slope so that the transistor behaves more closely to an ideal transistor; the drain current depends more strongly on the gate to source voltage and not so much on third terminal or not so much on the drain voltage that makes a perfect transistor which is required for analog operation.

So, in this condition suppose we want to come back to this model and try to define what is the behaviour of the output toad that is the drain terminal in presence of applied drain signal. So, you applying the small signal voltage at the drain and we are looking at the small signal current. So, how do we model this? So, we have said that if you are having a small signal vd, you get small signal current which is equal to V D upon id. So, I can say id is going to be V D upon rd where rd is the small signal resistance that we have just defined.

Therefore, we can represent this rd as a small signal resistance appearing between the drain and the source terminal. So, that is how we can model the effect of this finite output resistance shown by the drain port. So, we had just having a black box this transistor you not concerned here about the detailed physics or the equations, we are just looking at the small signal behaviour of the MOSFET. And we are modelling the output port between the drain and the source as a small signal resistance rd, which means that if you apply a small change in voltage by magnitude V D the resulting small current id that flows it just going to be a V D upon rd that is the small signal current id.

So, now how do we combine these two parameters; that we have come across so far gm and ro or rd in order to get a complete small signal model.

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So here, we look at to the overall function of the current. Once again we say that this is a function of two parameters that is V GS and V DS of the MOSFET. So, in saturation region especially we are having these two terms affecting the overall device. So, if I have to say what is the small signal current; this is a function of two variables what is the small change in current delta I D which I am calling as small id resulting from small changing in these two quantities. So, to a first order of approximation if I just take Taylor series expansion I can write this down as del f by del V GS at a particular DC point V GS naught and V DS naught. So, we are calculating the slope at a particular V GS naught in V DS naught multiplying it by this small V GS or that is the delta V GS. So, this is the change in this current because of change in gate to source voltage.

Likewise, I can differentiate it with respect to the second independent variable V DS. Again defined at a particular V G naught V d s naught and multiply this by the small change in drain to source voltage that is vds. So, as we have defined earlier the first term is nothing but our gm and the second term del f that is del id by del vds is something like one upon ro. Because remember how do we define ro that is del V D by del td. So, here the inverse of that del id by del V D that is one upon ro. I can also denoted it as gds because the inverse of the resistance is the conductance small signal conductance seen between the drain and the source. So, I can of the term is as the gds.

Therefore, the overall small signal change in the current flowing from drain to source can be written as gm V GS plus gds times vds right. So, this is what is captured in the combined small signal model of the MOSFET they are at the gate terminal you are applying a voltage small signal voltage V gs between the drain and the gate you do not have any physical connection ideally because it is isolated using an oxide. And then you have a small signal current flowing between the source and the drain that is gm times V gs because of the signal appearing between the gate and the source.

Likewise I have another conductance term I can call it gds or effectively this gds the conductance term is equal to one upon ro and that captures the effect of applied drain signal; if you are applying a drain signal over here vd, suppose you are applying a small signal over here V D what is the effect of that on the overall drain current. So, that next change in the drain current id will be the combined effect of gm which is the trans conductance term coming because of the change in gate to source voltage and the second term is coming because of the output trans conductance or small signal output resistance which is coming because of the channel length modulation factor.

That is how we can justify the combination of these two small signal parameter that we obtained independently while obtaining gm we considered V D was constant, and while obtaining gds or ro we assumed that the V G was constant. And finally, we took superposition of these two small signal parameters combine them to get the overall small signal parameter for a MOSFET.

So, this completes our small signal model of the MOSFET at low frequencies. So, this is the low frequency model small signal model of the MOSFET. When we go towards highest frequency of course we need to take care of certain other aspects that we are going to cover next that is the parasitic capacitances how do they come into picture how do they influence the behaviour. But before we go there we are also going to look at the parallel model for a PMOS. So, this is so far we had done it for NMOS the DC characteristics as well as small signal. So, how does the discussion go with respect to PMOS?

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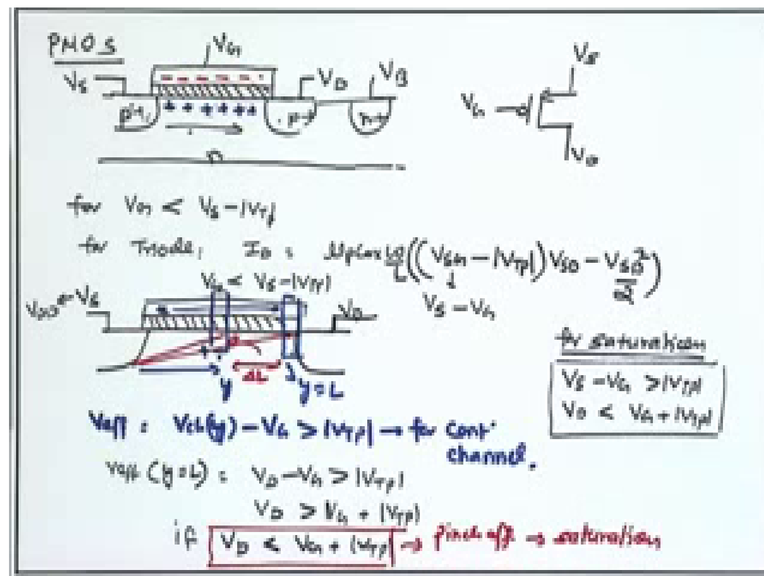

So, do we need to make changes to the small signal model in the DC current equations? So, let us talk about PMOS. So, for PMOS the device structure is just the reverse as we have seen in the very beginning you have p plus source and drain and you have the oxide held before, and the gate terminal V G. You may be having a source voltage which is supposed to be higher in this case and the drain voltage V D. And like wise you may be having the substrate contact this is a n well if you remember we had discussed about the concept of n well and we are going to have the n plus contact coming out this is the V B double contact for the PMOS.

Now, in this case we know that in order to create a p type channel this is the n substrate the source and drain are isolated by an n substrate. So, in the source and drain you have lot of holes, but within this region just below the gate you do not have a lot of holes unless there is some condition reached for the V G. Just like in case of NMOS in order to attract negative charges we had to put good amount of positive charges on the gate then only we were able to accumulate the negative charger and form a continuous conduction channel between the source and the drain.

In this case the condition is just reverse, we are going to form a p plus channel we are trying to have a lot of holes which are positive charges accumulated just below the oxide and to do that of course we need to deposit negative charges on the other plate right. So, here we need a lot of negative charges in order to ensure accumulation of positive

charges on the channel side; I must again for in the same argument the V G must be at least negative by a quantity call it mod V t p with respect to the channel in order to have the positive channel and used here.

Or in other words it is simply means that you need to have at least minimum amount of negative charge over here so that corresponding to that you have some minimum positive charge in the channel or positive holes accumulated in the channel which can form a continuous connection; continuous p type region between the source and the drain both of them p type. Once you have this continuous p type regions formed once again you have a continuous conduction in the MOSFET is on and you get a lot of current increase when you increase the V G further; when you reduce the V G further.

So, basically in this case we need to have with respect to the channel the V G should be negative we have requirement of negative voltage So, the condition is for V G should be less than V S minus mod V t. Or you can say the V G should be lower than as compared to the source by mod V TP. So, V t in general for PMOS is a negative quantity, but it is more convenient to deal with mod V TP in that case the operation or equations remain pretty similar to the NMOS. So, all we have to do is modify the equation for NMOS little bit. So, here we have V S we have V G and V D. And I can write down the equation for triode region first I D mu p cox w by L V SG minus mod V TP into V SD minus V SD square by 2.

So, here the source must be at positive terminal, because that is the terminal which is providing holes flowing from source towards the drain; so then nomenclature source and drain both in NMOS and PMOS is dependent upon the direction of the carrier flow. In case of PMOS the carriers are holes, they are supposed to flow from the higher potential p plus to the lower potential p plus. So, when the p plus region is at higher potential it is going to provide the holes; the holes are going to flow from positive terminal with a higher potential towards the terminal with lower potential because that is a electric field direction.

So, in that case the terminal with higher potential becomes source, in case of NMOS it was just the opposite. In case of NMOS if you remember the source is at a lower potential drain at a higher potential, and in that case electrons are the carrier electrons are flowing from say source to drain because drain is at higher potential electrons are

accelerated from the lower potential towards the higher potential in that case the terminal with lower potential becomes the source of the carriers in the channel. That is why in NMOS whichever terminal is at lower DC potential that becomes the source. For PMOS it is just the reverse the terminal at the higher DC potential become the source.

So, in the device structure point of view ideally there is no difference, of course you can have advance devices where you may have some asymmetry, but in general in a standard technology you do not have any structural difference between the source and the drain. It is only the DC potential at one terminal with respect to the other terminal which determines which one is going to be source and which one is going to be drain for the NMOS and PMOS respectively. So, here as we say we need the source terminal V S to be higher than the gate terminal at least by mod V TP so that the continuous channel is formed that is the condition for triode region operation.

So, if I once again talk about the channel length modulation concept similar concepts are going to come into picture. So, if we go on reducing the drain voltage. So, you have the V S suppose this is at a higher potential and you are having a V G which is lower than V S by V t. So, V G is lower than V S minus mod V TP. So, we have a channels formed and we know that at any point in the channel once again if I take a particular cross section and I call this location y. So, the effective potential drop between the channels is V G which is uniform so this whole region is V G metal contact no change in potential across this entire length. So, this is V G here we have V channel y, so effective potential V effective is just going to be V channel y minus V G and this must be greater than mod V TP in order to ensure continuous channel.

The moment continuous channel the moment we have a condition where this equation is violated for any y; that means, once again the channel is going to be reduced to 0. The whole charges that you are trying to build is going to reduced to 0. For example, what happens if we start reducing the drain terminal with respect to the source? So initially assume that the drain potential V D was close to the source potential, but now you start reducing it further and further. So, as compared to say V S which was initially equal to V DD you are reducing the V D taking it lower and lower, then of course at the drain end of the channel which I can say y equal to L; this point is y equal to L.

At the drain end of the channel I can say the gate voltage the effective voltage V effective at y equal to L is going to be the V channel which is close to the V D. So, this is just becomes V D and the gate potential is V G. So, V D minus V G. And in order for the channel to be present here this potential V D minus V G must be greater than mod V TP or in other words V D should be greater than V G plus mod V TP

So, as long as this condition is satisfying the channel will be continuous, but the moment if V D falls lower than V G plus sorry; if V D falls lower than V G plus mod V TP, then this condition is violated and once again at y equal to l we are having a condition of pinch off. At this point we have reduced the channel charge to almost 0. And under that condition we will once again have you know tapered profile charge over here has been reduced to 0.

And once again if you go on reducing the V D further and further similar condition will be applied; you will shift the channel further towards the source. And once again you have the delta L created. So, for PMOS the condition for saturation is that V D should be less than V G plus mod V TP. The moment V D goes higher than V G plus mod V TP the transistor is in triode region because you have a continuous channel form there is no pinch off, but the moment V D is lower than V G plus mod V TP then you have the condition of pinch off occurring, because you can imagine the last point over here close to the drain there you do not have any channel charge any more. So, this is the condition for pinch off and hence saturation region operation.

So, for the PMOS in order to have saturation region operation there are two conditions: V S minus V G should be greater than mod V TP and V D should be less than V G plus mod V TP. So, they are the two conditions we need to recall and we need to have at our fingertips that we can analyze circuits and find out the condition for PMOS to be in saturation region or triode region.

So, this is very important to be able to distinguish in a circuit find out the conditions for the operation of PMOS and we able to say that whether the PMOS is entering into triode region or it is there still in saturation region and so on. So, we will see that while analyzing circuits we will once again extensively make use of the saturation region condition for PMOS as well as NMOS.

So, this is about the DC characteristic of the channel length modulation and the saturation region condition for the PMOS. What do we do to the small signal model? Can we need to do we need to make any significant change to the small signal model, does it remain more or less same let us try to answer that part.

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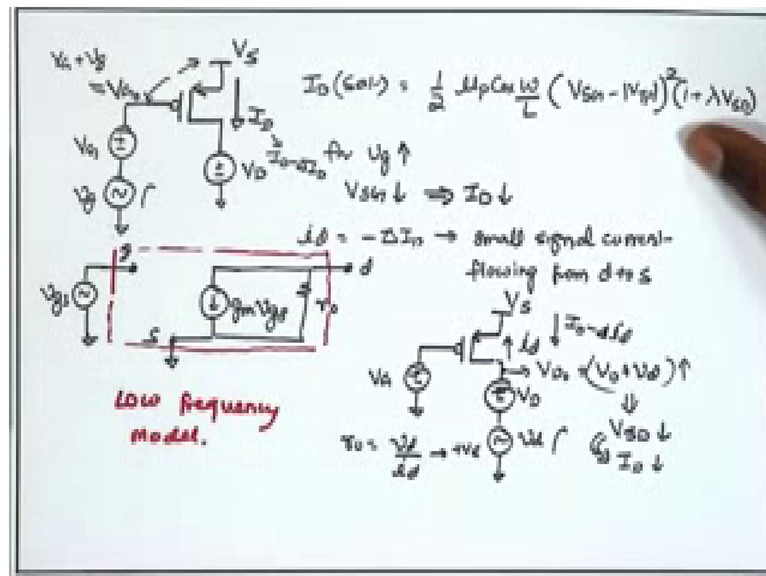

Now if I just without going into the equation if I just want to answer this I can look at my device. Suppose I have some V D established over here so this is V D I have some V S suppose for the PMOS incise one the source to be at higher potential V S suppose it is relatively large may be V DD. And I am applying some DC voltage at the gate, so suppose this is V G. On the top of that I am applying a small signal V G and with respect to this I want to find out what is going to happen to the drain current.

Now remember the drain current that we have defined using the equation for PMOS keeping in mind the equation for PMOS that we just arrived that V SG minus mod V TP this is for the triode region. For saturation region once again the same equation I D saturation region for the PMOS 1 upon 2 mu p cox w by L V SG minus mod V TP square 1 plus lambda V SD. This is the equation for the saturation region operation of the MOSFET. And now this current is the current flowing from source to drain. The positive direction of the current is from source to drain. So, I D defined by this equation is the DC current flowing from source to drain.

Now, what happens if I apply a small signal gate voltage and this going up? If the small signal is going up what are we doing to the V SG for v g going up means positive V SG is going down. Another result this implies that the DC current I D must go down because we are reducing the V SG of the MOSFET; this is the V G absolute V G is V G naught which is you know combination of V G plus small vg; so this absolute V G if I denote it as V G plus small vg. So, if I am increasing the small signal making it positive the V SG reduces id reduces that is the DC current which is reducing.

If I model my small signal current as the current flowing from drain to source what can I say about that current. So, this I D is definitely reduced to I D minus delta I D this goes to I D minus delta I D right whenever we are increasing the vg. So, if I define the small id as minus delta I D that is the current small signal current flowing from drain to source, then that quantity is positive; this is reducing the DC current is reducing, but the small id if I define it as minus id that is flowing from drain to source that is increasing. So, I can still use the positive gm and I can define the small signal current as flowing from drain to source. Increasing V G reduces DC current, but it increases the small signal current flowing from drain to source. So, that delta I D is negative I defined small id the small signal current as minus of delta I D, that is in this direction it subtract from the capital I D and hence leads to reduction in overall I D.

So, according to this that model we again had the same polarity of the gm V gs term source is at a DC potential in the AC case it becomes once again grounded, because DC potential is going to be short circuited this set to 0 for AC analysis. This point is another important point to be remembered while doing AC analysis, so this is set to 0. The small signal current the way we have defined it will flow from drain to source gm V gs; the polarity remains same gm is positive. And then we have the input signal applied at the gate V gs. This is the source is grounded and small signal is applied between gate and source, so it is also pairing between the gate and ground.

And likewise if I want to talk about ro of the PMOS: ro of the PMOS once again of course it is suppose to be as a small signal resistance of the PMOS how does they change we know of course, it has to be positive because we are talking about small signal resistance so there we should not be so much concerned about the polarity, but just to confirm that we are getting consistent polarity according to this definition.

So, in that case if I keep my gate voltage at a DC, this is fixed V G and now on the drain voltage I have an AC signal V D and on the top of that small vd. So, in presence of this small vd what do I expect should happen to the small id. So, remember again if I increase the vb make it more positive the small signal is going up V D absolute V D which is you know I call it V D naught is equal to V D plus small vd that is going up. So, this quantity is if it goes up that means, V SD is going down; V S minus V D it is going down. And therefore, these equations once again tell us that the DC current id will therefore go down; right the absolute DC current will go down.

And therefore, the way we have defined the small signal current flowing upwards from drain to source that becomes again positive, because id is reducing so the id is becoming id minus delta I D in this direction. So, if I define the small id as the change in current flowing from drain to source that becomes a positive quantity once again. So, the small signal ro which is going to be V D upon id is still going to be a positive quantity and that is appearing between drain and source. So, I can still define this as a positive quantity appearing between drain and source terminal. So, this is a drain the gate and the source terminal.

So, relatively what we need to convey from this is that the small signal model remains as it is the low frequency small signal module does not change. We can use the same small signal module for PMOS as well as NMOS. For DC condition we have to be careful, while defining the saturation region operation we just have to keep in mind the condition for saturation V S should be greater than V G by mod V TP to keep the channel on and V D should be less than V G plus mod V TP. So, that the channel is pinched off on the drain side the channel is pinched off on the drain side the moment V D becomes equal to or greater than V G plus mod V TP then the channel is no longer pinched off and you have a continuous channel and hence you are in triode region. So, this is the distinction we need to make. And is nothing to be by hearted if you have the physical operation the device in mind at any point you can quickly write down you can quickly derive that what is the required condition.

Now once we have gone through the small signal model at low frequencies; that is without considering the parasitic we have looked into the small signal model. The next point is to make the model more complete we are going to add two more features that is the high frequency parasitic capacitances that come into picture when we are trying to

operate these MOSFETs at higher frequency. And the second thing that we also need to add is the noise component arising from the physics of the MOSFET the operation of the MOSFET.

So, let us first talk about the parasitic capacitances their origin and their model: how to incorporate parasitic capacitances in the MOSFET model. So, this is the low frequency model where we have not accounted for the device parasitics. So, the name device parasitics tells us that there is something undesirable, parasite is something we do not want when it can be present from in the body it can create issues and it can create sickness it can limit our performance. So, parasite is an undesired phenomenon.

Likewise when we are talking about parasitic capacitances they are ideally not supposed to be there. We do not want them because it seems like they are going to affect our performance they are going to affect or limit the performance of the MOSFET and the circuit that we are trying to build with the help of those MOSFET. So, they are undesirable effects- that are inherently coming because of the device physical because of the device operation of this MOSFET. So, let us try to understand first of all what is the basic mechanism of those parasitic capacitances and how do we define and quantify them and include them in the small signal model.

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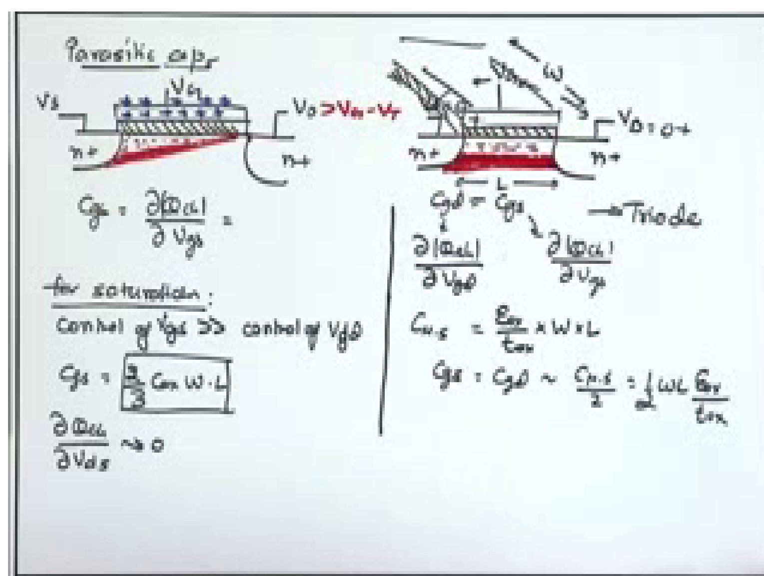

Once again look at the MOSFET structure and try to see what is going on when we are changing the different terminal voltages. So, if we assume that the MOSFET is in

saturation that is the region with which we are concerned most of the time in this course and in this discussion. So, let us assume saturation region operation. And what we have seen is that if you are in saturation region the channel charge is having a tapered characteristics, so you have a pinch off at some point if not exactly at drain maybe some point away from the drain. And this region is the channel charge; your V D is greater than V G minus V T therefore the channel is pinched off. And rest of the region is filled with negative charge you have lot of electrons here; mobile electrons which are balancing some positive charges on the gate.

So, now what happens if I keep the drain voltage constant source voltage constant increase the gate voltage a little bit? When I am increasing the gate to source voltage; that means I am putting more positive charges dumping more positive charges; so putting some more positive charges whenever I am increasing the V G to V G plus delta. And in order to balance those positive charges I will definitely need additional negative charges of the total channel charge will increase. Now, this total area the shaded region plus this dotted region will be the total charge, so because of in order to balance this additional positive charge that you putting on the gate you need this additional negative charges.

So, there is the charge storage mechanism present in the device. So, whenever you are trying to increase the gate voltage and trying to store some more positive charge it has to be balanced by equal amount of negative charge on the channel. Whenever there is a charge storage mechanism in a device we say that there is a equivalent capacitance present, because capacitance determines the charge storing capacity of the device.

So, for example, if I have to define C gs; what is the small signal capacitance coming between the gate and the source. So, I can define this as C gs d Q channel mod by d V gs. Why mod because remember the charge in the channel is negative, we are just looking at the quantity mod Q channel because that much amount of positive charge you are putting on the plate. So, capacitance is the positive quantity. So, we need to define the del by del V gs of mod Q channel that we know that if you are increasing the V gs. For PMOS for NMOS you are going to get more positive charges on the gate and as a result equal amount of negative charges on the channel. So, if you are adding delta Q positive charge on the gate you get more delta Q negative charge in the substrate.

Now here if we consider triode region operation which is easier to understand from the point of view of the device capacitances. So, in the triode region we had the source and drain voltage almost similar potential both of them close V D is; suppose V S is 0 V D is just 0 plus little bit positive under that condition the channel charge was almost uniform. So, there was no tapering, so channel charge was almost uniform negative charge all over.

And then under this condition if I change the gate voltage V G make it positive or negative we are expecting this charge to expand uniformly all throughout. So, it will expand uniformly it will increase uniformly all throughout. Therefore, what we can say is if I am changing the gate voltage that is changing the effective V gs it is also changing the effective vds and V gs as well as vds are having equal impact on the channel charge, because it is almost symmetric. For instance if I look at it in other way gate and drain suppose they are constant and I change the V S I make it more negative; that means, there will be more channel charge created on the source side. So, it will be you know kind of getting tapered on the source side.

Likewise if I keep the source and gate constant make drain more negative by definition it no longer remains as drain because if the drain is more negative with respect to source then you have this terminal being the source. But just for the sake of understanding if we make the drain more negative with respect to fixed gate and source you get more negative charge is accumulated towards this end. And they are being balance by more positive charges on the gate.

So, in the triode region operation cgd as well as cgs are almost similar in magnitude. This can be denoted as del qch del vgd and another side cgs can be represented as del Q channel del V gs. But in the triode in the saturation region operation the channel has been pinched off on the drain side. So, drain is losing control on the channel charge it having very weak control only because the channel length modulation if you increase the drain voltage by large amount it will shift little bit further.

So, it does have some control, but very small amount. So, for saturation region we say that the control of gate to source voltage on channel charge is much stronger. So, for saturation this is for the triode. For saturation region operation control of V gs much

larger than control of vd or vgd. And we can all together ignore the effect of the change in drain voltage or vgd on the channel charge.

So, in case of triode region this was just act like a parallel plate capacitor. You have metal, you have the channel charge which is negative. So, this is acting like the positive plate the silicon is acting like the negative plate, and if they isolated by this thin oxide of thickness tox. Per unit area the effective capacitance is just epsilon ox upon tox. Total capacitance between the gate and the silicon is going to be obtained by multiplying this with the overall area. So, L is the channel length and w is the width of the MOSFET in the direction perpendicular to the gate.

So, this is just forming a parallel plate capacitance and the total gate area w times L's multiplied by capacitance per unit area that is epsilon ox upon tox gives me the effective C metal silicon. And since in the triode region gate and source are having equivalent or similar degree of control on the channel charge we say that cgs is equal to cgd approximately equal to cms by half. So, each of them become one upon two wl epsilon ox upon tox approximately. This is an approximated relationship this is true in triode region.

But in the saturation region the control of the source is much stronger on the channel control of drain is much weaker. So, effectively cgs takes a larger role and we can derive the exact formulation by integrating the effect of increasing gate to source voltage on total charge and arrive at the accurate value. But approximated analysis can give us cgs approximately equal to 2 by 3 times cox time w times L. So, more than half of the value or more than half of the overall capacitances between the gate and the bulk so two by third of w l cox is dictated by the cgs.

And the drain voltage is not having much control on the total channel charge is a very big dependence in the triode region. So, the channel charge or the capacitance resulting from channel charge is almost reduced to 0. So, we say d Q ch del vds is approximately reduced to 0, because the drain is not having much contact much control on the channel charge. So, this term is reduced to 0. So, this is the first component cgs which results from the change of channel charge because of the change in V gs.

There is another component of capacitance between the gate source gate drain that all arises from overlap of the gate with the drain and source region. So, these basically talk about the overlap capacitor.

Thanks a lot.