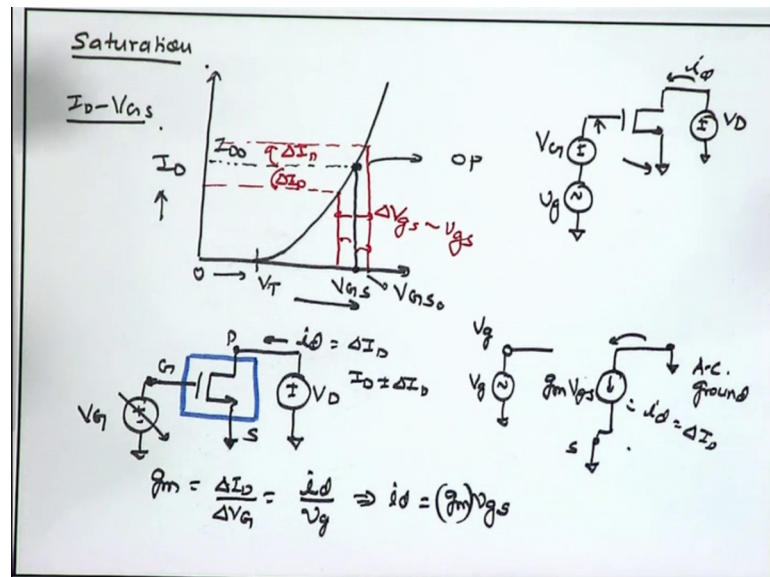


Analog Circuits and Systems through SPICE Simulation
Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture – 02
Basic Analog Design Part – I
Contd.

Hello, and welcome us again to the first part of this course; I am Mrigank. In the introduction session I give you brief overview hint what we have going to cover in the first few lectures on analogue design.

(Refer Slide Time: 00:42)



So now, let me talk about the large signal and the small signal characteristics of the MOSFET where that we are going to use in saturation region to arrive at the MOSFET characteristics. So, looking at the squared law equation from the x axis I have V_{GS} on the y axis some plotting the I_D . So, how do I obtain this plot? I can apply DC voltage at the gate of the MOSFET call it V_G . I can apply a drain voltage source say V_D I am not talking about, how to apply that drain volt your, how to generate that gate voltage assume that you have these sources available somehow on the chip or in the test board you are able to generate these required DC voltage is V_G and V_D and connected to the drain and the gate of the MOSFET.

Source is connected to the reference point, so source is grounded. And now I gradually sweep my gate voltage starting from the minimum value close to 0 going on increasing the gate voltage till I reach a V_T the current will be very small it will not be 0 minded, because we are having subthreshold operation and there we know that there is an exponential dependency of current on the voltage.

So, in this region of course, current is very small. For practical purposes if we are operating the device in saturation region we can ignore the current in this region and call it that the MOSFET is off in this region you do not have significant current flow. Once we hit V_G equal to V_T beyond that point v observes steep increasing current following the square law dependency. And by sweeping the V_G from minimum all the way to a large value we can obtain this plot. Now how does this link to the small signal parameter of the MOSFET?

So, when we talk about small signal parameter we are talking about processing very (Refer Time: 02:46) very weak signals with the help of this MOSFETs exploiting the device characteristics; exploiting this characteristic curves of the MOSFET.

So, first thing is we need to have the DC operating point; desired DC operating point of these devices no more. What does that mean? That means that on this I_D vs V_{GS} curve we are going to have a desired V_G we are going to have a particular choice of V_{GS} call it $V_{GS, \text{naught}}$, corresponding to which we are going to get a particular I_D naught. This is the defining my DC bias point of the circuit. I have chosen a certain $V_{GS, \text{naught}}$ and the I_D, naught and at this point I am going to operate my MOSFET. So, this is the operating point of the MOSFET.

Now, on the top of this operating point which is determined by the DC voltage I can apply some small signal which is input to my circuit for amplification of processing using the physical characteristics from this MOSFET. So, I can apply a signal ΔV . I can increase my gate voltage by small amount or decrease by a small amount which is my small signal I can call it ΔV or rather ΔV_{GS} . Or in terms of small signal we can just write it as small v_{gs} that is a small signal change that we are imposing on the top of this circuit. So, basically I am applying a small signal in series with this gate terminal and then trying to observe what is happening to the current characteristics.

So, this curves tells us that if you are increasing the gate voltage by little bit my green current will go up, reduces the green current goes down. So, I get a commensurate delta I_D on both side; increase and decrease by delta I_D . And we can denote this MOSFET as a three port device. So, we can treat this as a black box. So, you have these three terminals that are available to you: the gate, the drain, and the source. We are giving a source at the reference point that is grounded. We are applying some signal between the gate and source that becomes our applied signal V_G . On the top of this constant V_G we are applying some small v_g going up and down. And corresponding to that we expect the current in the output branch I_D , we expect some small change in the current in the I_D branch that is your delta I_D .

So, the net current of course, is going to be I_D plus minus delta I_D . So, when I am applying V_G plus minus delta V_G I get a corresponding I_D plus minus delta I_D flowing into the drain current. So, by changing the voltage across the first two terminals I am getting a change in current flowing across the third terminal. And therefore, there is a transconductance operation going on. Applying a small signal voltage between gate and source we change the current flowing between the third terminal and the device.

So, we can define this three port model in terms of transconductance. So, we can draw the three ports: we have the gate, we can just use the small signal that is applied on the top this DC. So, we can forget about the DC V_G we can forget about V_D and look at only this small quantity small v_g and the resulting small i_d that is resulting in our small signal operation.

So, in that case we are just going to apply some small v_g over here setting the DC to 0. And we are going to look into the drain terminal; once again in this particular example if I only considered the small signal the V_D is constant. So, the drain voltage is a DC it has not having any small signal. So, from the point of view small signal I said it to 0. So, I said this is an AC ground because in the corresponding circuit over here we have set the drain to a DC voltage or V_D .

And as a result of the applied V_G effectively the V_{GS} because the source terminal is also grounded we are getting a transconductance term, we are getting a small change in the current flowing from drain to source and we can denote this as a constant term g_m times the small signal v_{gs} and this small change in current which is your small i_d or

ΔI_D can be obtained from this transfer characteristics from this curve $I_D - V_{GS}$ curve of the MOSFET.

So, if you look at this curve and say that is your changing the V_G by ΔV_G what is the change in ΔI_D obtain. So, that can be written as V_G times the slope of this curve. So, g_m can be defined as ΔI_D upon ΔV_G or in terms of small signal small signal i_d by small signal v_g . So, what is the small change in the drain current we will obtained when we are changing the gate voltage by small amount; that is the transconductance term. And the trans comes from the point that we are applying the signal between the first two-ports and we are getting a change in current through the other port.

So, if you have a conductance or a resistance you apply voltage across the two terminals of the resistance and you get change in current across these thing two terminals of the device. But here are applying a small change in voltage across the first two terminals of the device and the current through the other terminal is changing. So, is the trans term community picture, and the slope of this curve at a particular DC point that we have chosen for our circuit operation defines the transconductance of our MOSFET. And therefore, the ΔI_D or the small signal i_d can be conveniently written as g_m times v_g . And remember that in this condition we have taken the source as the reference point, so it is always with respect to the source $g_m v_g$ becomes the transconductance.

Now in order to arrive at the expression for g_m and look at how it depends upon the device characteristic that we have in our hand we can try to derive the expression and related to the device parameters.

(Refer Slide Time: 09:54)

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \cdot 2 (V_{GS} - V_T) (1 + \lambda V_{DS})$$

① → $\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \times 2$
 $\underbrace{\hspace{10em}}_{I_D} \quad \underbrace{(V_{GS} - V_T)}_{V_{ov}} \rightarrow V_{ov}$
 $= \frac{2 I_D}{V_{ov}} \quad \text{--- (a)}$

② → $\frac{\sqrt{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2} \cdot \frac{1}{2}}{\sqrt{2} \times \sqrt{\mu_n C_{ox} \frac{W}{L}}}$
 $\underbrace{\hspace{10em}}_{I_D} \quad \underbrace{\hspace{10em}}_{\sqrt{2} \times \sqrt{\mu_n C_{ox} \frac{W}{L}}}$
 $= \frac{\sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}}{\sqrt{2} \times \sqrt{\mu_n C_{ox} \frac{W}{L}}} \quad \text{--- (b)}$

So, here once again looking at the saturation region characteristics because that is what we have going to use most of the time. We can differentiate this curve at a desired DC point V_{GS} and V_{DS} . So, we can obtain the slope of I_D V_{GS} curve at the particular point has the noted in the last slide and they can write this down as 1 upon $2 \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$ in $1 + \lambda V_{DS}$.

And now I can manipulate this equation that I am getting in different ways to obtain more compact equation for g_m and figure out this dependency on the device parameters. So, first case I can multiply this equation and divide by $V_{GS} - V_T$ square. So, I am multiply the numerator as well as denominator by $V_{GS} - V_T$. Also I can multiply and divide by 2 .

So, if I look at the first term. So, within this blue box the term that I am having is same as the DC bias current that we started with that is the I_D . And the second term $V_{GS} - V_T$ is call or is generally termed as the V_{ov} the overdrive voltage. You need minimum V_T with respect to the source at the gate voltage two turn the MOSFET on. The axes voltage $V_{GS} - V_T$ is termed as the overdrive voltage and then this we can express this expression as $2 I_D$ upon V_{ov} . This is one expression for g_m .

Likewise I can modified in a different way, I can use this equation, I can separate out I can steal the route of $\mu_n C_{ox} \frac{W}{L}$ by L take $V_{GS} - V_T$ inside make it a square and we can to some extent. If we can afford to ignore say λ , we can suppose the

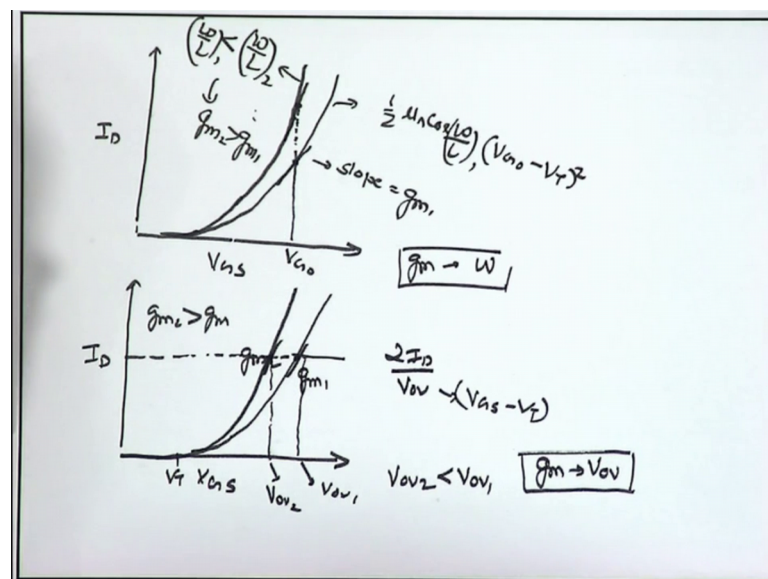
channel in more relation is we can ignore lambda then we can drop the second term over here and just use the first term. Multiply and divide by root 2 and also we are left with again another square root term $\mu_n C_{ox} W$ by L .

So, once again the term under the first square root is our I_D . So, what we get over here is $\sqrt{2 I_D \mu_n C_{ox} W}$ by L of the MOSFET. So, this is another expression of the g_m which can be handy, while working on designs, when figuring out what should be the g_m what should be the gain. So, this is another expression that we should have at our finger tips.

So, it tells us couple of things, it tells us that there is a dependency on I_D if you are increasing I_D for a given V overdrive your g_m is going to increase or vice versa for a particular I_D if you are reducing the V overdrive the g_m is going to increase. Likewise it also tells us that for a given I_D if you are changing the W by L increasing the W by L the g_m is going to increase.

Once again as I suggested that it is not good enough to just remember this formula, it is also important that we link this expression to the actual device characteristics. But how this g_m change reduction or increases come in when I am changing my I_D or V overdrive. So, it is also important to keep that into mind. So, that is look at the two dependency.

(Refer Slide Time: 14:10)



So, if I revisit my I_D vs V_{GS} curve from which we have obtained the definition of g_m . So, if I am at a particular V_{GS} , so call it V_{GS} naught sources grounded. So, as we said the slope of this curve at this particular point is going to give me the g_m . This slope of this curve is the g_m . So, as per this equation if I am say increasing the W by L , so, this curve is for 1 upon $2 \mu_n C_{ox} W$ by L 1 and times V_{GS} naught minus V_T square. And if I choose to increase the W by L ; as I said W by L is the design parameter available to the IC designer I can tweak my W by L I can change it increase or decrease that to needs certain specs of the circuit.

So, how does this curve change? Definitely if I double my W by L for particular V_{GS} naught my curve is going to go up right, V_T remains same but the curve goes up. So, at the same value of V_{GS} naught we are expecting that this W by L 2 which is greater than W by L 1 we are going to get a larger slope. And hence a larger g_m : g_m 2 is greater than g_m 1 which was at this point. So, keeping in mind the physical characteristics of the curve becomes are important; we should know why the change in the g_m is happening.

Likewise this is a dependency on W . Likewise, we can for the same you know conditions we can also see what is the dependency on the overdrive voltage and conclude that whatever expression we are obtaining is making sense. Once again drawing the I_D vs V_{GS} characteristics for a particular V_T ; my W by L is fixed, my I_D is fixed the second the first equation that I have for g_m is I_D by V overdrive.

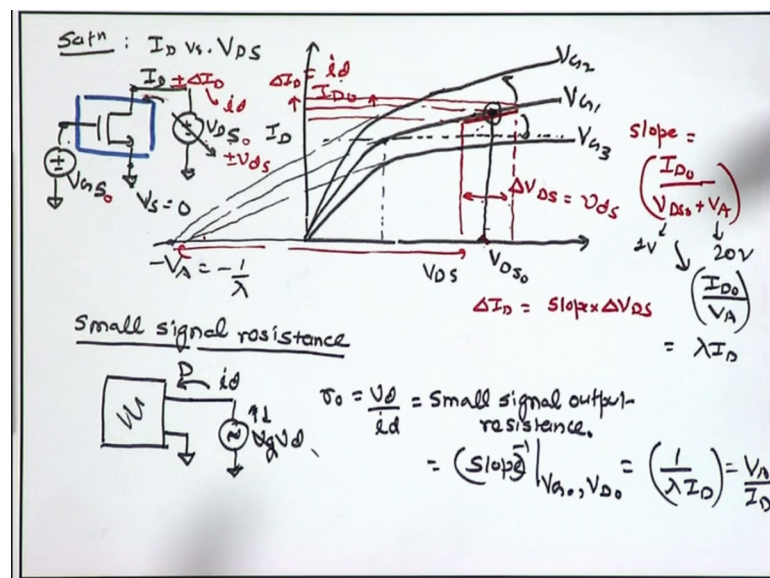
So, this case my I_D level is being fixed so I am at a particular I_D . So, my horizontal line is fixed. And then if I am reducing my V overdrive the what that mean this is once again V_{GS} minus v_T ; that means, I am is reducing the V_{GS} . Once again for a particular characteristics if I have to obtain the same value of I_D for reduce V_{GS} the curve will be the point will be somewhere over here. And this will be again a part of different I_D vs V_{GS} curve. So, basically we are changing the V_{GS} .

Once again, we can clearly see that g_m 2 is going to be greater than g_m 1 . And clearly the V overdrive 2 is smaller than V overdrive 1 . and this gives us the dependency of g_m on V overdrive. So, it is important that we are able to link the small signal parameters that we are arriving at with the actual characteristics of the device. Then we can better appreciate what is the dependency of gain on W , what is going to happen if I change my

bias current, what is going to happen if I have certain parameters in our hand like V_T and so on.

So, this is about the small signal transconductance parameters. Let us now talk about another very important small signal parameters that is r_o of the MOSFET, which is very crucial for analog design not so much maybe for the digital part. So, once again if I talk about the saturation region operation and look at the I_D V_{DS} characteristics of the MOSFET.

(Refer Slide Time: 18:20)



So, in order to obtain this curve saturation region operation for I_D versus V_{DS} curve of the MOSFET. So, first of all the question is what is the curve we expect when we have a MOSFET we are fixing the gate voltage to a DC call it capital V_G and we are sweeping the drain voltage this time; remember reference point is source voltage, here in all cases we are putting the source as a reference point. So, I can always write V_{GS} V_{DS} in this case v_s is equal to 0. And this case once again we are going to sweep the drain voltage starting from 0 to some maximum value dictated by the particular choice of the gate to source voltage.

So, what is the curve we expect the well known I_D V_{DS} characteristics? So, we have already seen what happens in the triode region. So, when we start with a very small v_{gs} we said that the MOSFET is in triode region and in that case the equation that is governed is the linear dependency on V_{GS} and V_{DS} . And we will see what is the

phenomena that leads to saturation. In ideally in saturation; saturation term means that the current through saturate it should become almost constant and the MOSFET should behave like a ideal current source becomes completely constant, it is not should not have any effect because of changing V_{DS} ones that interns into saturation region.

But the actual MOSFET characteristic tells us something else you do have a finite slope of the MOSFET which means that we do have some finite output impedance looking into the drain. So, let us see what all these term means the small signal output impedance or the slope of this curve the concept of channel length modulation and the requirement of saturation region operation.

So, here this is for a particular V_{G1} . So, what I in do? As I can fixed as V_G as to a V_{G1} and then sweep my drain to source voltage from minimum 0 going all the way to higher value and at each point I can measure what is the current I_D flowing through this MOSFET. That is how I obtain this curve. I can change my V_G I can go for a larger V_G V_{G2} an obtain another curve. For a larger V_G of course, the saturation region as the triode region expression will tell me that a particular V_D in the current is going to be higher if I am having a large V_G . And likewise for a smaller V_D I can have curve which is lower. And graphically it is known that if you are extrapolating these curves they meet at a particular point on the x axis negative x axis at minus V_A which can also be termed as minus 1 upon λ which is the constant parameter V_A as well as λ I am assuming is a positive constant positive parameter of the device.

And then, if I am talking about a particular V_{DS} V_{DS} naught, I am looking at a particular V_G naught. So, I have once again fixing the DC operating point of the device, I am choosing the bias condition the device, I am choosing a certain V_{G1} I am on the top of that V_{G1} I am choosing a certain V_{DS} naught. So that fixes my DC operating point it tells me that I am at a particular DC bias current I_D naught. This is the operating point of the device. And at this operating point I can figure out what is the slope of this curve at this operating point, because that is going to tell me something about the behaviour of the output port of this MOSFET.

It tells me that if I am keeping my V_G constant that is I am sticking to the V_{G1} curve and changing the V_{DS} little bit across the V_{DS} naught point. So, V_{DS} I have kept it to V_{DS} naught and then I am changing it little bit on both sides; ΔV_{DS} you can call it

small signal V_{DS} on both sides plus minus delta. So, I am increasing and decreasing V_{DS} by some mechanism maybe just by tuning this knob over here artificially. So, what is the corresponding change in the current that I am going to get? So, this going to lead to ΔI_D or you can call it the small signal i_d . So, what is that small signal ΔI_D or the small i_d resulting from change in this V_{DS} to plus minus small V_{DS}

How to I going to remind that? So, I can look at this curve once again I can see for a particular V_{DS} the small V_{DS} what is the change in ΔI_D that I am going to get. This is the small change in I_D that I expect. Once again the small change in I_D can be expressed as the trans or the slope of this curve ΔI_D and I can write it as slope of this curve times the ΔV_{DS} . So, all we need is to because what is the slope at that particular DC point. If I know the slope I know; what is the small signal behaviour of this device looking at the output port. So, I can say that if I have a DC condition V_{DS} from the top of that I am applying a small signal V_{DS} what is the small change in the current I_D so that I can obtain by the slope; slope multiplied by the ΔV_D gives me the ΔI_D .

So, I can see some questions coming in, but right now we have question regarding g_m , what is the significance of g_m . So, once we go towards the application of this device in to circuits we will be able to appreciate what is the significance of g_m . So right now we have just looked at the transconductance operation of the device where you are applying the input signal at the gate and getting some change in the drain. So, it is the transistor operation rights you are applying signal that has certain port, you are getting current change at the different port. So, that is the main transistor operation that we are interested in. So, we look into it when we go towards application with revises into circuits.

Now here once again if I talk about the small signal operation: so starting point was we fixed we choose a certain value of V_{DS} ; we choose a certain value of V_G which landed us on this circle on this point with us fix V_{DS} naught and a fixed V_{GS} naught. And then on the top of that we are changing the V_{DS} . So, looking at this particular simple circuit we are fixing this V_{GS} to V_{GS} naught, we are fixing this V_{DS} to V_{DS} naught and then on the top of that we are changing the V_{DS} by little bit by small amount if small signal and then noticing the small change in I_D that is the ΔI_D (Refer Time: 25:33) MOSFET. And that is easily obtain for this curve.

So, I can write down what is the slope of this curve if I look at this point, the slope can be identified as the y length, the length in the y direction divided by the length in the x direction. Length in the y direction the height of this point is just $I_{D, \text{naught}}$. So, I can write the slope as $I_{D, \text{naught}}$ because this is just $I_{D, \text{naught}}$ starting from 0 this point is $I_{D, \text{naught}}$, divided by the length in the x direction which is $V_{DS, \text{naught}}$ plus V_A in the opposite direction. So, this is the slope.

Approximately in general the V_A will be much larger than $V_{DS, \text{naught}}$. If I am talking about 180 nanometer technology the supply voltage that we have is 1.8 volt V_A can be 10 or 20 volt almost an order of magnitude higher than $V_{DS, \text{naught}}$. So for 180 nanometer I can say V_A is going to be around 20 volt or higher $V_{DS, \text{naught}}$ at the max 1 volt of that order. So, we can conveniently ignore this $V_{DS, \text{naught}}$ term in presence of V_A and we can just say that the slope is approximately equal to just $I_{D, \text{naught}}$ upon V_A .

Generally, this is the term this is the expression that is used for the slope. Although in the graph that I have drawn it is not very prominently clear that $V_{DS, \text{naught}}$ is much smaller than this V_A , but generally that is the case V_A and $V_{DS, \text{naught}}$ of desired operating point. So, generally the slope can be just defined as $I_{D, \text{naught}}$ upon V_A . And that can also be written as λI_D . So, λ is one upon V_A as mentioned over here; so we having the slope given by λ times I_D .

Now if I want to define a quantity that is the small signal resistance seen into the drain terminal; looking into the drain terminal what is a small signal resistor. So, what do we mean by looking into the drain terminal? Remember once again treating this MOSFET as the three port device, a black box where you have only three terminals visible to you: the gate the source and the drain. You are treating the source as the reference point grounded it. The gate voltage is fixed at a particular $V_{GS, \text{naught}}$ and then on the third terminal V_{DS} which we can take it as the output terminal where we are trying to test the device changing the DC voltage over here $V_{DS, \text{naught}}$ to a small value plus minus ΔV_{DS} what is the change in the current.

So, that gives us the quantity small signal resistance. So, for any two-port circuit any two-port network or a model reference point maybe ground. You have one port available,

you want to see irrespective of whatever is there in this box, you want to see what is the impedance looking into this terminal of the box, why I am calling this drain? This is the box and I am calling this is the drain terminal which is available to me other ports are fixed at some point I do not care; the gate voltage is think that the some point I do not care. I am just looking at the available port the drain and trying to see what is the impedance, what is the small change in current that I am going to get flowing into this source if I change my voltaire this node by small v_g .

So, once again it is very important to distinguish this small v_g from capital V_G , so this capital V_D sorry v_d . So, this capital V_{DS} providing me the DC point just like on this x axis we have the DC point corresponding to that we have a DC current $I_{D, \text{naught}}$. And if you are talking about the drain terminal here we are trying to change this drain voltage little bit up and down by a amount V_D , and what we are trying to do is we are trying to measure the small change in current flowing into the drain terminal. So, we are only looking at the small signal I am forgetting about the DC condition, I am forgetting about this $I_{D, \text{naught}}$ I am just concerned about this small i_d which is flowing into the drain terminal; the small change in current.

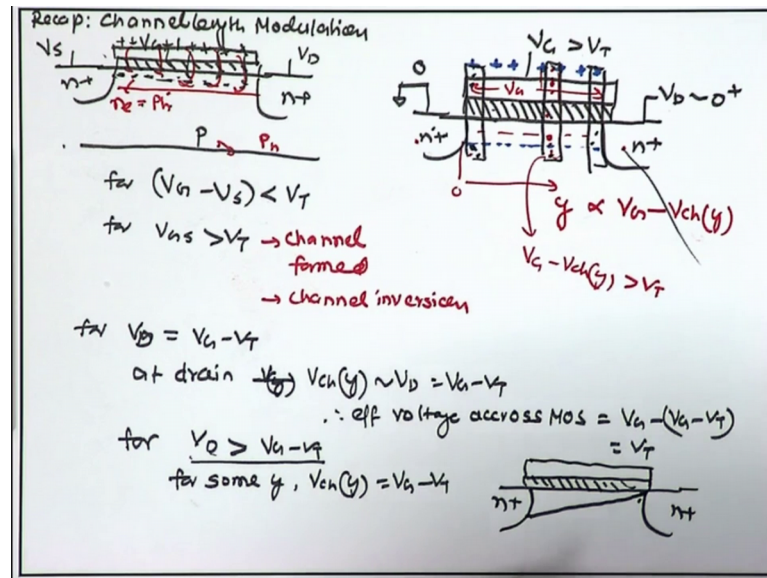
So, this change in current becomes my small signal; I forget about the DC value bias point. So, what is the change in current the small i_d which is going to result from changing in the drain voltage by a small amount of v_d ? So, this v_d upon i_d is going to give me the small signal output resistance; this is going to give me the small signal output resistance. Once again this can be obtained as the inverse of this slope. So, what we obtain from his slope was i_d upon v_d . So, if I have to talk about v_d upon i_d it is just the slope inverse at the particular $V_{G, \text{naught}}$ and a particular $V_{D, \text{naught}}$.

So, once again we have to define the slope but at a particular DC point. So, first of all we have to identify what is the DC point at which the device is operating. So, first is identify this capital $V_{DS, \text{naught}}$ capital $V_{G, \text{naught}}$ capital $I_{D, \text{naught}}$ so that gives me the operating point. And on that operating point at that point what is my slope, inverse of that slope is giving me the r_o . And therefore, this becomes equal to one upon $\lambda I_{D, \text{naught}}$ or V_A upon $I_{D, \text{naught}}$. So, this is the bias point voltage DC current.

Now before we try combine these two parameters g_m and r_o to arrive at the combined small signal parameter of the MOSFET, let us briefly talk about the channel and

modulation. Although many of you might be already aware of it, quite thorough gated, but once again people working racial domain they hardly worry about lambda, hardly worry about r_o . So, in those cases it is good to have a brief recap of this might underlying mechanism behind r_o or the channel length modulation and the resulting slope that is revisit; that very quickly.

(Refer Slide Time: 32:04)



So, if I look at the MOSFET structure recap of channel length modulation; so considering the NMOS once again. So, what we have seen is that if you are having a gate voltage V_G beyond a certain voltage called V_T that is the threshold voltage we have the MOSFET getting on. As long as the V_G is lower than the threshold voltage for V_G minus V_S ; V_S is a reference point we are assuming it to be grounded. So, for a V_G less than V_T there is hardly any current there is hardly any conduction, so practical purposes we can ignore it we do have some threshold current that is always bearing mind that we do have some threshold current, but if we are operating with larger bias current with an ignore that.

So, beyond below V_G less than V_T we do not have much conduction in the channel. So, here we have a P type substrate and lot of holes over here, but we do not have electron significant amount of electrons forming the channel. Once we go beyond V_T for V_G greater than V_T we induce enough number of electrons in the channel. So, when we are increasing the gate voltage essentially what are we doing, we are depositing

more and more positive charges on the metal gate. Making a metal terminal positive means you are depositing more and more positive charge. And these positive charge will attract more and more negative charge at this point; more is the positive charge we will require more amount of negative charges over here to balance the electric field created by the positive charging.

So, the moment you are trying to deposit positive charges on the gate terminal trying to make it more positive, we need negative charges on the other side of this oxide to balance the electric field or terminate the electric field. So, they are these positive charges they produce an electric field and they attract the negative charges. So, that they accumulate over here and from the channel. That is a basic mechanism for forming an n type channels. So, beyond the certain point when your V_{GS} is sufficiently larger than V_T you have enough number of electrons accumulated over here so that the substrate region has become almost n type as the bulky p type.

So, we say that if the electron concentration in the bulk sorry the whole concentration in the bulk is P ; P whole the electron concentration at V_G equal to V_T almost we can call it n electron is equal to P whole. That is called channel inversion that happens only when you are channel is completely inverted beyond V_G equal to V_T So, that is of course, we can go to more device level operations, and we can drive the exact physical phenomena involved in that, we can derive the physical meaning of V_T . But in this limited session of course they cannot do that, we can point of the reference material so that those of who you are interest in going to the device details and brush up the device fundamentals can do that. So, V_T itself is the very important parameter that has many important dependencies on other parameters. So, it is important that we aware of V_T also the origin of V_T also.

So, I would definitely recommend getting into the basic device concepts and be aware of this concept of channel inversion that how the p types of state is getting inverted, how you are putting more and more positive charges on the gate and that is attracting more and more electrons on the surface and creating an n type channel connecting the 2 n plus regions. So, once this happens we say that the channel has been formed. You have enough number of negative charges accumulated over here and there density is equal to the whole density in the bulk. So, that is the channel inversion; channel has been inverted.

Now, the channel in version depends upon the relative difference of the voltage between the gate and the silicon. The gate is metal in between you have oxide and then you have the channel which is once again silicon. So, metal oxide and silicon it is forming a capacitor. So, in order to do a form of channel any section of the MOSFET; if I redraw this little bit more detail. If I have to talk about any particular locations suppose the sources that are ground voltage and this is oxide we are talking about the gate voltage V_G and the drain voltage is small suppose it is close to the 0 it has to be positive right little bit positive voltage is needed to ensure any current flow. If you have both source and drain we know that there is no current flow you need a potential drop you have current flow. So, assume that it is close to 0 little bit 0 plus. So, you have some current flow provide the channel is created.

Now, V_G is greater than V_T so under that condition as I said you are going to have a channel of electrons created you have deposited, so many positive charges over here to balance those you are having lot of negative charges over here. So, you are having the channel created. At any point in the channel the effective density of these electrons at a particular location y ; suppose I call this my reference point 0 and at a particular location y in the channel I am looking at the electron density at this point that is going to depend bit on the difference between the gate potential and the channel potential.

So, this is going to depend upon the difference between the V_G at this point and the channel potential $V_{channel}$ at y . $V_{channel}$ means the potential at the y . V_G is all port constant right; this is the metal gate metal does not have significant potential drop. So, all throughout V_G is constant right. So, this is entire region V_G , but in the channel you have a relatively higher resistance. So, we have a potential drop across the channel starting from the source going all the way to drain.

So, the potential is dropping across the channel. This is the higher resistance material silicon. And therefore V_y ; $V_{channel}$ y is not constant, $V_{channel}$ is dropping from a positive potential on V_D side going down all the way to 0 at the drain side. So, $V_{channel}$ y is a variable. As a result at a particular slice if I take out the slice of the MOSFET and try to see; what is the effective potential between this capacitor of metal oxide and silicon at this point? Let us going to be V_G minus $V_{channel}$ y that is a we have written over here.

And in order to invert the channel $V_{channel}$ this effective voltage must be greater than V_T . So, in order to have the channel at the source side we said that V_G should be greater than V_T because on the source side the effective potential between the gate and the channel was just V_G this is close to 0 because this is adjacent to the source which is having 0 potential. So, at this point we just have the overall potential between the gate and channel as V_G , but at a particular location V_y it is reduced to V_G minus $V_{channel}$. And therefore, in order to have the channel continuous at the location V_y it must have V_G minus $V_{channel}$ greater than V_T .

Now if you go on increasing V_D and make it more and more positive and recheck condition such that V_D has reached say V_G minus V_T . So, under that condition just adjacent to the channel; just adjacent to the drain terminal if I look at the $V_{channel}$ at drain the V_y or you know $V_{channel}$ is approximately equal to V_D which is V_G minus V_T . And therefore, effective voltage drop across MOS that is the metal oxide semiconductor it is reduced to just V_T , because this is going to V_G minus V_G minus V_T .

If we go beyond that if V_D increases beyond this then definitely the effective voltage is reduced below V_T and once again we are going to lose the channel at that point. So, we say that under that condition the channel has been pinched off, you do not have an effective electron density on the drain site. So, at this time the channel has been pinched off the electron density over here has been reduced to 0, but definitely on the source side you still have the strong channel created.

So, this is basically now creating a depletion region. And what happens if we go on increasing the drain voltage further? So, if my V_D is going beyond V_G minus V_T . So, for some point in the channels or some y in the channel we will have $V_{channel}$ equal to V_G minus V_T . So, at some you know location in the channel we will have a condition where, $V_{channel}$ is equal to V_G minus V_T . If I just continue from here. So, if I am going for larger and larger V_D .

(Refer Slide Time: 41:53)

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$\frac{1}{2} \mu_n C_{ox} \frac{W}{L(1 - \frac{\Delta L}{L})} (V_{GS} - V_T)^2$$

\downarrow
1 - γ for $\Delta L \ll L$

$$\rightarrow \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \frac{\Delta L}{L})$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

So, we expect that at some point in the channel definitely down there we are going to have $V_{channel y}$ equal to V_G minus V_T . And once again at this point we are reaching a condition where V_G minus $V_{channel y}$ has been reduced to V_T . So, the pinch-off point moves further. So, this entire region is depleted of electrons do not have a net electron in this region we say that this is depleted.

And therefore, the effective we called this ΔL , effective channel length across which the length the channel is formed is now reduced to L minus ΔL . Now it can be shown if it try to derive this equation from the very basics all we need to do in order to capture this effect of reducing L is to modify the channel length the effective channel length appearing in the MOSFET to L minus ΔL .

Because, what happens is that you are having a depletion region beyond this point. So, in this region you are having lot of positive charges. So, lot of negative fixed charges over here in the P type region and you have a lot of negative charges in the N plus region. So, here in this depletion region just like in the depletion region of the diode here we have a depletion region and we are going to have a strong electric field in this region. So whatever electrons are able to reach to this point there easily subduing.

So, in order to write down the overall equations for the current I can just write; I can just modify my equations and replace the L by ineffective channel length as if my channel length has been reduce to L minus ΔL and imagine that my channel ends over here.

And then whatever current I get that same kind of going to exit out of this channel; that is it is not going to change because current cannot change. So, my modified I_D becomes $\frac{1}{2} \mu_n C_{ox} W (L - \Delta L) (V_{GS} - V_T)^2$. So, all I have done is the original current equation as modified to $L - \Delta L$, I am assuming the ΔL to be relatively small here as exaggerated it is looking largest, but in general if I assume that the ΔL is small as compared to the channel length I can take out a lot of (Refer Time: 44:24) $\frac{1 - \Delta L/L}{L} (V_{GS} - V_T)^2$. And this can be expressed as $1 - x$ where x is very small assuming x is much much smaller than 1 for ΔL much much smaller than L I can express this equation as $\frac{1 - \mu_n C_{ox} W (L - \Delta L) (V_{GS} - V_T)^2}{L} (1 + \frac{\Delta L}{L})$.

And must again this $\Delta L/L$ this is a fractional change in the current can be written as λV_{DS} that is. Once again coming from the device characteristics proportional to V_{DS} we are increasing the V_{DS} making the drain voltage more and more positive the ΔL increases the check pinch of point shift further another result the current is supposed to increase slightly. And the proportionality constant is once again coming from that slope I_D/V_{DS} characteristics.

For the smaller is the λ smaller will be the change and in that you can ignore this ΔL by, but if the λ is smaller especially we have going for scale technologies λ degrades another result it becomes more and more significant. The slope in the saturation it becomes more and more prominent, we cannot treat in ideal current source. This is the basic origin behind channel modulation, I can write down the overall current equation as $C_{ox} W (L - \Delta L) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$.

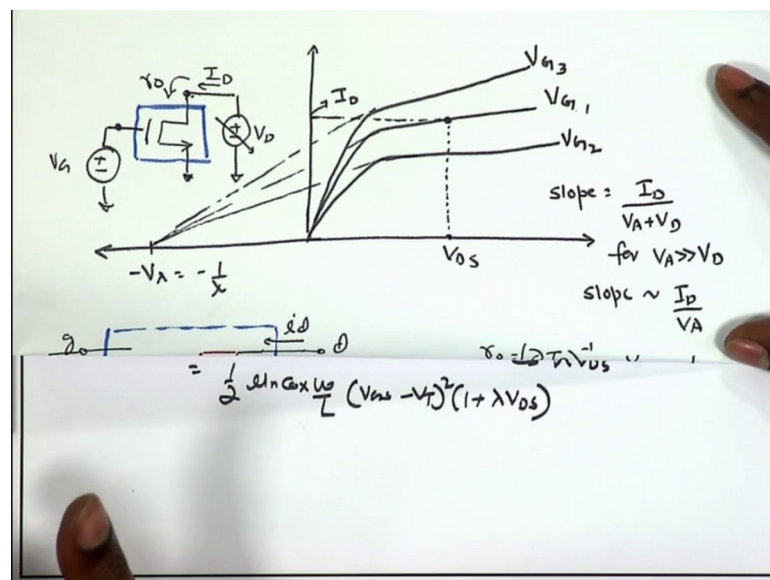
Once again remember that here we have taken such an approximations there is an deriving it from the basics and deriving at the final equation because of lack of time, we have just said that the key point remember is your effective channel length is getting reduced. The length over which you are calculating the current flow it is just L to $L - \Delta L$. And we are assuming that the drain is shifted to this point, because after this there is no significant electron concentration.

So, whatever mechanism be used to arrive at the original current equation we just change the limit of L to $L - \Delta L$. And whatever current reaches here because of the strong electric field in this region it get sug in towards the drain which is positive

potential which is V_D get an significantly greater than V_G minus V_T you have a positive potential over here strong electric field in this direction which sucks in all electron that reaches here. That is the basic mechanism. For more detailed device terminal derivations we can once again provide this an extra nodes, we have defined we do not have though so much time to go through that in this course.

So, this is basically gives us the small signal operation and the characteristics that we used in our previous discussion about the channel length modulation.

(Refer Slide Time: 47:09)



So, this characteristics that we obtain it comes state from this equation or you can say this characteristics is being well captured by this equation: the lambda V_{DS} representing the dependency of the drain current on the drain to source voltage. The good MOSFET and ideal MOSFET will be such that lambda is close to 0. So, that the curves is almost flat so that the channel in modulation is almost negligible ΔL is much small as compared to L that is an ideal MOSFET, because what do we need for a good transistor the good transistor is such that the current is being controlled only by the voltage between gate and source then is the good transistor because the transistor operation the voltage across the two-port should control the current flowing cross the third port. The voltage across the third port should not control the current that is a good transistor. So, for our analog operation for good amplification we need good r_o . A very small slope, a very small channel and modulations so there is a ΔL upon L is very small that gives

us better device suitable for analog amplification as we will see in the continuation of this lecture.

So, this is talking about the two small signal parameters g_m and r_o ; we will come back and we will try to combine these two parameters and complete the small signal model of the MOSFET. And on the tau of that we will then try to add the small signal capacitances to develop the high frequency model visit the concept of noise and try to add the noise sources to the MOSFET to complete the model for our circuit analysis. So that is what we are going to do in the next class. And the last session once again we will start with the circuits and try to apply these models for analyzing the circuits for frequency response, for AC analysis, noise analysis, small signal analysis, DC analysis and so on.

So, (Refer Time: 48:56) I will have a introduction section also towards the end, where will try to address some of the key questions that have been posted. So, there is a time for the break right now, we will meet once again after the break; may be after an hour or so at around 1:45 pm.

Thank a lot.