Communication Engineering
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Lecture - 23
The Phase Locked Loop (Contd.)

We will now continue our discussion on the Phase Locked Loop that we have started last time to recap. We had looked at the steady state operation of the phase locked loop, that is assuming that the loop is in lock. We had argued that under certain condition the instantaneous phase of the VCO output of the loop would follow the incoming phase will track the incoming phase.

In the process, the derivative of the input phase d phi by d t and the derivative of the VCO phase would be nearly the same. And therefore, the VCO input voltage could be considered to be the replica of the modulating signal that we want it to get from the demodulator. So, that was one part of the discussion that we had to demonstrate in the steady state if you tap the phase locked loop at the input to the VCO or after the loop filter, after the amplifier.

Then, that output can be considered to be a demodulated output for the FM signal or the angle modulated signal, that particularly for the FM signal that is under consideration that was the first part. The second part was you try to figure out how the locking actually occurs; now in this case we have to go through a non-linear model of the loop. Because we found that the phase locked loop actually is a non-linear system, it is in fact, we obtain a differential equation description for the operation of the phase locked loop.

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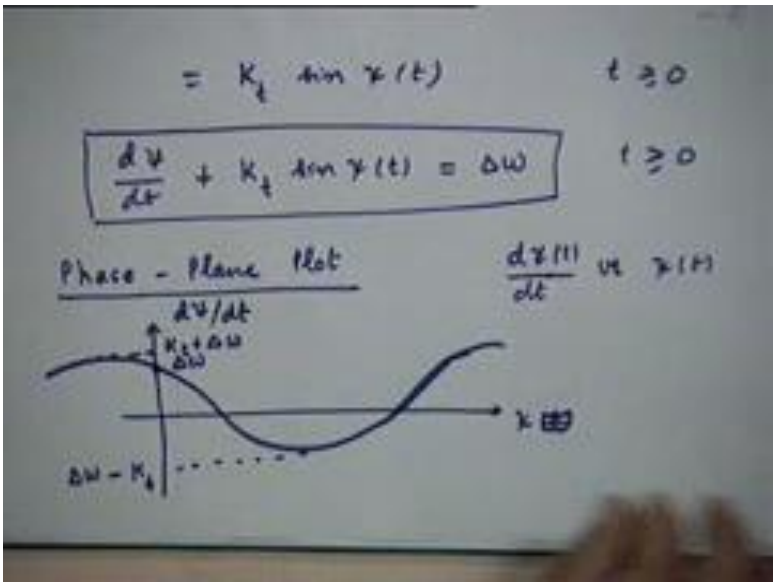

In particular we arrived at this non-linear differential equation, which specifies the instantaneous phase error between incoming phase and the VCO output phase. So, we found that this phase error, follows this non-linear differential equation and you try to look at the operation of the phase locked loop by considering what does this differential equation imply in terms of it is operation. And to do that, we took request to a graphical picture, graphical the picture has this differential equation through the, so called phase plane plot.

In the phase plane plot, basically we plot d psi by d t versus psi of t, so this; obviously, becomes the sinusoidal function with the peak occurring when sin of psi of t is either plus 1 or minus 1. So, let it is plus 1 this gives the delta omega minus K t that is a negative peak, whether it is minus 1 this gives you the peak value as delta omega plus K of t which is the positive peak and at psi equal to 0, this point intersects the d psi by d t x is a delta omega. Because, at that point psi is 0, so d psi by d t is equal to delta omega, so this was a phase plane plot.

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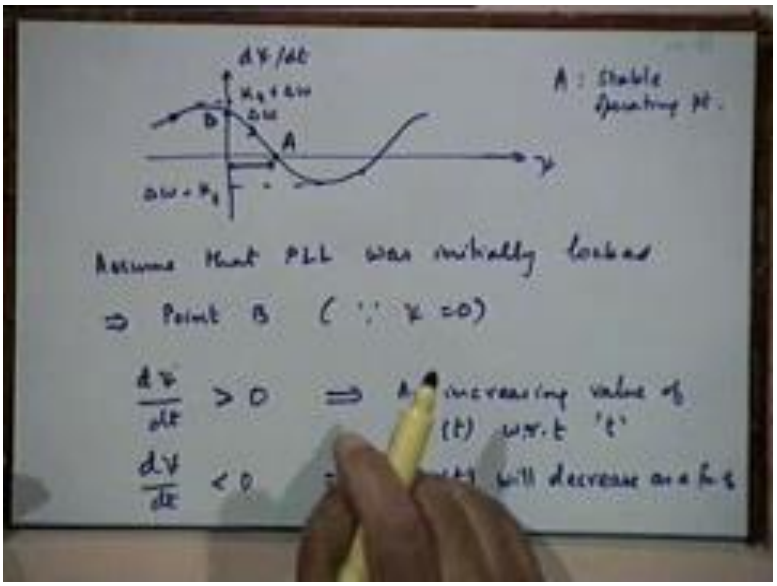

And then, we discussed that this phase plane plot essentially gives you the trajectory of the operating point of the phase locked loop. In the sense for example, if initially you are somewhere here on the trajectory, initially assuming that the steady state phase error was 0. Somehow, initially when we considered a case when all this discussion we did in the context of the step input in the frequency of the incoming signal.

As if your moderating signal was a unit step function of course, we cannot do it in a general, we cannot plot a phase plane plot for the general signal, you have to do it for a specific signal and the specific signal we considered was a unit sub function. So, for this case assuming that initially the loop was in locked at the carrier frequency, we found that the loop will eventually if you move the operating point will move on this trajectory to the right.

And the second important point is the motion on this trajectory will be to the right, if you are in the upper half plane of the trajectory, the motion will be to the left if you are in the lower half plane of the trajectory. And based on this arguments we concluded that, this point A is a stable operating point of the loop, which means that after the frequency step has been applied, the loop will eventually try to come to this condition.

Because, at this point d psi by d t becomes 0; that means, there is no further movement in the operating point. Because there is no derivative, there is no slope psi as the function time becomes the constant value and the constant value is this value, whatever is the

value here this is psi axis. So, whatever is the value of psi at this point is the steady state value of the phase error.

Student: ((Refer Time: 06:37))

They will be many such points, but they all periodically placed, connect such point will be at this value plus 2 pi. So, in as much as phase is anywhere specified modular 2 pi it does not matter, which point you lock on to it hardly matters, phase error. We cannot distinguish between the phase error which is of 1 degree or 361 degrees, it is a really the same thing, so that does not really matter. So, we now proceed further and just do a further little bit of discussion on the phase, on this of what we get from this phase plane plot.

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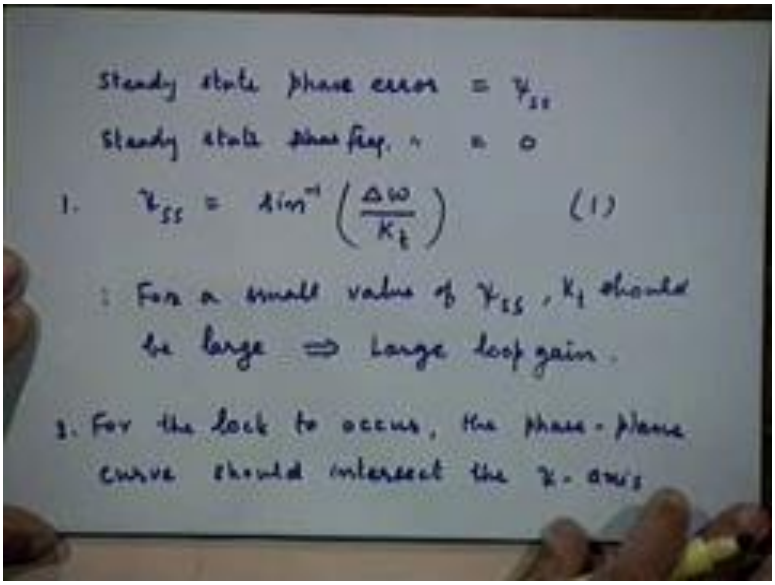

Let us call the steady state phase error of let us denote it by psi sub s s and of course, we said the steady state frequency error would be 0, that is the frequency error. Can you tell me what is the value of psi sub s s is it possible to see from this equation or this plot. If you look at this equation once again ((Refer Time: 08:11)) at the stable point what is the value of d psi by d t that is equal to 0. So, put that equal to 0 you can solve for the corresponding value of psi that will be sin inverse of delta omega by K t.

So, this will be sin inverse of delta omega by K sub t these point, now what does it show, it shows some very important facts. That, if you want the steady state phase error to be

small, what should happen K t's will be large for a given frequency step at the input, if you want the steady state phase error to be small, this argument should be small which will happen. So, for a small value of psi s s K t should be large and what is K sub t if you remember, it is the loop gain is not it. So, basically we are saying that we require a large value for the loop gain.

Now, we require a large value for the loop gain not only for this purpose, but for another very important reason. Let us see, all this discussion was nicely concluded and we could demonstrate the phase plane plot, that indeed the loop will lock in as much as the phase error. Thus comes to a small value, it does not become 0 of course, if you want it to make it 0, if you want to make this steady state phase error equal to 0, you should have a loop gain of infinity, you must have a very, very large value of loop gain.

So, the larger the value of the loop gain, the smaller you can make this steady state phase error. But, nevertheless whether large or small loop gain, the important point was that for it to be come to the stable point. It should have a stable point is not it, now if there is situation where a stable point may not be there at all.

Student: ((Refer Time: 10:38))

Then, delta minus K t is a positive number, so as it in that case this phase plane plot this curve will not intersect this I axis at all and you will always be in the positive half plane. The loop will the trajectory of a operating point will always keep on moving, the operating point will not be able to find a point at which it can stabilize. You keep on attempting to lock, but we will never really be able to lock, there is very interesting way of looking at it.

So, the second important thing to note is that for the lock to occur, so this was let us say the first point, the value of the steady state phase error. For the lock to occur, the phase plane trajectory or phase plane curve should intersect this psi axis.

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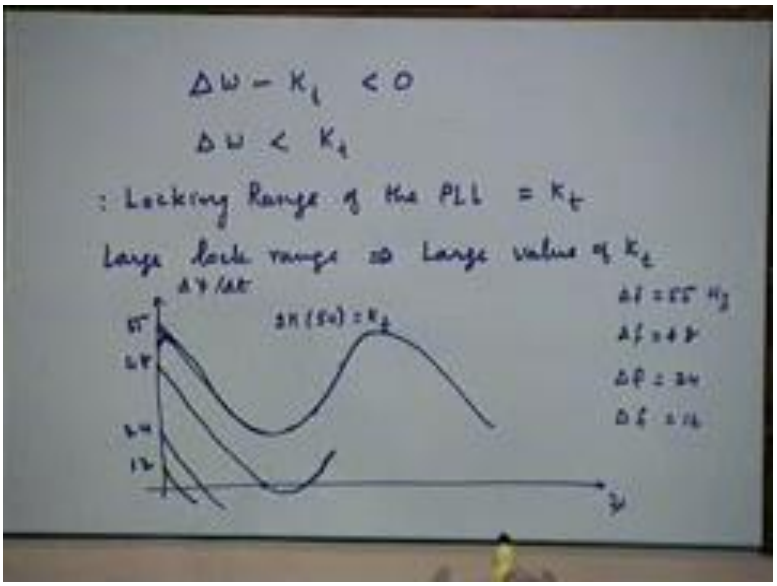

And in order for that to happen what do you need; you need to make sure that delta omega minus K sub t is less than 0. The negative peak of this curve should be negative; I mean the lower peak of this key should be negative, which implies that the delta omega should be less than the loop gain. So, the loop gain plays a very important role in the operation of this system, number one the large value of the loop gain will imply the small value of the steady state phase error.

The large value of the loop gain will also imply a large value of what is called locked range of the loop. So, loop gain in a way besides what is called the locked range or locking range of the PLL, because locking range of the PLL is the maximum frequency step that you can employ, that you can have at the input. And still the loop is able to produce a steady state situation that a frequency error is 0, that is the VCO exactly locks to the input signal frequency.

So, locking range of PLL is equal to K sub t and large lock range requires that we choose a large value of K t. Let me summarize this discussion by showing you a plotting a set of phase plane curves, but different values of K sub t for different values of delta omega or delta f . Let us for this discussion assume that your loop gain is has some fixed value let us arbitrarily chosen the fixed value to be 2 pi into 50, so let us consider the phase locked loop, in which the loop gain has this value.

So, let me now plot the phase plane plots for a different sets of delta omega, so when I choose let us say delta f equal to 55 hertz, that you will say apply a frequency step of that frequency step of 55 hertz of the input. Initially the loop is in lock and you apply a frequency step of 55 hertz, it means delta omega is 2 pi into 55. So, this condition is not satisfied, which means the loop will not the directive will not intersect the psi axis, you will get something like that, it will not intersect the psi axis at all, suppose you make it 48 hertz it will almost just intersect now, but intersect it here.

So, we will now be in the situation like that etcetera, so a stable operating point will exist, but the corresponding steady state error would be quite large, if you make it half of this. So, this is 55 hertz, this is 48, if I make it half of this as you can see the steady state phase error will come down accordingly, if I have it further it will come down further. So, this is the sequence of curves that I have plotted for delta f equal to 55 hertz, 48 hertz, then 24 hertz and 12 hertz. So, this picture says it all it demonstrates very clearly that as we increase the loop gain we get better and better performance from the phase locked loop, any questions here.

Student: ((Refer Time: 16:19))

No.

Student: ((Refer Time: 16:30))

The same thing will apply you thing about it, the frequency step in either direction would imply the same thing, in a way you are saying if I agree with you. What you are saying is precisely the same thing what happened thank you, you can make it delta omega model, because positive of frequency negative only the roles will get into exchange.

So, that also means something else; that means, even in the steady state I cannot always use a linear approximation that I discussed earlier, do you agree. That, because a linear approximation to be valid what is an assumption that you made, that psi of t is very small. But, suppose your loop gain is not very large and delta omega is quite large, you could have a very large value of the steady state phase error and therefore, for that value of the steady state phase error, I cannot assume sin of psi of t is equal to psi of t.

So, the linear approximation that we considered would not be available for use even in the steady state, if your steady state phase error is not very small. So, it is therefore, imperative that if you want to use linear approximation in the steady state at this ((Refer Time: 17:57)). And it is useful to look at that small phase error approximation or linear approximation to the steady state behavior of the loop at least approximate behavior, if not exact.

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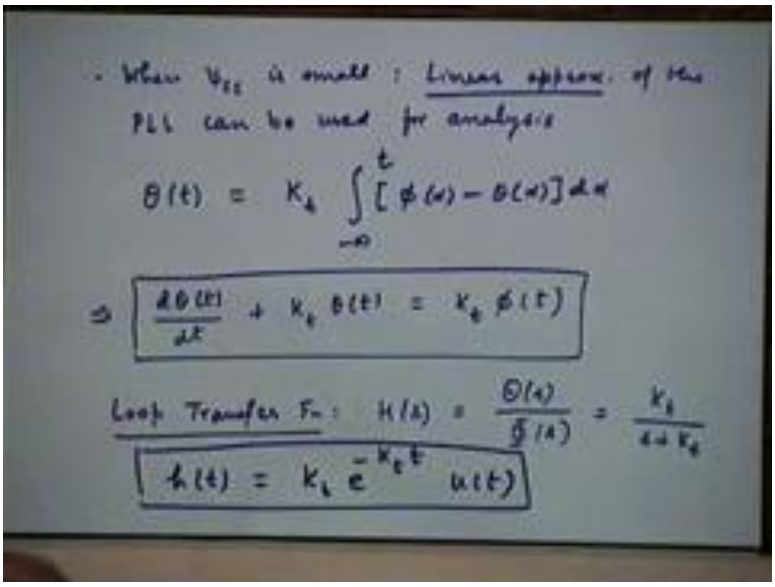

So, when psi s s is small we can use the linear approximation can be used for analysis, what does it mean, if remember your final equation from which we derived the differential equation first. That theta of t was equal to K sub t integral of theta of t is an instantaneous phase of the VCO output, this all this was equal to K sub t times there it was sin of phi alpha minus theta alpha t alpha. If you are going to use a linear approximation, that sin can be removed and we can simply write it as phi of alpha minus theta of alpha d alpha.

And if you want to convert this into the corresponding differential equation, this will becomes d theta by d t plus K t theta t. So, instead of sin theta t you have K t theta t is equal to instead of K t sin psi t, you can write this K t phi of t this is a linear differential equation. So, when the linear approximation is valid the loop is now describe at or near the steady state by a linear differential equation and when that is, so it is possible to study it much more conveniently.

Because, we know how to study this linear differential equation, let us say by Laplace transforms, in fact we can obtain a transfer function model of the loop. For example, I could define a loop transfer function, sometimes also called the close loop transfer function with as a ratio of the Laplace transform, the output and the input. And what is the output here, output is theta of t, the final phase of the VCO and the input is phi of t, the incoming phase function.

So, I define the loop transfer function H of s as theta of s upon phi of s, definition of any transfer function is Laplace transform of the output variable Laplace transform of the input that is what we are doing. We are considering the VCO output phase as the output here, may be the Laplace transform of that is the input incoming phase function, which is phi of t Laplace transform of that is phi of s.

So, what will be the value of the transfer function here, you can derive it from here by just taking the Laplace transform of both the sides, can you tell me what will be the value of theta s upon phi s from this differential equation, it will be simply K sub t upon s plus K sub t. And the corresponding h t, the corresponding impulse response we can write as K sub t e to the power minus K sub t into t u t, that shows that is unit step at the input there is not produce, the unit step at the output in which you create goes through the exponential function, impulse function of the input not the unit step, this is the impulse response.

An impulse function at the input does not produce an impulse function in terms of the output, but some other impulse some response which is an exponential ((Refer Time: 23:09)) response. This will ideally if you do not want the system to do any distortion of any kind, then this h of t should be equal to delta t itself, under what condition will this converts to delta t when K t it becomes very large.

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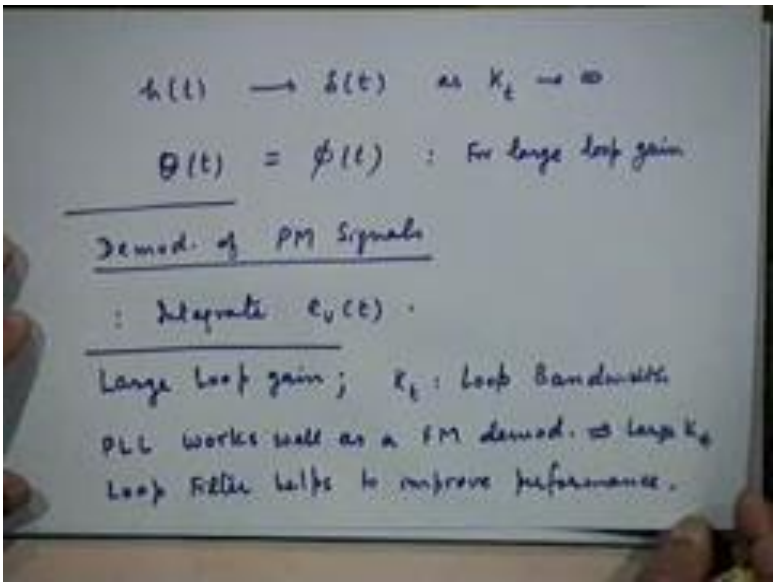

So, h t will converge to delta t or will tend towards delta t as K t tends to infinity and when that happens your theta of t would be the same thing as phi of t, there will be no phase error for large loop gain. So, no much of how you look at it needs the same result, before we proceed further suppose I ask you the question, that I want to use the PLL for demodulating phase modulated signals, what will I do, how should I do that, demodulation of PM signals, what is the answer you should integrate the output of the demodulator of FM demodulator.

So, just take the integral at integral of e sub t, so integrate e sub v t that will produce a required demodulator, let us do for any you know you have the FM demodulator output, and if you want the demodulator phase modulated signal, you just have to integrate the output of the FM demodulator standard result. Some final remarks before we go on to some other discussion of the PLL; yes, is there any question?

So, what we notice from this discussion is, that the large loop gain is crucial, large loop gain incidentally ((Refer Time: 25:43)) if you look at this transfer function, suppose you think of this transfer function purely as a filter, what is a bandwidth of this filter let us say the 3 dB bandwidth. Now, looking at the loop transfer function as the filter, you have transfer function K t upon s plus K t, what is a 3 dB point of this transfer function. It is a low pass function you can see that is not it as omega increases, the value will come down it will attenuate the signal more and more, what is that 3 dB point s is equal to K t.

So, you can think of K t as the 3 dB bandwidth of the loop or K sub t also, so K sub t has a lot of significance, K sub t is the lock range, K sub t besides the steady state value of the phase error, K sub t can also be considered to be what is called the loop bandwidth. So, K sub t can also be construct with in this particular case, the loop bandwidth, so what we are saying is, that if you want a good performance from the phase locked loop, in terms of steady state phase error, in terms of lock range and consequently in terms of demodulation of FM signal, you would require either a large loop gain or equivalently a large loop bandwidth.

Now, that is usually, so if you want to the PLL to work properly as a FM demodulator, again you want large value of K sub t, these are the conclusions we are instinct. Now, large loop gain is not always possible, it is very difficult it also has some problems associated with it ((Refer Time: 28:07)) which will not go into right now, but it is usually not easy to realize a very large loop gain. So, you need to think of improving the performance, when we do not have sufficiently loop gain.

And one way of improving the performance is you know remember this loop that this analysis that we have done is for a very specific situation, when we have removed the loop filter. So, one of the advantages of using the including the loop filters is that we can relax on this condition that we have on the loop gain. So, presence of loop filters helps, only thing is the moment we have loop filters our analysis becomes much more complex is it not? Because I can no longer write that differential equation, so easily have to also consider the how the filter effects the differential equation.

So, far the phase detector output except for the multiplication by the loop gain was directly going into the VCO input. So, it is very easy to relate the VCO phase output to each input, it was very easy through that integral or through the differential equation. The moment you have an addition of filter coming between these two, you have to also see how that affects the entire description, in terms of either differential equation or integral equation. It is not, cannot be done; it just becomes little more complicated. At the moment we will not going to that, but we will have a very deep discussion of the at least one more loop where the loop filter.

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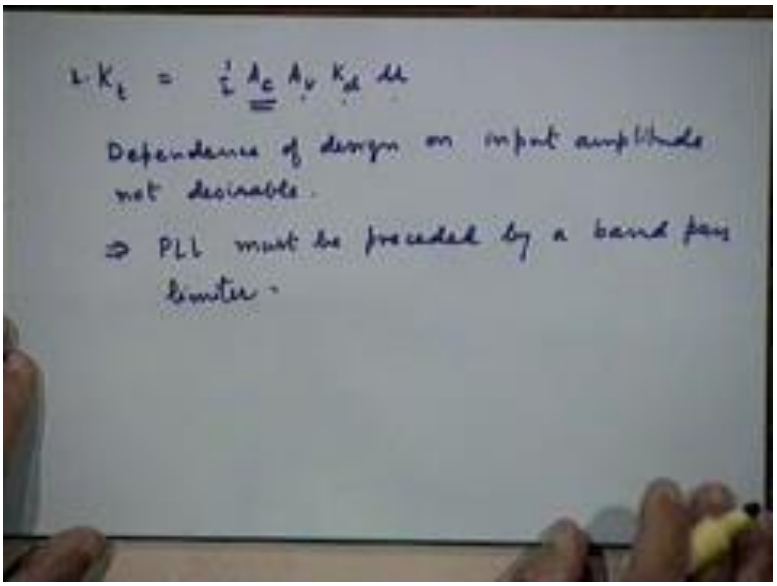

Now, the second remark is look at the value of K sub t, that is given by I do not remember the exact value it is half A c, A b, K sub d anything else mu there are, so many factors which determine the value of the loop gain, what is it mean if you first of all input signal amplitude itself has a effect on the loop gain. Now, other thing of course, more or less constant of the PLL itself, A v is associated with the VCO, K sub d is associated with the phase detector, mu is the gain that you have incorporated in the phase locked loop.

So, these three are constants of the loop, but A sub c is a constant associated with an input signal, that is not a very nice thing to have you do not want a loop design to be dependent on the amplitude of the input signal. Because, if that is, so the input signal has the weak amplitude, the loop gain goes down input signal has a stronger amplitude, the loop gain goes up let us not very desire about.

So, dependence of because, otherwise what we have to do is, we have to design the loop for operating to a certain signal amplitude and the signal amplitude changes, if you have value of K sub t changes and then you all your design is gone. So, dependence of design on input amplitude not desirable, can you suggest a way of removing this dependence.

Student: ((Refer Time: 31:51))

And show that the input signal always has a constant amplitude, input FM signal always has a constant amplitude and we know one method of doing that the bank pass limiter. So we can precede the PLL by a bank pass limiter, good that is a very good answer.

Student: ((Refer Time: 32:25))

Good question, I think I forgot to mention that, the question let me repeat the question. For this complete discussion I have taken the input signal to be a cosine function, and the VCO output to be a sin function, why did I do that when you see the...

Student: ((Refer Time: 32:50))

That is right, because I am how am I real it depends on how you realize your phase detector, I am realizing the phase detector by multiplying the two signals and low pass filter in the output. When, I multiply cosine with sin I will get a difference component will be sin, if on the other hand multiply cosine with cosine, the difference frequency will be a cosine function. The cosine function will not be sensitive to the sin of the phase error, it only decide the magnitude of phase error and you cannot track the phase locked loop will not be able to work properly.

Because, it must not only know what is the phase error, so that the phase error can be driven to 0, it must also know whether the phase error is positive or negative you want to be sensitive to the phase error. So, it is important that this it is also automatically works like that, so in a locked condition it is implied that if the input signal is cosine, the output signal will be sine that is there will be pi by 2 phase shift between the input signal and the demodulated signal.

So, the input sign carrier is cosine to phi of c t, the VCO output will be sine to phi of c t, this will automatically happen. Because, you have close loop and the close loop will work like that, that was the good question I forgot to mention about that earlier. Now, what can we do about the removal of these disadvantages of the first order loop, this loop that we discuss is called a first order loop.

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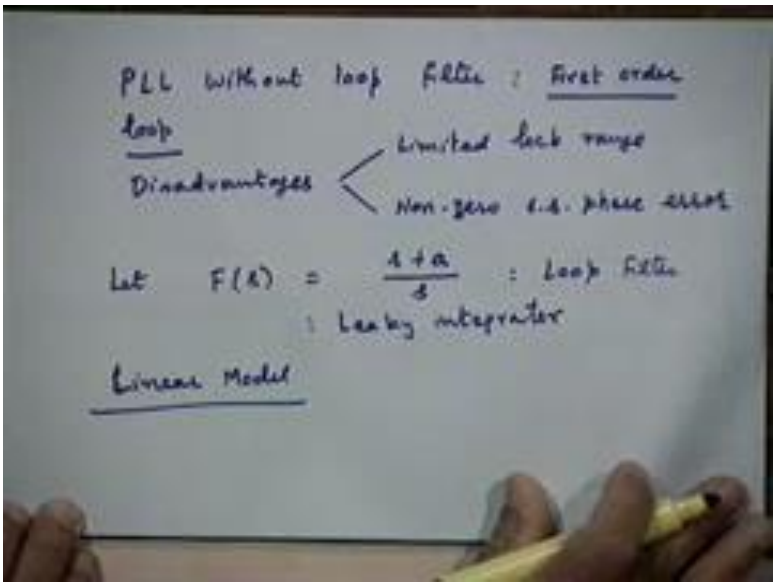

So, loop the PLL without the loop filter, now can you also see why it is called a first order loop.

Student: ((Refer Time: 34:48))

That is one way of looking at it and another consequence of that is through the transfer function that we had, the loop transfer function K t upon s plus K t is the first order transfer function. So, that is why we call it a first order loop, it has the disadvantages that we already seen, there are two basic disadvantages which lead to non-optimum performance. One is a limited lock range and the second is a non zero steady state phase error, these are the two disadvantages that we are discussed, can we do something about it.

As I mentioned we can try to remove both these disadvantages by using a loop filter of an appropriate kind. To illustrate that can be done, that in deed happens let us consider a loop in which we choose a loop filter to the transfer function like this. This is the transfer function not of the loop, but of the filter in the loop that we are going to put, which we are omitted in this discussion. This is as you can see, essentially an integrator the second part a by s is an integrator, the first part is one which allows your input signal to just go out, such an integrator is called a leaky integrator.

Because, it allows an input signal to leak through to the output, as well as the component will come after integration. So, this essentially what is called a leaky integrator, so basically your linear model let us consider the linear model for the simplicity of discussion, because the non-linear model will become very complex now. The phase plane plot the differential equation will be second order differential equation now.

Because, if one order differential equation is contributed by the loop filter and one order the differential equation contributed by the relationship between the VCO output and the VCO input, because there is an integral relationship there. So, this will become a second order differential equation and the phase plane plot will be much more complex now, we will not go in to all that discussion. We will consider the steady state operation, I will at least prove through steady state argument, that you need it is now possible to get both these things are you looking for, so we look at that.

Student: ((Refer Time: 37:56))

No, I think it need not like to have any phase error, after the locking has occurred as long as the phase error is there we should know whether it is positive or negative. So, that loop can operate itself to drive the phase error to zero, the ultimate goal of the phase lock loop and that is why it is, so called is to drive the phase error to zero, in whichever direction is the current phase error may be.

Student: ((Refer Time: 38:34))

I thought I already answer that question, if you still have the doubt we will discuss it separately ((Refer Time: 38:49)). Let me return to this, so let me consider the small error model or the linear model for this case.

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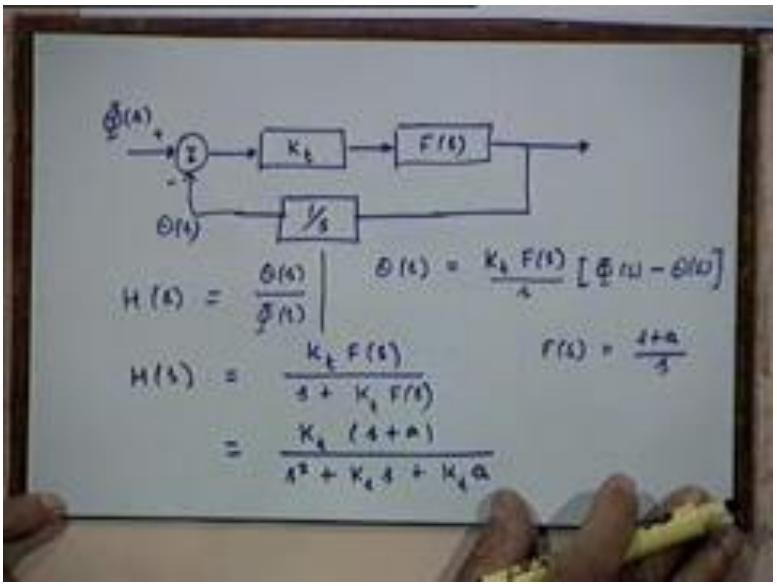

So, what is the linear model for this case, we have this I have removed the sinusoidal non-linearity here, because I am considering a linear model. The input is phi of s, the VCO output is theta of s, this is the loop gain I am denoting it by a block and what we are now introduced additionally is a loop filter with transfer function f of s as given. The output of this is fed to the VCO and the VCO here will be represented by a transfer function of 1 by s it is an integrated, so it is transfer function is 1 by s and you are taking the demodulated output over here.

So, what is the close loop transfer function here H of s equal to theta of s upon phi of s we need to find that out, if you do that, so we need to find this to be let us proceed step by step, let us write an expression for theta of s which is equal to can I write it in terms of this point here. Suppose, I go through the loop like this, it is K t times f s times into 1 by s of the fully transform of the signal here and what is that phi of s minus theta of s.

So, basically it is K sub t into f s upon s of phi of s minus theta of s just let in the transfer function it is a cascade of three functions. Now, you can solve for theta of s, take this theta of s to the left hand side let us solve for that, so if you do that and compute theta s upon phi of s it is very easy to do that. So, I leave that as an exercise you can check this out and this becomes equal to K t times f s upon s plus K t times f s and substitute for f of s as equal to s plus a upon s this becomes K t times s plus a upon s square plus K sub t s plus K sub t a, so that is what you have here.

So, it becomes a second order loop because, your transfer function is a second order transfer function. So, when you use a first order filter as a loop filter which is a first order filter, the loop becomes the second order loop, the loop transfer function has denominator degree which is two.

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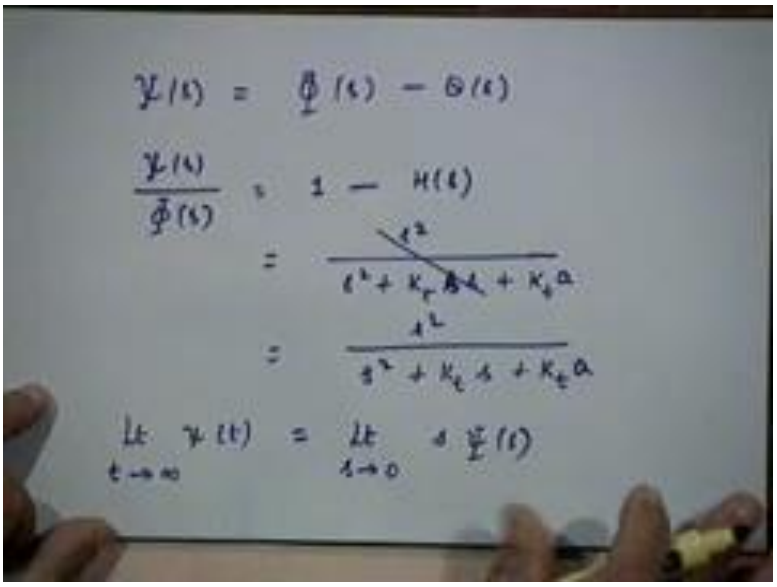

We are interested to look at the phase error, so it will be interesting to look at psi of s, the phase error. The phase error is phi of s minus theta of s, if about to consider the transfer function let us say between psi of s and in the input phi of s that will become 1 minus H of s if I divide both sides with phi of s. And if I do that, you can see that if I substitute for H of s from the expression that we just derived, this expression here this will become s square upon the same denominator as before s square plus K t s K t a s plus K t.

Student: ((Refer Time: 43:51))

K t.

Student: ((Refer Time: 43:55))

It will be K t s, so I rewrite it s square by s square plus K sub t s plus K sub t.

Student: ((Refer Time: 44:09))

Now, from this can I say something about the steady state phase error from this transfer function is it possible to say something about the steady state phase error, even without

going through that non-linear analysis. There is a final value theorem that you know the Laplace transforms, what is the final value theorem. Suppose I want to find limit of psi of t, s t tends to infinity, this is limit of s tends to 0 of s time psi of s of course, to do that I must first consider some kind of input, I have to say something about phi of s.

Let us present the same kind of input that we are talking about earlier, let us say that input is a frequency step. So, if the input is a frequency step what can you say about phi of t, the input frequency is a frequency step what happens to the phase will be integral of that, the phase will be integral of the d phi by d t, d phi by d t has a frequency step.

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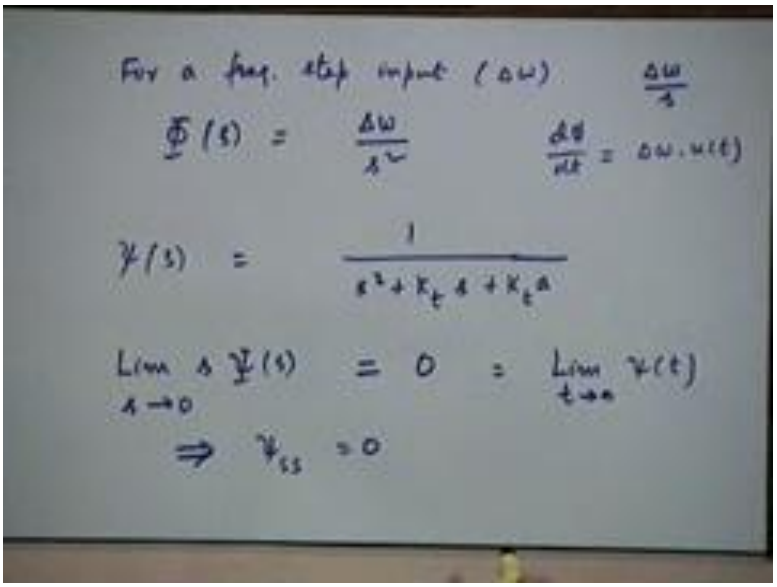

So, phi of t rather phi of s what can you say about phi of s, so for a frequency step input, the frequency step of delta omega, you can say that the phi of s is nothing but, see frequency step itself means that the Laplace transform of this would be delta omega by s, Laplace transform of the integral of that will be delta omega by h square. So, phi of s will become delta omega by h square are you with me on this, all of you, the frequency step that is your d phi by d t is delta omega u t, that is what a frequency step of the input means.

So, therefore, phi of t would be integral of this the Laplace transform of this is delta omega by s, because Laplace transform of u t is 1 by s. Laplace transform of phi of t will be another multiplication of 1 by s, so that becomes by delta omega by h square. So, now

substituting that in the expression for psi s upon phi s I am taking phi s on the right hand side, what do you get psi of s would be equal to 1 upon s square plus K t s plus K t a.

Now, take the limit of s psi of s as s tends to 0 what do you get it becomes 0, so it is implies that the steady state phase error is because this is nothing but, what you want limit t tends to infinity of psi of t, so the steady state phase error is equal to 0. Similarly, you can argue I leave that as an exercise for you to complete, that the steady state frequency error would be zero. In fact, that is trivially obvious from this, because frequency error is going to be derivative of the phase error, so if this is 0 that will also be 0.

So, a second order loop removes both the disadvantages of first order loop; however, the only difficulty is the complexity of analysis, this analysis that we have done is a very approximate linear analysis, which is valid around the locking situation whether loop is nearly in the lock. So, that the linear approximation can be assumed to be valid, otherwise the proper non-linear analysis which will of course, lead you to the same conclusion, would actually show much more clearly how the locking actually occurs.

Because, you will have to be able to again see that how the track operating point varies as a function of let us say psi. In this case you will find, that the phase plane plot is not a very simple sinusoidal curve, it is a very complex curve and it does not it is typically sinusoidal curve which gradually keeps on approaching the psi axis. And eventually needs or cuts the psi axis at a fair equal amount of distance, after going to many, many cycles rather than every cycle, in the first order loop the sinusoidal curve was intersecting the psi axis every cycle every two pi radians, that will not happen there.

So, the actual non-linear analysis will show all that, that there is a lot of what is called cycles slipping taking, taking place before the lock actually occurs. But, I am skipping all that analysis, we do not have time for all that it is a very detailed treatment of the phase lock loop, which you can if you are interested learn by yourself, it is a very complex system to study, because it is a non-linear system. So, I think that is sufficient discussion for the phase locked loop, but this is not the only kind of feedback demodulator we can have for frequency modulation.

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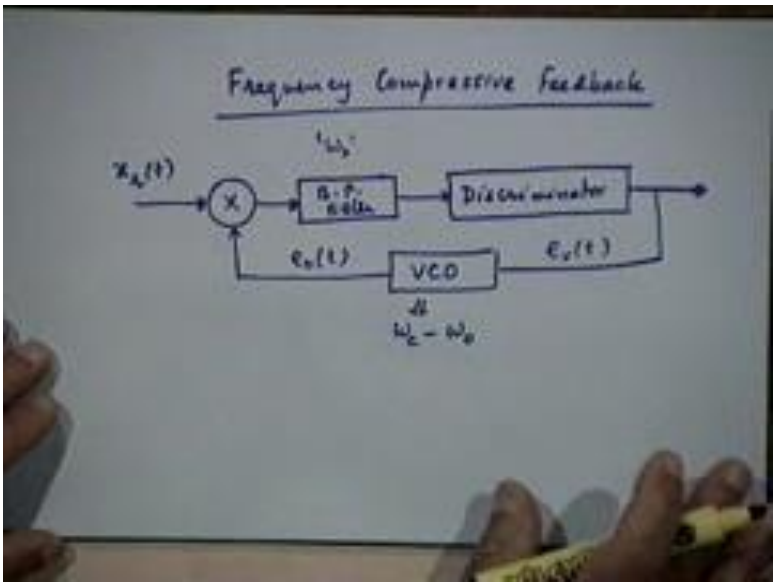

There is another very interesting variant of phase locked loop, which is often used in for demodulating FM signals more or less for the same purpose that the PLL is used, which is called system with frequency compressive feedback, which is very similar to a phase locked loop, but there are some major differences. Let us look at the block diagram, you have an input signal x sub r t I have a multiplier I do not call it a phase detector any more, I call it a multiplier I had the phase detector also as a multiplier, but that was followed by a low pass filter.

So, that to make the phase detector I will not follow it up with a low pass filter, I will follow it up with the bank pass filter, that may be very surprising. And because, this will not make sense if the carrier frequency here and here are same is it not? Because if the carrier frequency here and here are same, then the difference component will always be proportional will always be center around 0, so I do not bank pass filter serve will serve no purpose.

So, it obviously, implies that the VCO output is not at the same carrier frequency as the input or in the lock condition also, it is at a different carrier frequency. Here, as in the phase locked loop the carrier frequency at the VCO or the lock conditions will be the same as that of the input signal. So, therefore, it is implied here that the VCO works differently here, now what will happen then that you will have a signal here which is at

some finite carrier frequency, which will depend on the centre frequency of this bank pass filter and will depend on the frequency of the VCO here.

This I will follow it up with discriminator again, it is a very intriguing kind of structure and all kinds of questions should come to your mind, when I am plotting this. And here is a demodulated output and here is a feedback loop, which contains the VCO again, where the center frequency of the VCO is omega c minus omega 0 at the bank pass filter as the center frequency of omega 0.

So, we will once again call it e sub v t, e sub o t and now there must be lot of question in your mind, I have a discriminator in this loop. And natural question that will arise is if I am going to use the discriminator anyway inside the loop, why should I have this device at all I could as well straightaway use the frequency discriminator and demodulator of FM signal. So, why all this complicate, so how this works and what are the advantages of this structure over the simple straight forward discriminator are issues that will discuss in the next class.

Thank you very much.