Advanced VLSI Design
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Lecture - 33
Introduction to VLSI Testing

Good day. Welcome to the module on VLSI testing for the course of Advanced VLSI Design. So I am Virendra Singh from Indian Institute of Technology, Bombay. I would take you through the various challenges in VLSI testing and the solutions for that. The outline of this lecture would be introduction of VLSI test, the VLSI design flow, VLSI test challenges, Test economics and basics of VLSI test.

I acknowledge the help of or support of Prof Vishwani, Prof Adit Singh, Prof Fujiwara, Prof Saluja and Prof Samiha who help me preparing this course material. So as Prof Chandorkar mentioned you in the very beginning that VLSI or chip design has gone through the various phases. If I look at the history of microprocessor it is started from 4004 and now we have dual core or quad core kind of processors which are implemented with nearly billion transistors.

And now as he mentioned in his very introductory lecture that the cost of the design manufacturing of a chip is nowadays more or less governed by the testing of a chip. He roughly mentioned some figures that it cost you about 200 dollars per hour if you put it one test or two test. So that means here if you happen to test your chip for an hour you need to spend 200 dollars that is a huge amount.

And that may not be feasible for a commodity processor or that kind of device to spent 200 dollars for that. So now I will take you through why this kind of cost incur in testing of a system chip. As we know that here most of the chips we are fabricating have some kind of fabrication defects. If they have fabrication defects in that case, we have to carefully test each and every device if it is a faulty in that case we have to reject those devices.

If it is fault free we have to ship those devices and get revenue out of it. Some of the devices are not faulty, but they have some weak faults those are latent faults those are not pronounced at the time of manufacturing, but as it works or function in the field these effects pronounce

and then here device will fail after working for few weeks to months and so we also want to reject these kinds of weak devices and generally we need to take these devices through a stress test that often referred as burn-in test in VLSI test domain.

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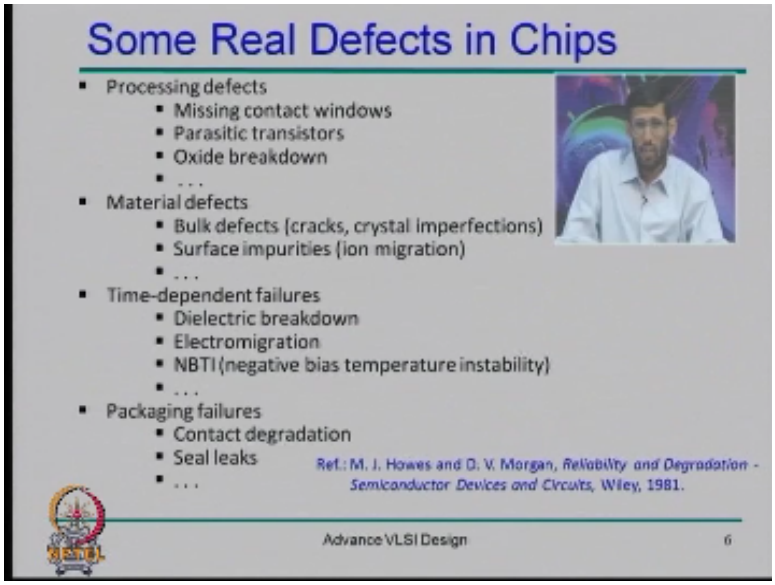

If you look at what kind of defects that may incur in the manufacturing process like there are some of the processing related defects which may incur while you are printing your circuit on the chip. There may be like formation of parasitic transistors, there may be missing contact window, there may be oxide breakdown. There might be some defects which are related to material like here surface is not clear or surface impurities are there might be crystal imperfections.

There are some time dependent failures that may occur those are not presented the moment you are fabricating, but like dielectric breakdown or electromigration mean here when devices is operating some metal may migrate due to the heat and so that may result into a open. And the other dominating effect nowadays coming up is negative bias thermal instability.

Whenever a PMOS transistor operative under negative bias its threshold voltage increases eventually the delay of the transistors increases. Hence your circuit operates slower than it was desired. Then there are packaging related failures like a contact degradation so on and so forth. So many of the defects that may occur when you are manufacturing a chip some of the defects are also time dependent which are occurring while chip is under operation.

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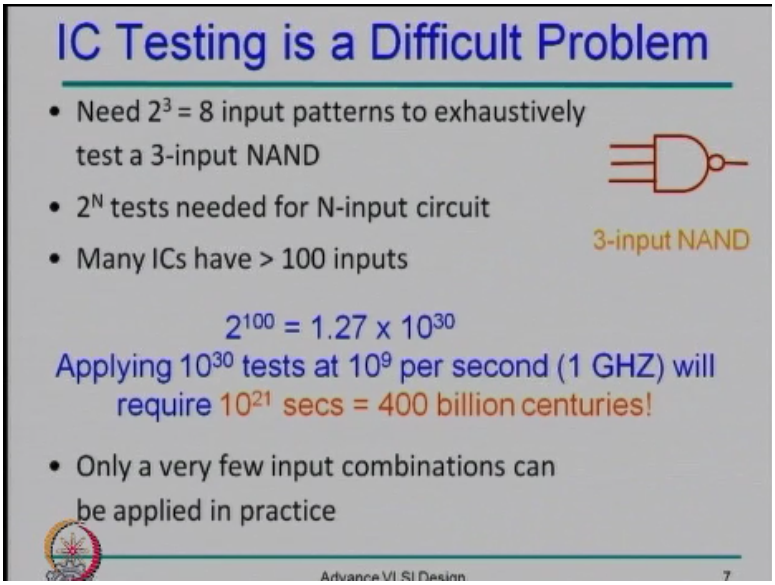

Now let us look at how difficult the test process is. I guess all of us have gone through this kind of exercise to test whether a chip is faulty or fault free and what often we do. We try to apply all possible inputs to a chip and then try to see whether we are getting the correct output or not. Like here if I have see this 3 input NAND gate if I want to test it here I need to apply all eight inputs to this AND gate.

And I have to check whether the resulting output is correct or not. So in this case here I need to apply eight inputs. If there are N number of inputs then I need to apply 2 raise to the power N inputs this kind of test is known as functional test. Once I apply this test and figure out the devices is correct I do not bother about the defect that may occur while it was under fabrication.

Though here the time dependent defects might still be off concern to us. So like here in today's device we may easily have hundreds of inputs when there are hundreds of input you may need to apply 2 raise to the power 100 input that roughly equal to 10 test to the power 30 if you apply these inputs by a very fast tester that can operate at one gigahertz you may need 10 test to the power 21 seconds that is roughly about 400 billion century.

That mean here one chip you have fabricated today that would be ready to use after 400 billion centuries it impractical. So this tells you the difficulty in the testing. Now here our aim is to test a chip in reasonable amount of time not in billions of centuries and reasonable amount of time I will come to that point little bit later, reasonable amount of time is few seconds to few minutes.

Due to several reasons I cannot wait for several centuries. So that means here if I want to apply in few seconds to few minutes I can apply only very small subset of these 2 raise to the power 100 inputs. Now the biggest challenge is how to find out that subset of 2 raise to the power 100 inputs that can give me the similar kind of confidence that your device is defect free or your chip is defect free so that it is ready to use.

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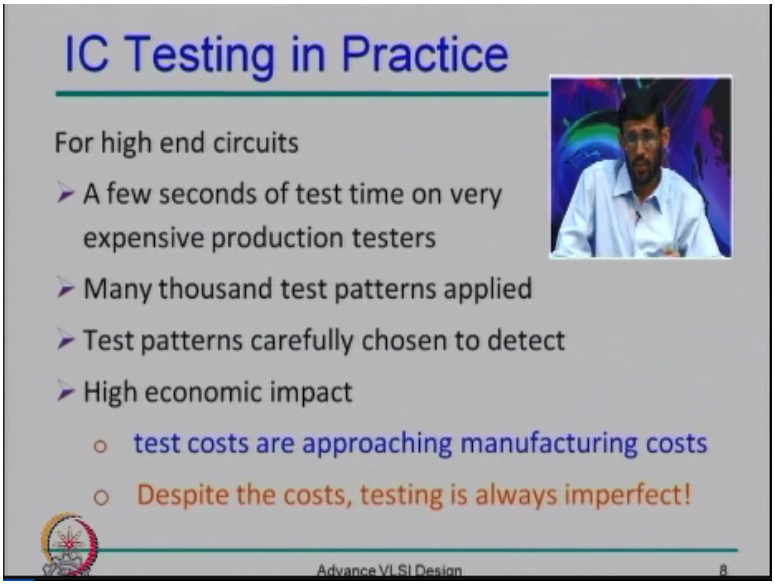

Now for all the high end circuits like why I have written high end circuit because for some of the chips like twice you even do not need to test because it is expensive. Now the test time is few seconds to few minutes and every manufacture chip must be tested. So that means here we have to apply many thousands test patterns in few minutes to few seconds. So that means here we have to choose these pattern carefully.

So that this can be applied in reasonable amount of time which is few seconds to few minutes. So now this has impact on economics and what that impact is now if you look at the test cost to apply a test for few minutes that reaches roughly nearly equal to the total manufacturing and design cost. Though, despite all these cost here still testing IC imperfect because I can never apply those exhaustive test set.

But here still I want to get the similar confidence which I would have obtain by applying 2 raise to the power 100 test.

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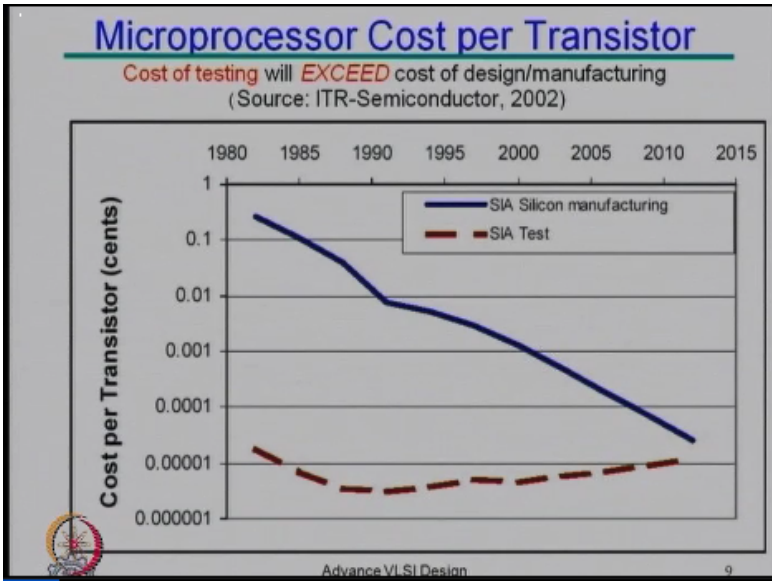

So this slide tells you which was given by ITRS in 2002 what they speculate is that sometimes in 2013 or 2012 the total cost of design and test design and manufacturing of a transistor would be nearly equal to the total test cost of a transistor that is really worrying. Now that means the test has the equal share as design and manufacturing in IC and if it exceeds in that case here the total cost would be dominated by the test.

That means here, we should be careful and we have to have good methodology to test a device. So that we can get the very high confidence and with very minimal cost. So engineering is all about economics always you have to develop a cost effective solution. So we have to device a methodology so that here we can test device in reasonable time and we can get the similar kind of confidence that we would have obtained by applying exhaustively the test.

So the other thing that affects the economics is like due to the defects and if some of the defects are systematic defects. That means there is something wrong with your process you have to set process right.

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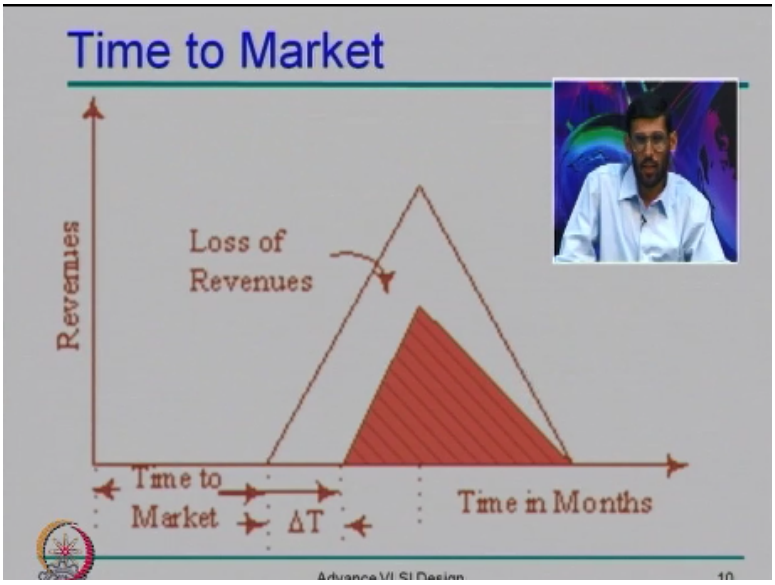

And in this exercise your time to market may be delayed and this area under this curve tells you that how much revenue you can get. In the beginning, you can get really very high revenue, but here as time passes the revenue per product decreases because now you have many competitor's products in the market and hence your sale reduces or your market share reduces and hence you will have less and less revenue therefore you have to reduce the cost.

So initially you can sell a device at higher cost. Now if there is a escalate in the time to market by few months said here delta T now the revenue will reduce to this one and companies they reported that if there is a delay by 6 months in launching a product the revenue drop maybe roughly equal to 30% that is as really big numbers. So the companies are very aggressive in launching their product, but they also want to make sure that quality is very good.

Otherwise it is not the revenue loss their image is also in stack so that gives bad impression in the market and hence they also do not want to do that so there is always a trade off.

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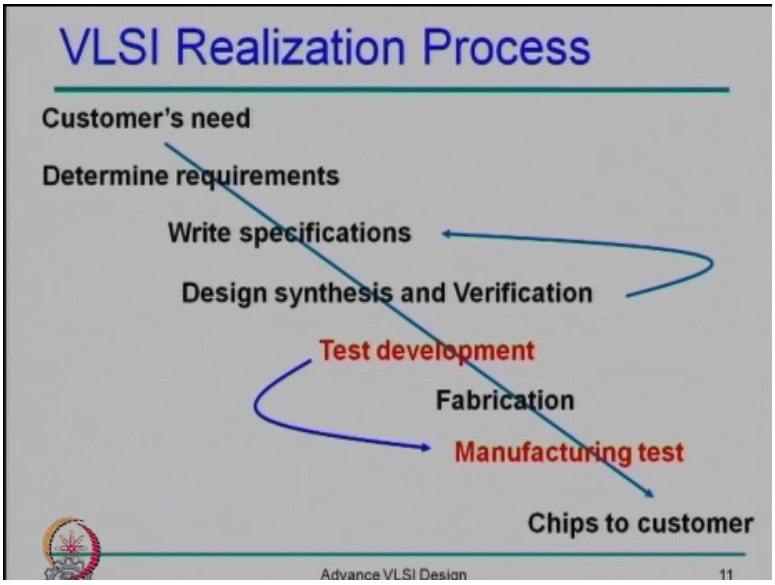

Now come to the VLSI Realization process and let us look at where exactly it contributes. So where exactly your test appears in the design flow, you know, design flow starts from the customer needs and customer has some kind of vague requirement. He may say that I want to build microwave controller and in that microwave controller if I put milk in this. This should operate let say 300 watts for 5 minutes if I want to cook a rice then it should operate at say 250 watts for 15 minutes so on and so forth.

So from that customer needs the engineer must analyze the requirement and determine what exactly their requirement is and from that requirement they have to prepare the specification these specifications are most of the time written in hardware description language HDL that may be Verilog or VHDL or system C and from that SDL often we use the cad tools that can synthesize your design.

So that means here from this specification you write RTL then RTL you again synthesize as gate level netlist then you do the place and route and finally you do the tape out you produce GDS2. So here I want to point out that at every level of synthesis you need to verify whether your design or synthesized RTL or gate level netlist is correct in functionality vis-à-vis specifications that you have written down.

Then once you have GDS2 you sent it to fab. Fab will fabricate your circuit and then give it back to you. Now you want to make sure that every device has no manufacturing defect. It is defect free only in that case you can sell it to the customer. So now here after fabrication you have to test each and every chip. Now here as we discussed you cannot apply exhaustive test

set to each and every chip.

So what you need to do is you need to find out a small test set that can test your chip give you the very high confidence in the manufacture chip that it is defect free. So for that here often so you need to generate the test that process is referred as test development. Generally, we need gate level netlist for this. So now we can start this process before fabrication process. So test development process is one-time process for a chip design whereas manufacturing test application is recurring cost you have to test each and every chip.

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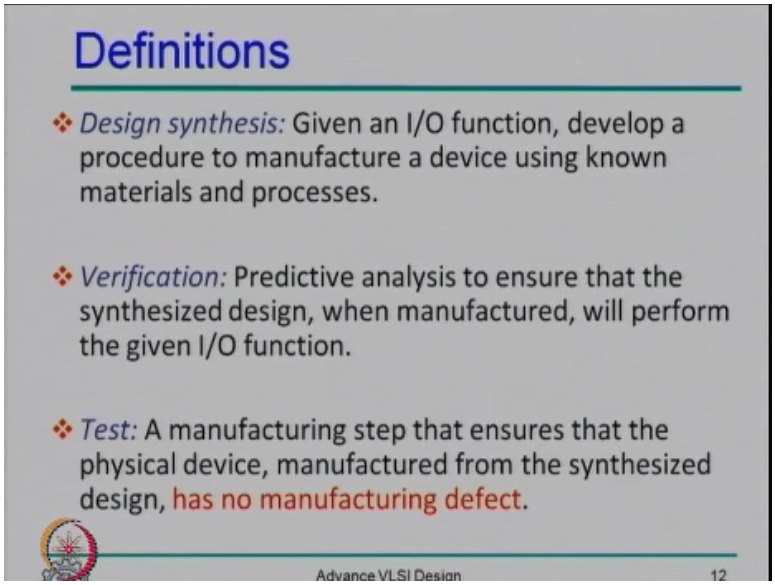

There are couple of definitions we often use in VLSI one is the design synthesis that is defined as for a given IO function we need to develop a procedure to manufacture a device using known materials and processes. The verification is defined as predictive analysis of the design to ensure that synthesized design when it will be manufactured will perform the given input output function.

And test is a manufacturing step that ensures that the physical device manufactured from the synthesized design has no manufacturing defects.

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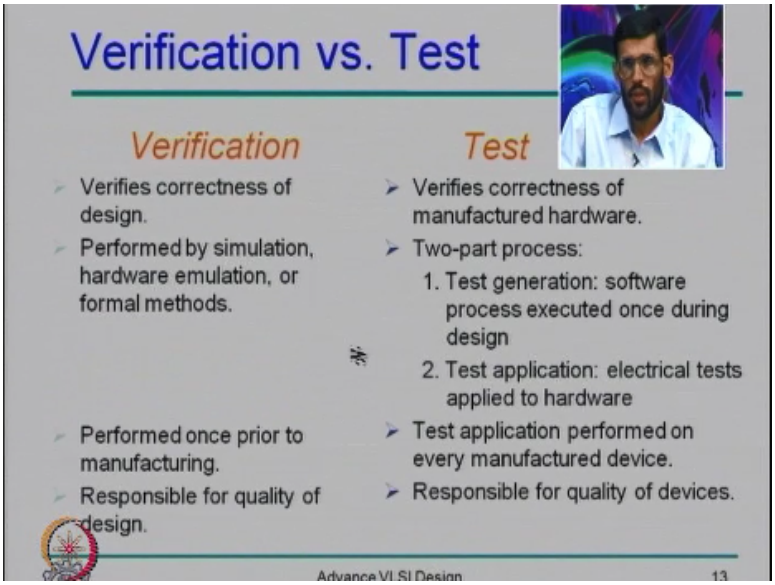

Often people confuse between a verification and test. Here just briefly I would like to tell you about the difference between verification and test. Verification is responsible to verify the correctness of the design so that means here whatever design you have made that is correct with respect to the specifications. Now the verification ensures the correctness of manufactured hardware. Test ensures the correctness of manufactured device.

Verifications is performed by simulation I guess all of you are familiar with the simulation based verification, but simulations is much slower process. So then here often companies do use emulations wherein they emulate the design on some reconfigurable platform and try to exercise as many vectors as they can and try to ensure the correctness of the design and the more correct way is the formal method maybe in this course.

And some other lectures will deal with the formal techniques how you can use the formal techniques to verify your design. If you look at the test here it is two step process. One step is to develop the test that means here you want to develop a small test set that can be applied in reasonable time and reasonable time is few seconds to few minutes and other thing is the test applications.

So test application is recurring so that means here you have to test each and every chip. So that means here these vectors you have to apply on the manufactured chip by using automatic test equipment. A verification is performed prior to the manufacturing so that means here it is more or less the software process you have Verilog or VHDL design and you want to perform the verification on that.

Whereas the test has two parts. First part is one-time process whereas the second part is applied to each and every manufactured device. Verification is responsible for quality of design how good quality design you are producing whereas the test is responsible for the quality of the devices that you are manufacturing. So in this module we will look at the issues related to test.

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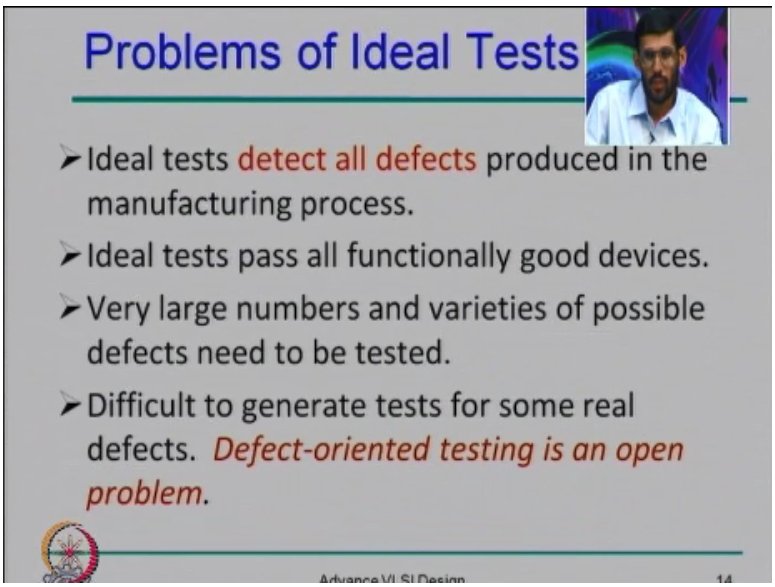

Now here first let us look at what are the problems with the ideal test. Ideal test is supposed to detect all possible defects that may occur during the manufacturing process. Ideal test wants that here all functionally good device should be passed and all functionally bad device should be rejected. So that means here you need to test for large number of possible defects and it is really very, very difficult process.

And defect oriented test is still an open problem some of you might work for your research interest to develop some defect oriented test. Methodology that may advance state of the art in test.

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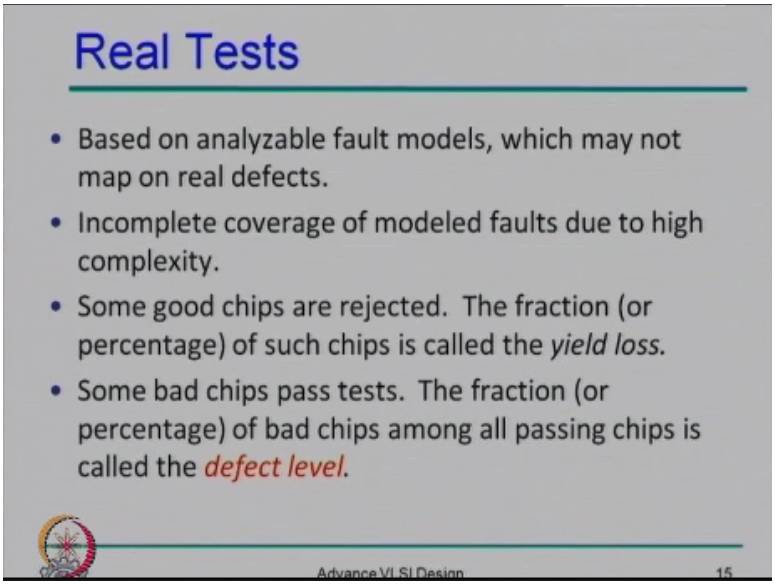

Then here look at the real test. Ideal test is supposed to detect all possible defect, but here defects maybe numerous. So some of the defects I listed in the beginning, but now here you cannot target all possible defect, but one thing is very clear all this defects will affect the functionality of device in one way or other. So that means here these defects may occur in terms of logical error.

So now here so we need to model the impact of that defect as an error at the output of the circuit and that model is referred as the fault model and now here fault model may or may not match all real defects sometimes, but here it is capable to detect by large number of defects because you cannot apply or you cannot target all possible defects here because of the high design complexities.

Here it is almost impossible to get 100% coverage for all model defaults and that is why we get the incomplete coverage and that is another thing which always bothers us always we want that at least we should test a chip for all possible modeled faults. Modeled faults are the faults which implicates in terms of logical error and now here I will come to this point little bit later, but here due to the bad design or test methodology here some of the good chip may be classified as bad chips.

And hence you are rejecting those chips this will lead to the yield loss. Hence it results in to the increase per chip cost and now here the other thing is we are applying very small subset of total test that we need to apply. Hence a fraction of chips may escape the test so that means here those chips maybe classified as good chips. Though they are faulty chips and this will

result into defect level.

So that means the fraction of bad chips among the total chip is known as defect level and every company wants to keep this as low as possible. The kind of DPPM people look at is something roughly 100 defective parts per million parts manufactured. Though here it depends on the application where you would like to use your chips.

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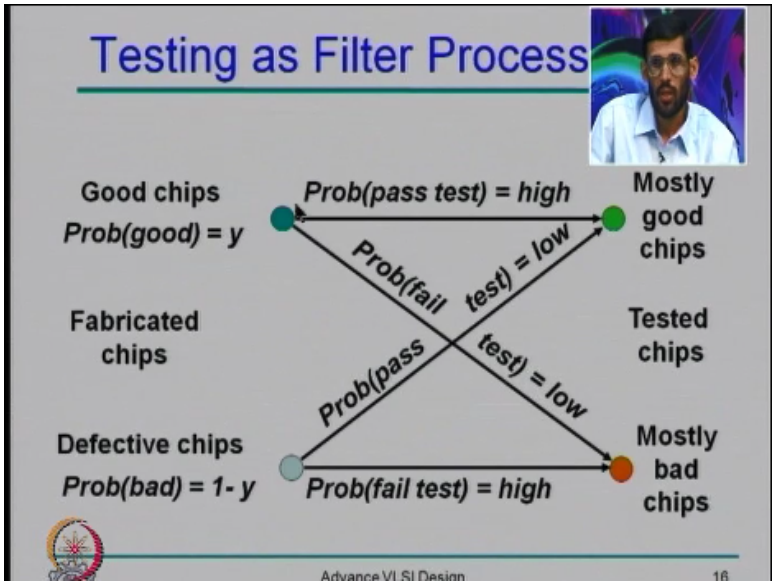

So the testing is something like filtering process. You have some good chips, some bad chips then here you want to test this and good chip should be classified as good chips, but some of the bad chips may also be classified as good chips. So this probability of classifying bad chip as good chip contributes to the defect level whereas we want that here all the bad chips or defective chip should be classified as bad chips.

But some of the good chips may also fail the test. I will come to this point why some of the good chip may fail because here we can no longer apply the functional test we have to work on the structural test and structural test does not care about the functionality. Some of the vectors that can be applied in the non functional mode that can uncover the defect, but those vectors can never be applied in functional mode.

Hence that fault may never be excited and hence that fault will not create any malfunctioning in the chip. So what we can say is that if we classify these good chips as bad chips we are losing those chips unnecessarily and that results into yield loss.

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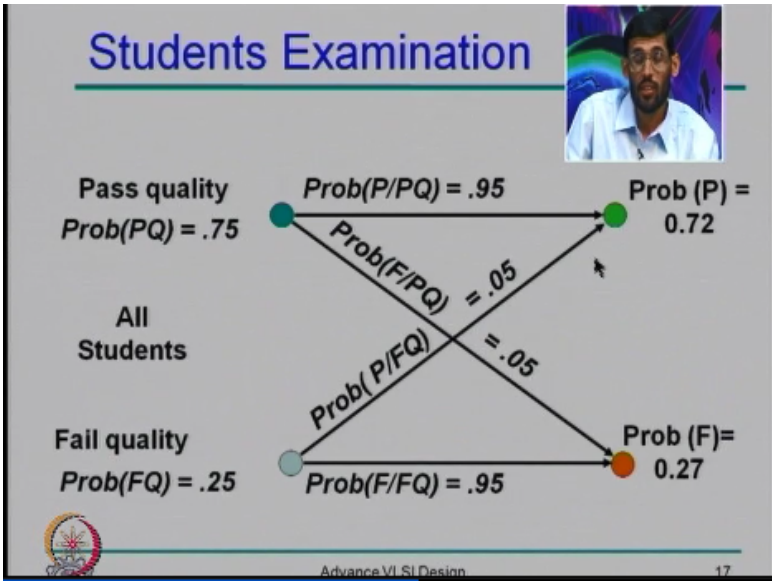

So this process is something like a student examination and all the faculty and students are struggling with this problem. So if I wanted to test how good you people are in learning the VLSI test. What I need in reality I want to create all possible questions and you are supposed to answer all those possible questions may be in 2 months, 3 months, 4 months, but nobody has that much time to test still here we want to test a student and want to award the grade.

We want to say that this student is pass quality student and this student is fail quality students, but by testing 3 hours' exam, for 1-hour exam. So that means here in 1 hours or 3 hours you can answer definite number of questions that is much smaller in comparison to the total number of impossible questions you may have for that course.

So now it is a big problem for the instructor to design a small set of questions that then give the similar kind of confidence to the instructor that he or she would have obtained by asking you all possible questions. So like, for example, in class there are say 100 students 75% students are pass quality students, 25% of students are either not sincere or not attending classes or this course may not be the priority for that. So they are fail quality students.

So now here ideally I want that here I want to classify these students as pass quality students these students as fail quality students I design a questions in order to design a question paper always every instructor use some kind of error model that these are the often errors students do make. And then you have to set a question paper that can uncover those errors.

So out of the 75% say the probability of passing the exam of say 95% that means here 95%

students will do write the right answers they will pass the exam whereas 5% students they were under stress or they might not have read that portion in the previous night and hence they are not able to answer the questions and then they may fail. And the similar lines like here out of 25%, 95% fail quality students will fail.

But some of the students maybe they might be smart they read only those questions previous night and they are able to solve those questions and they are able to solve the exam and hence they pass the exam. So out of 75%, 72% students will fail by the simple probabilistic calculation you can compute the probability of pass is 72% and probability of fail is 27%.

Now here this is very much concerned to the instructor that many of the fail quality students are passing the exam and this is much more concern to the students that here pass quality students are failing the exam. So here out of the 72% students if I look at the contribution.

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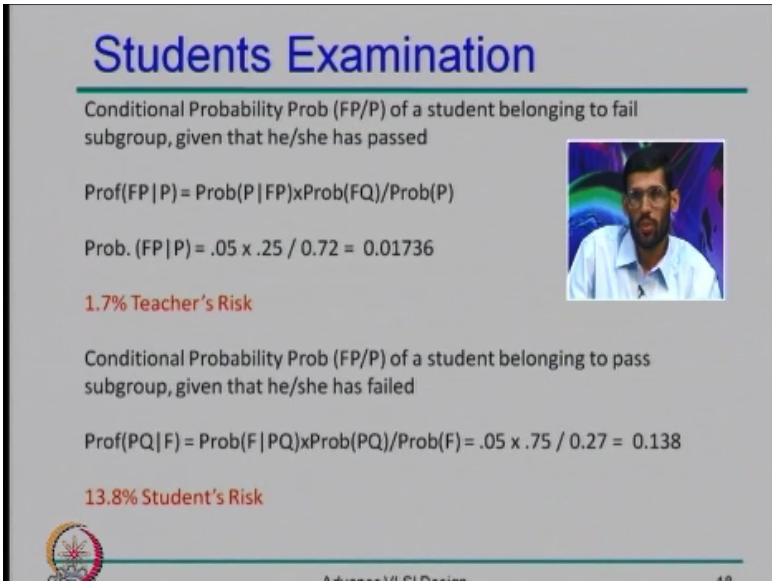

That how many fail quality students are passing the exam that you can compute by computing the conditional probability of students who belong to the fail subgroup, but then they have pass the exam. So now the probability can be computed as the probability of failing or passing the exam and to the total probability of the fail quality students divided by the total pass students and now here that comes out to be 1.7%.

This 1.7% is referred as teacher's risk because here these are the fail quality students who are passing the exam. You can reduce the teachers risk by making your question paper more tougher if you do that in that case some more pass quality students may fail. So then you have

to evaluate the other risk then compute the conditional probability of students who belong to pass class.

And then they have failed and that comes out to be 13% so that means here this is the risk of a student by having the harder exam. So now here we need to have a tradeoff between the teacher's risk and student risks. The things are very similar in VLSI test wherein the teachers risk corresponds to the consumer risk because they are likely to get that parts and students risk is corresponding to the foundry risk or companies corporate risk.

Now here you have to have tradeoff. There is little difference because in examination we give some benefit of doubts like here if students are solving more or less large number of problems correctly then we tell them pass quality students, but in VLSI test it means chip has to pass all the test. It is not like if it passes the 80% test it is classified as good test. So now here that is a little difference between the student examination and VLSI test.

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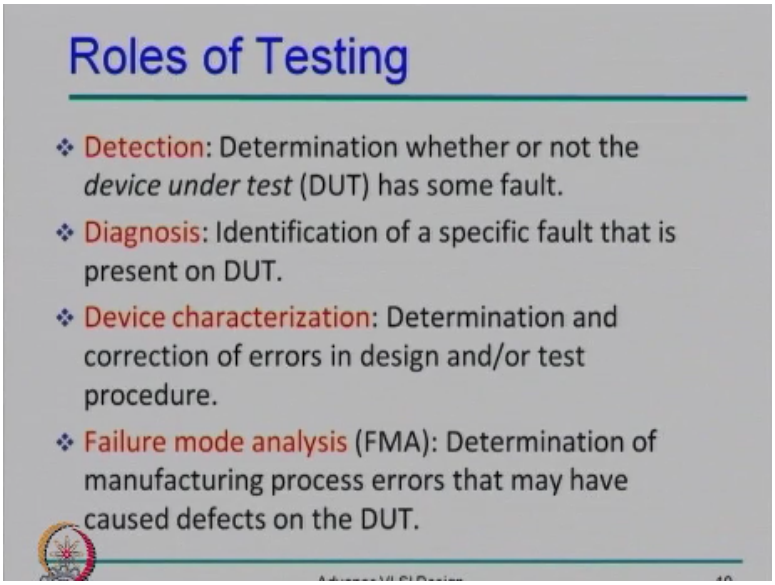

Now here look at what role VLSI testing plays. It has plays a role in detection of faults. It also plays a role in diagnosing the fault what kind of fault has occurred and if the fault occurs multiple times or in multiple chips then it is of concern and hence we have to look at why that fault is occurring often and that is known as failure mode analysis. So test also helps you in diagnosing and doing the failure mode analysis that what went wrong in the process while you were manufacturing the chip.

So that you are getting many chips faulty and you have to set the process right.

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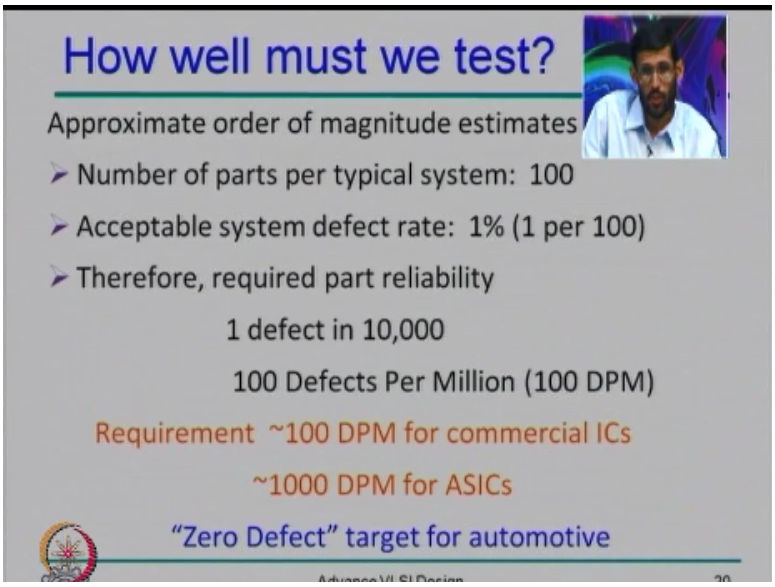

So now the question comes how well must we test a chip? It has direct relationship with the test cost and the quality of test because ideally we want that here quality should be as good as the exhaustive test is. Now here let us look at how well test a chip. Let say we have a system that has roughly say 100 chips those means these are reality nowadays. You have system with more than 100 chips as well and say now what kind of defect level you can accept.

Say one system out of 100. I assume I can accept as a defective so that means if it is defective I can send back to the company and then company may replace that. Though the cost is involved in that. If it is so then so that means if a system is defect free if all parts are defects free. So that means here if I say if I can accept 1% systems as defective that means one chip out of 10,000 can be defective.

That results into like 100 defective parts or chips per million chips that we are producing that means here if I accept the 1% defect rate here my defective parts per million requirements is roughly 100. So for almost all the commercial chips 100 DPPM defective parts per million is admissible whereas for some of the applications like mode automotive applications they do not want any defective parts.

So they ask for zero defects. Zero defects is almost impossible to get, but here the DPPM must be very, very low that must be very, very close to zero because nobody accept a chip that goes in breaking system of a car and you say that there is a definite possibility that this chip will fail and so nobody wants to buy that kind of car. So hence they have very strict

requirement for quality of the chips.

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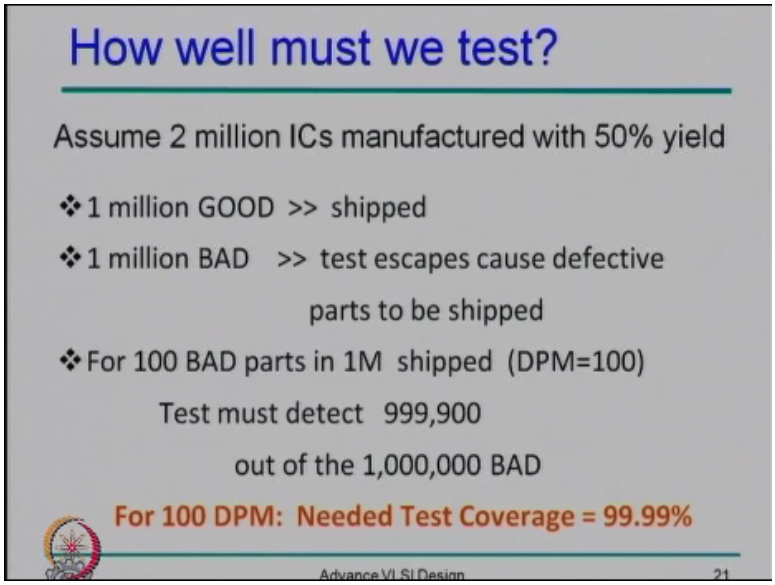

So here let us assume I produce 2 million chips and my manufacturing yield is 50% that means 50% chips are good, 50% chips are bad which is very close to today's manufactured chip though here based on the immature or mature process quality varies. So the yield may go as high as 80%, 85% that may go as low as 20%. Now here say I have reasonably good yield 50% so that means one million chips are good which we want to ship another million chips are bad which you want to reject.

Now here out of one million bad chips if I say that my DPPM is 100 that means here 100 bad chips may be shipped. So that means here 9,99,900 chips must be detected as bad (()) (36:47). So now here if I look at the test coverage this should be 99.99% that is the kind of requirement we have if we have 100 DPPM requirement this goes further high if the DPPM requirement is < 100 or if the DPPM requirement is relaxing it can be further enhanced.

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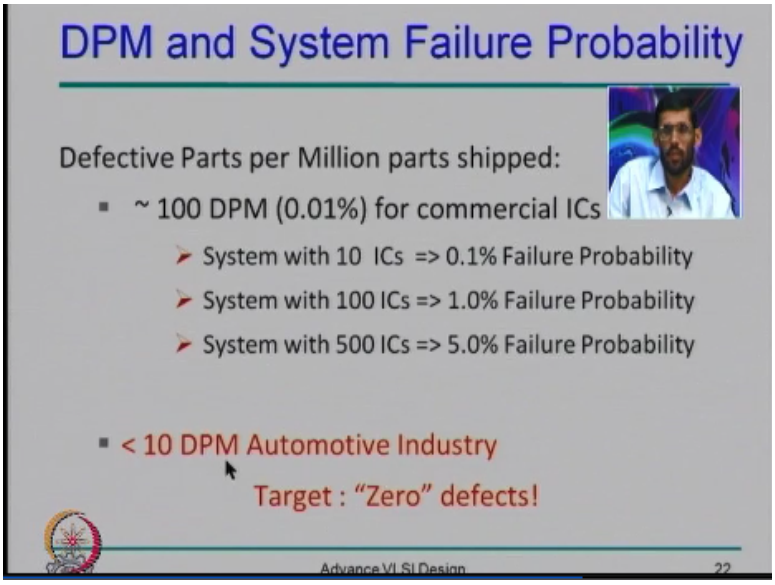

Now if you say that 100 DPM in that case chip with the 100 ICs may have 100% failure 1.1% failure probability chips with 100 parts maybe 1% chips with 500 ICs this may have 5% failure probability. Now here for like automotive industry I say they are targeting for zero defects, but they really look for less than 10 defective parts per million parts.

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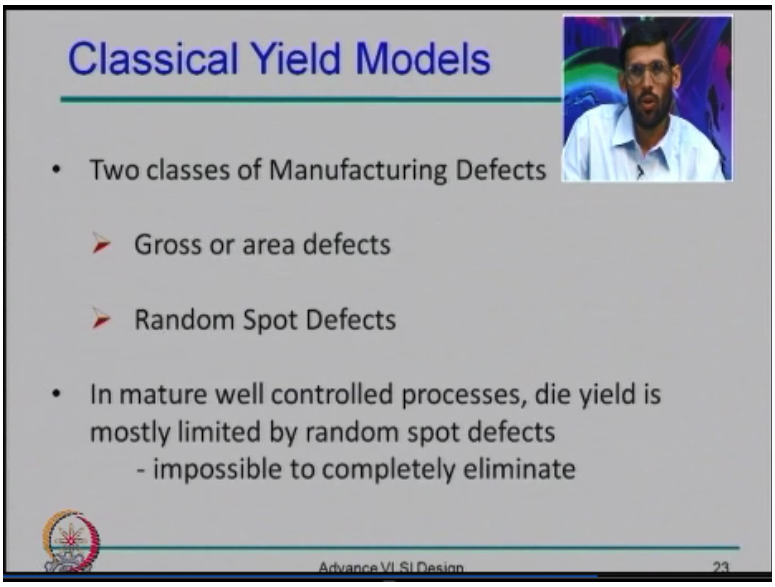

So now here look at the yield model why we have 50% or 70% yield that comes from the manufacturing defects and the defects maybe the gross or area defect that we may have that maybe a systematic defect of the process or that may be random defect. So mature well controlled process die yield is mostly limited by the random spot defects it not by the systematic defect that may appear due to the systematic process defect or the material defect, but here now the elimination of random defect is almost impossible.

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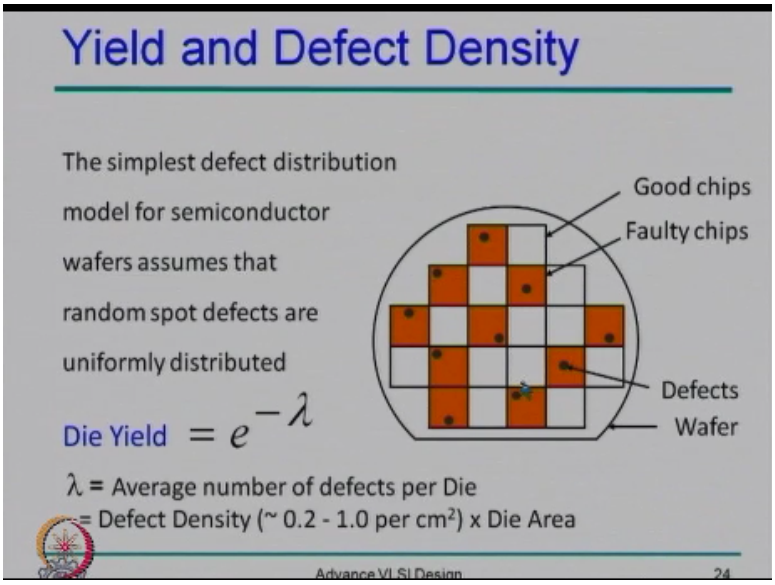

If I look at the chip say here this chip has many of the die. Some of the die are effective some of the die are good die. So these die are the defective die why die are the good die and now here say in this chip if I say I have 10 defects out of 22 die and these defects are randomly distributed all through the area in that case these 10 defects may spoil 10 different die and so we have to reject those die.

So this yield model can be captured by simple Poisson model that gives you the die yield Poisson process and that e raise to the power - lambda where lambda is the average number of defects that may occur per die and that number of defects is equal to the defects density and die areas. Defects densities are somewhere between 0.221 per centimeter square if you look at the manufacture device right from 60s or 70s this defect density stays more or less same.

So that means here if you have bigger area then you are likely to have more defects and so if these are pure randomly distributed you are likely to spoil more number of chips.

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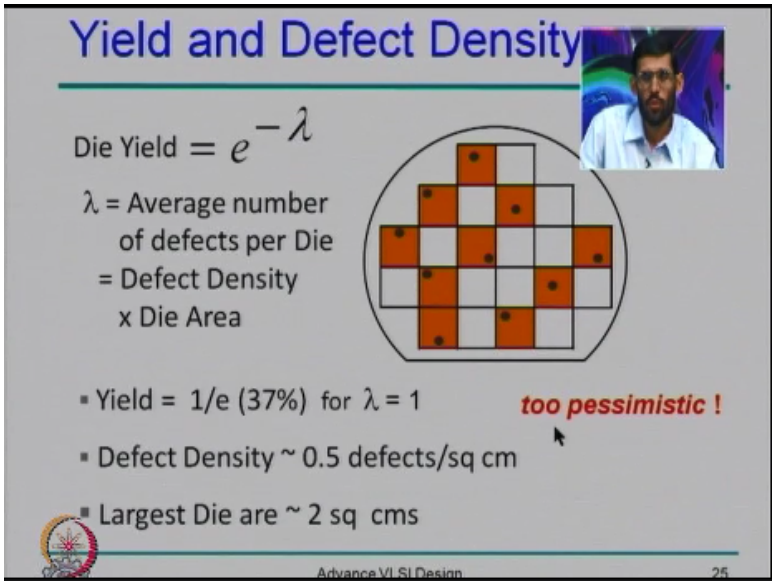

And if I say look at the pure random distribution assuming that there are .5 defects per square centimeter and die area is say roughly 2 square centimeter that means the average number of defects would be equal to one and hence the yield would be 37%. It looks too pessimistic so that means here 37% die are good means remaining die are bad and you have to throw those die.

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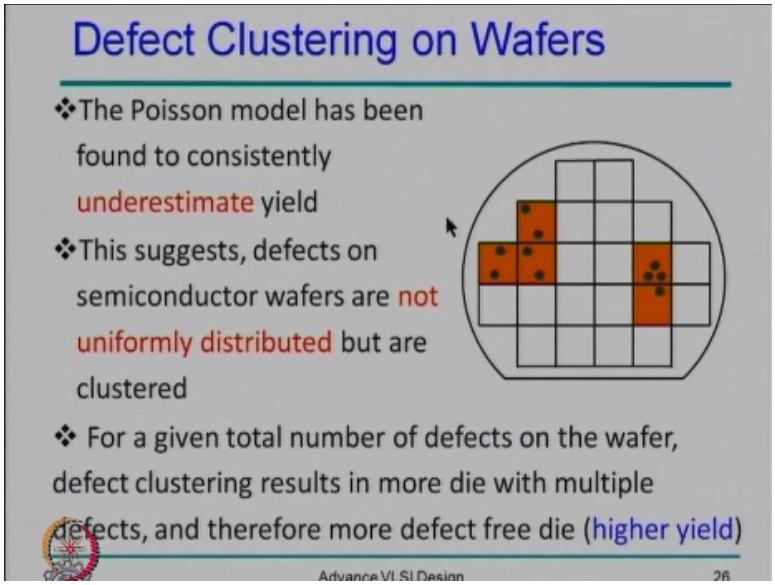

Though here in reality the Poisson model does not capture the clustering phenomena and the defects. So all the defects are really not identically distributed everywhere so are uniformly distributed everywhere. They are clustered and then the clustering density depends on process to process. Now here you can configure out the clustering density of a process and based on that here you can compute the yield, but here definitely when the defects are clustered they will spoil less number of die hence the yield would be higher.

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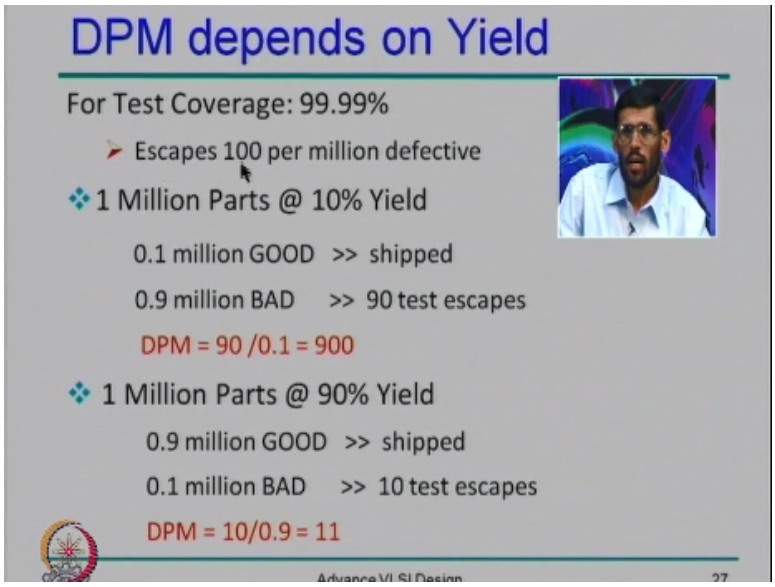

So now here if you look at the like we were talking about 99.99% coverage and now here we are okay with 100 DPPM so defective parts per million. So that means 100 defect parts per million may escape the test. Hence now assume you have million parts and your yield is 100% in that case your.1 million parts are so one lakh parts are good those we are shipping, but the 9 lakh or .9 million points are bad.

So that means here out of .9 million the 90 parts may escape the test. So now here 90 parts may escape the test that means here the total DPPM will go as high as 900. So this gives you the correlation between your fault coverage, your yield and the DPPM. So that means here you need very high fault coverage for this if you want to bring down the DPPM. Assume that another process is matured and you have 90% yield out of that.

So like here 9 lakh parts are good they are shipped and one lakh parts are bad. So that means they may have only 10 test escapes. So 10 test escapes will give you only 11 defective parts per million parts that is pretty low. So that means here what it tells us is the biggest challenge is for the complex system and which have low yield. If you have high yield you are really not very much worried about the test coverage even the lower coverage may give you the very low DPPM.

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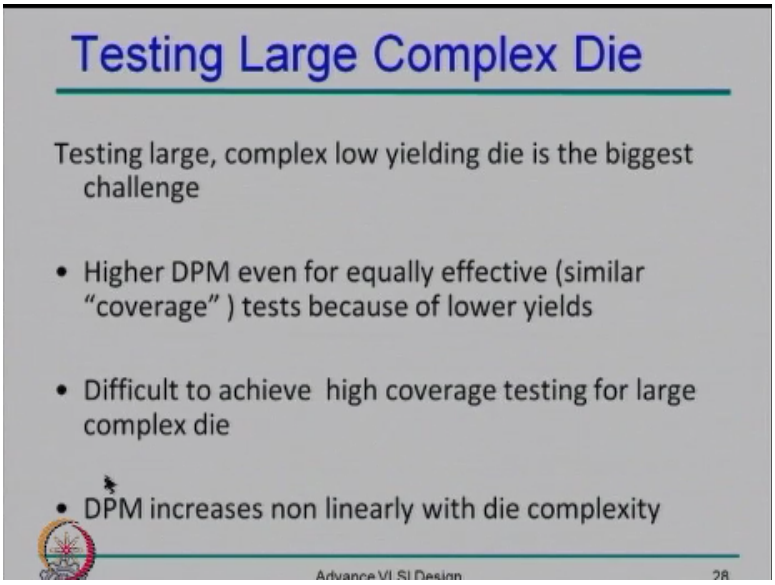

So it is the low yield die which are of big concern other thing is because of the complexity it is very difficult to achieve very high coverage and defective parts per million. This is not linearly increasing with the complexity. Complexity means the number of off grades that you have, but it increases non linearly with the complexities that another concern.

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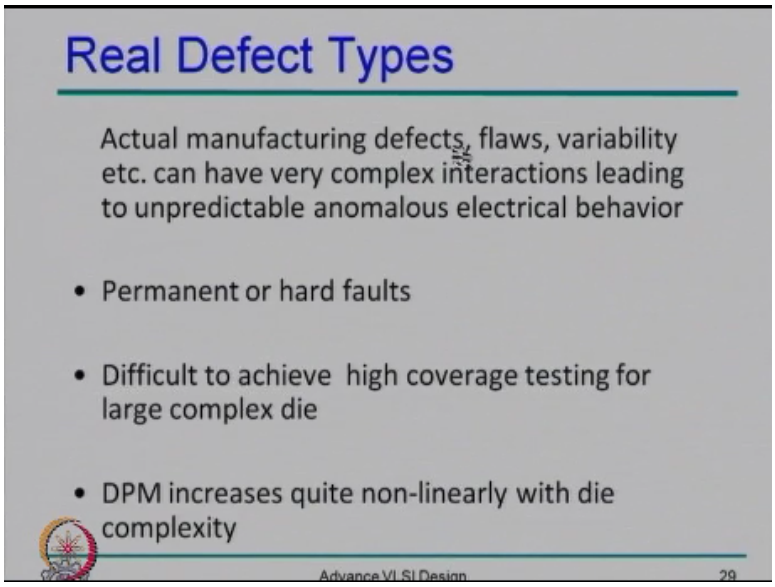

So now here were if you look at the manufacturing defect that may come from the flaw in the defect, flaw in the process. Now the variability is again becoming increasingly important as the variability is more in terms of channel length or say of the gate here its speed varies with that and hence some of the devices may not have logical fault, but they may have timing faults. So these faults are either permanent faults or hard faults or some of the faults are also transient because the devices are becoming weak and weak.

And hence like if some environment radiation strives on that device it may produce a glitch and that glitch may continue to stranger the system and that gives you the wrong output. So those are the kind of transient fault we have.

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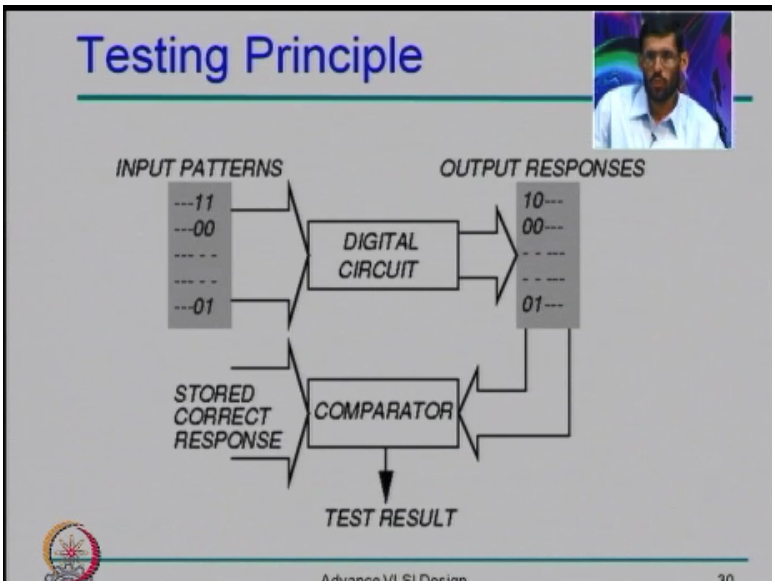

Now if you look at the test. Now you have produced circuit then you want to apply couple of inputs or patterns that you have developed during your test development procedure. So this is a small set of factors what you will do using very expensive tester you apply the test. You collect the test response and that response should be compared with the golden response that you obtain through the simulation and if there is a match you say the device is good and you ship it fails then you have to reject that device.

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So in order to apply the test here we use some expensive devices like Advantest this ATE is

one of them and these are really expensive devices.

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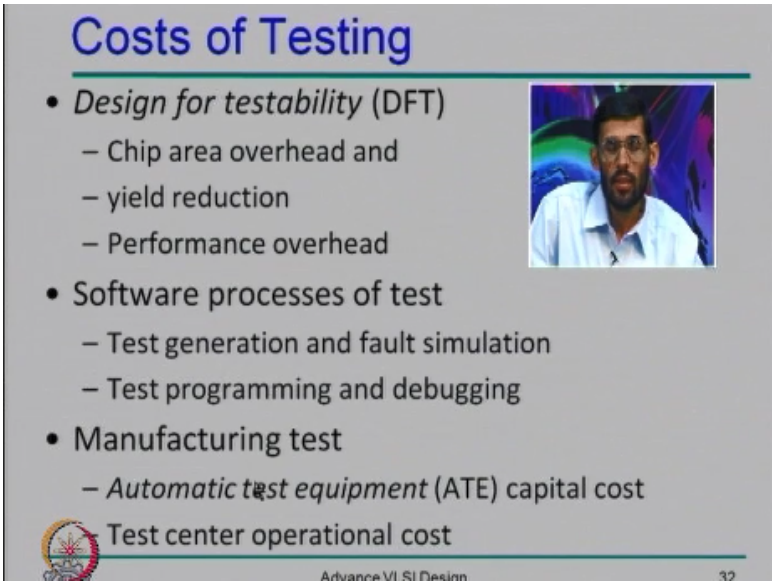

So now here if you look at the various cost involved with this process those costs are like design cost that we have. This yield to the like all the chips are not very suitable or to develop a very compact test set. If they are not, then we have to have augmentation in the design and that augmentation comes in terms of extra area that we need. If the area increases again here yield decreases and then with the augmentation of design it comes with the performance penalty as well.

So that is the design effort that we need to put. So this comes as recurring cost. Another cost of course I explained you earlier is the test development cost that purely the software process. So you have to develop a small test set and then you have to buy expensive test equipment that is capable to apply the test, collect the test response, compare the golden response with the golden reference and give you the flag whether it is good chip or bad chip.

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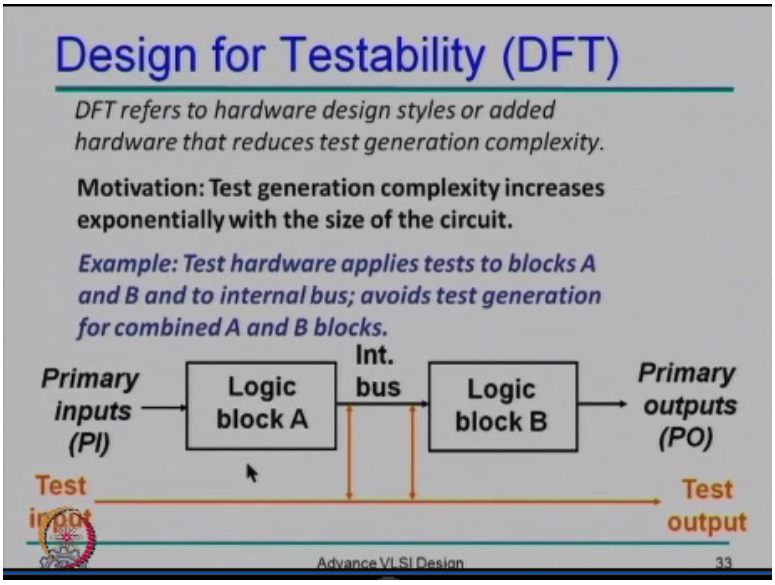

So like here this slide tells you that here if the output produced by this logical block A goes through the logical block B that is not easy to observe. So what you can do is you can have one additional bus that can take output from this logical block A and you can simply see observe the output from here which was otherwise very difficult to observe through the logical block P and hence this is the additional cost that is typically referred as design for testability.

I will come to this point what are the other design for testability techniques we have.

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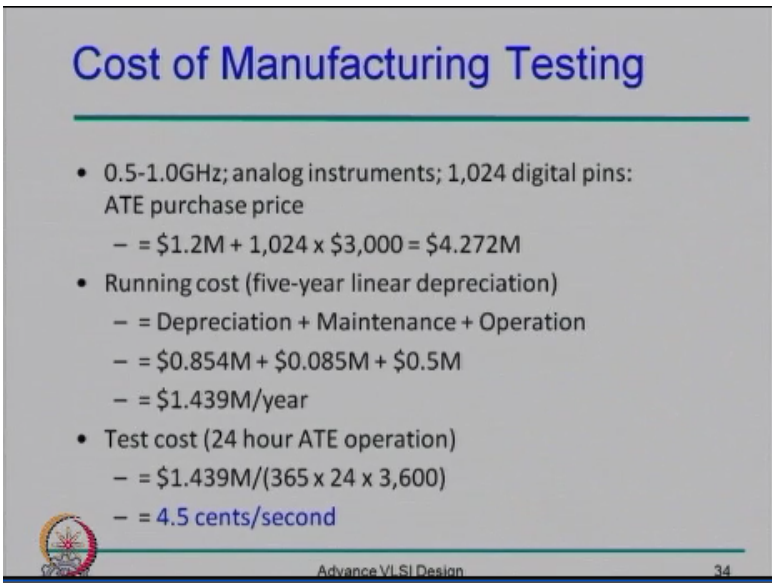

The other cost is the manufacturing test say here you buy a test equipment that may operate at one gigahertz these data are pretty old maybe 10 years old. So you buy a tester that I have shown you earlier say it was 1024 pins and say the base actually cost is 1.2 million and then

3000 dollars per pin it cost me then it is roughly about 4 million dollars it cost. Now here when you operate this and say that I will continue to operate this tester for next 5 years after that anyway this tester would be too slow and it would be obsolete.

Now I have to depreciate this over 5 years and say that 20% depreciation. So about a million-dollar point at 5 million dollars is the depreciation cost per year then the maintenance cost maybe we say that 2% cost is the maintenance of the equipment and then some operational cost like manpower and say like AC cost and building cost and all these things. So now here if you divide this cost per year then it something like 1.4 million dollars per year.

If you distribute this per second in that case here this comes out to be roughly 4.5 cents per second. If you operate this 24 hours a day a 7 days in a week. So now here I assume that roughly it cost you 5 cents per second that is just the test equipment cost and now here if you say you want to test your device for a minute say this cost is roughly 5 cents then it cost you about 3 dollars per minute.

If you test your chip for an hour it costs you about 180 dollars per hour that is what Prof. Chandorkar mentioned you earlier that it cost you about 200 dollars per hour. So these are the major cost those are involved in that. So that makes it a difficult process.

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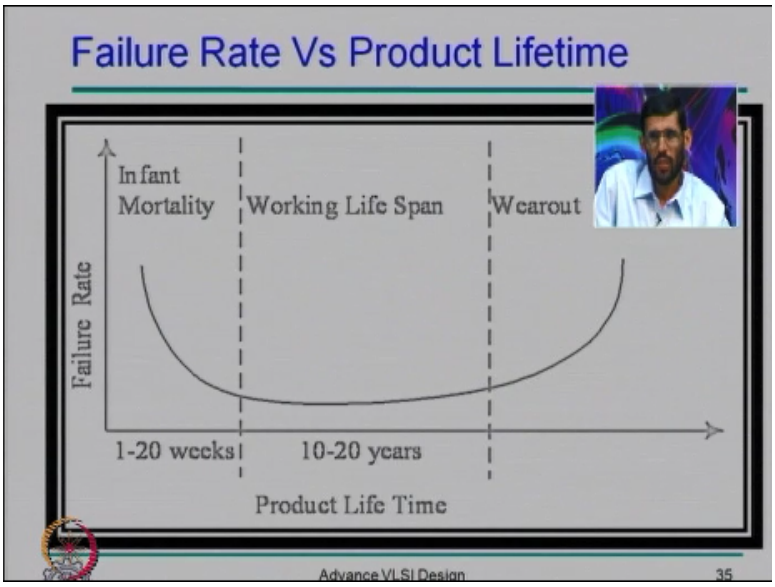

Now one more thing at the end I would like to mention in the test challenges that like when you manufacture a device based on the yield couple of devices are good, couples of devices are bad. So out of the devices which are good couple of devices are weak devices they are

likely to fail in initial couple of months like here for example if you have very weak contact or very weak line.

And now here when chip operates then due to electromigration that line may become completely open after a while and hence that chip will fail. So this phase is known as infant mortality and that happens in first few weeks and after that device operates fairly well for next couple of years and after that aging starts to appear in the picture and due to various aging effects.

NBTI is one of the dominant effects nowadays and then here device starts to fail to operate at the rated frequency or it may completely fail. So now we need to care two more things. First thing is we have to wearout all the bad parts just after manufacturing, but then during the testing we also have to make sure that these weak devices should also fail so that here they may not fail in the field just after they start to operate.

So now for that you need to provide some accelerated conditions so that these devices may see that kind of aging effecting right after the manufacturing and so we generally test these devices at accelerated voltage, accelerated temperature. So the temperature is something like here about say 125 to 130 degree centigrade whereas the voltage roughly we raise to 40% to 50% of the denominal VDD that we have.

So these are the infant mortality we should make sure that this happens right after the manufacturing other thing so after that here whatever devices which passes the test they will work fairly well for couple of years and then here we have to have some mechanism to detect the fault if it occurs while it is in the manufacturing if the life time that we are looking for is long enough like for this express applications you cannot replace device every years.

So they have to have lifespan of 15 to 20 years so that means here you have to have some mechanism that may detect the defect that may occur and then you can test that. So conclusion here I try to motivate you why VLSI design is VLSI test is very important in the VLSI design flow, why you need to study this topic as well with the advanced VLSI design course and what are the various challenges we face for the VLSI test and at what level we need to take care of various issues.

With this, I summarize this lecture, have a good day. We will meet again with the next lecture wherein we will discuss about the various test fault models, test techniques so good-bye. Thank you very much.