Advanced VLSI Design
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Lecture - 15
Interconnect Aware Design - Low Swing and Current Mode Signaling

In the last lecture, we had looked at the fundamental problem of the delays introduced by long interconnect. We had seen that while scaling, improves the speed of active electronic circuitry. The interconnects in case of local interconnects retain their old speed, whereas long interconnects actually become much slower. This puts an inherent limitation on the maximum speed at which the system can operate.

We had looked at the existing methods of improving interconnect speed in case of long wires and buffer insertion is the dominant technique which is used for this. However, buffer insertion is far from perfect. It takes power, it makes the line unidirectional and ways of making the line bidirectional are not easy. In order to reduce the total amount of power consumed by the long interconnect.

We had looked at low swing signaling, low swing signaling and voltage mode is already in use. Essentially what it means is that over the bus, we do not use the same zero and one levels as we do in the main logic. When the signal is to be conveyed over long wires, the line swings by a small amount of swing. This reduces the dynamic power considerably. At the receiving end, we have an amplifier and this amplifier will then restore the logic levels so that the rest of the logic does not know the difference.

This technique is quite successful and we had seen a variant of this which is called the current mode logic. The current mode logic differs from the voltage mode logic because it terminates the line in a low impedance. We had also seen an Active circuit which can be used for producing a very low and controllable input impedance. There are many other ways as well for loading the line with a low impedance so that it operates in the current mode.

The current mode essentially makes the impedance of the line low and therefore it is able to charge and discharge capacitors to the small voltage levels much faster. As a result, it has inherent advantages over the voltage mode of signaling. Having established that there is a lot of promise in low swing signaling over the traditional buffer inserted lines, we now see how we can optimize this mode of signaling so that we can get the best possible performance from this.

One of the methods for this we had briefly discussed yesterday, we shall take it up again in detail today and that is called inductive termination. There are 2 other methods also which we shall see today and then see what are the kind of optimizations which are possibly in this technique. Let us look at the basic current mode signaling technique.

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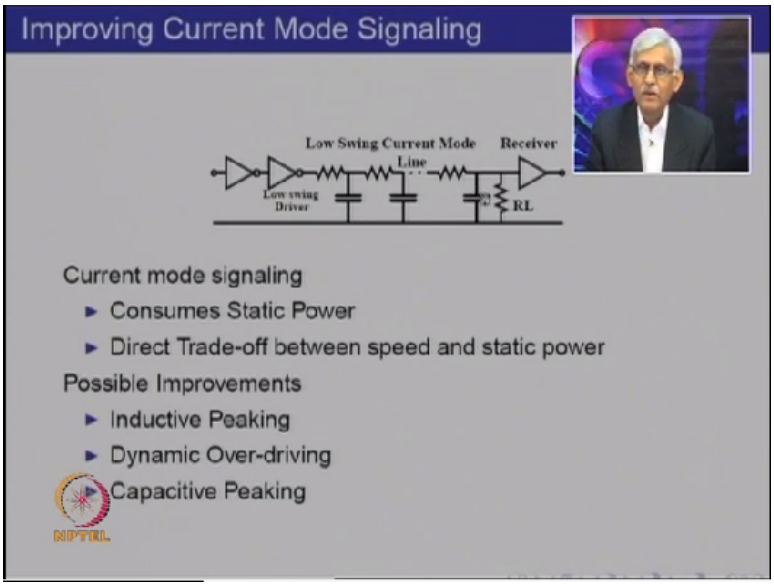

We need special drivers which are called low swing drivers. These ensure that the voltage at the line does not go from rail to rail but swings around a small common mode voltage here. This small swing is then conveyed here and terminated into this load resistance. Notice that the common mode voltage means that there is a steady current flowing through this and therefore there is static power consumption.

This small fluctuation at this point is then amplified by this receiver to a level where the output now again swings from rail to rail. So this is the basic model of the current mode signaling which we have been discussing and now we want to see what are the possible improvements which are

possible. Notice that this wire is an RC line and therefore has a low pass characteristic. It will therefore selectively attenuate high-frequency components of the signal.

And therefore distort the wave shift. When we want to carry out very high-speed communication over these lines then we need to worry about this low pass nature and we are always looking for ways which will improve the bandwidth of this length. There are various ways which have been suggested in the literature for this. There are 3 dominant ways which we shall discuss. One of them is called inductive peaking.

The idea is that rather than terminating the line in a pure resistance, we terminate it in a load which has an inductive component. Because of this, the termination now has a high pass characteristic which to some extent mitigates the low pass characteristic of the line, as a result we can enhance the bandwidth and get higher speed transmission on the same infrastructure. I will just mention two other techniques here.

We shall see the details of these when we come to it. Both of these techniques do the correction at the transmitter end rather than at the receiver end. At the transmitter end, in dynamic overdriving, what happens is that whenever there is a transition on the signal that means it is not resting steady at 1 or 0, then you employ additional drive and this additional drive enhances the high-frequency components because it is used only during transitions.

That then combats the attenuation of high-frequency signals down the line. Capacity of peaking is a very simple implementation of dynamic overdriving and it essentially puts a series capacitor in series with the line here and that has a high pass characteristic and that can compensate to some extent the low pass behavior of this line. There are side effects to this which we will worry about.

But we shall come to these details when we look at these two techniques a little later in this lecture. But to begin with, let us look at inductive peaking.

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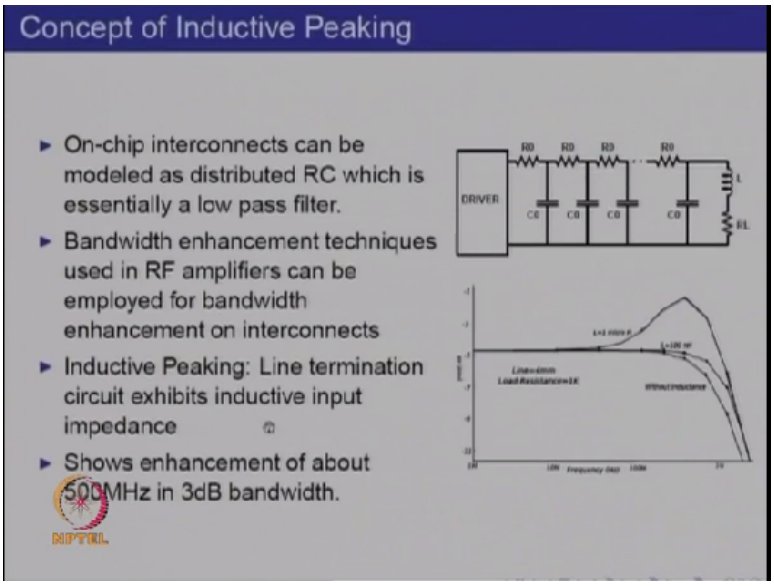

We had seen this in the last lecture and we will quickly go over this again. Essentially the termination that we had seen here now has an inductive component and using ideal components, first we find out what is the effect of placing this inductance here. We will worry later on how to implement this inductance. These three curves correspond to no inductance. This lower curve putting hundred nanohenries which is this middle curve and putting a microhenry is this last curve.

I would like to remind you again that these curves are on a log scale and therefore this small extension of the bandwidth is not negligible. In fact, you can increase the bandwidth at the 3dB point by about 500 MHz in this. From this, it appears, by the way the values of R and C have been taken from current technologies and it is of the order of tens to hundreds of ohms per unit length here and centro ferrets for the capacitor.

Using those values of R and C, we find that typically we are looking for inductances which are in the range of let us say hundred nanohenries. Now a 100 nanohenry inductor is not easy to put on chip. If you were to make a coil whose inductance is 100 nanohenry, it will actually consume just too much area to be practical. Therefore, we need to look at electronic implementations which will give us the equivalent of this kind of termination.

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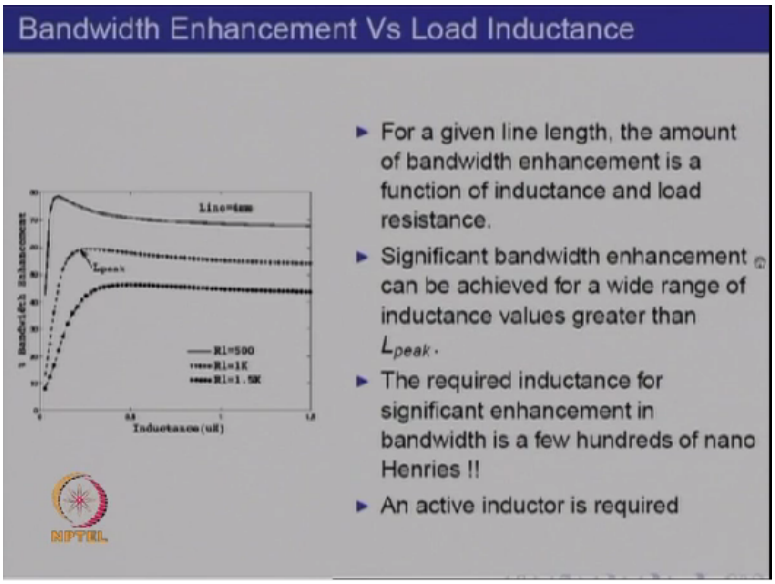

The amount of inductance that we need also depends on the line length. So here we have taken a 4 millimeter line and these three curves correspond to different values of the terminating resistance and these are 500 ohms, 1K and 1.5K. We now choose various values of inductance and see the effect this amount of inductance will have on the bandwidth.

So you notice that essentially these curves for a side choice of resistors, actually peak at a value of inductance which is of the order of hundred or a few hundreds of nanohenries and once you choose that value, this value will remain optimum or close to optimum whatever be the termination resistance. Therefore, in short, irrespective of the terminating resistance that we actually use.

We somehow require inductors of a few hundred nano henries and clearly passive inductors of this value are not practical and we therefore look for active inductors which will provide this much of inductance.

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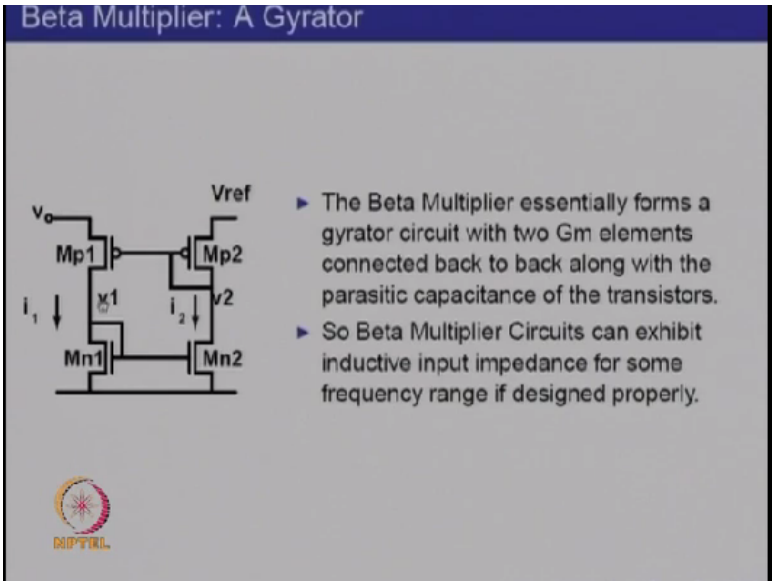

In fact, the beta multiplier circuit which we had seen as the termination resistor earlier itself can provide inductive component if it is properly designed. The reason for this is that the beta multiplier essentially forms a gyrator circuit which has two Gm elements connected back to back. So these two have positive feedback and they are connected back to back.

When you have two Gm elements connected back to back, they do have the capability of converting a capacitor into an inductor and therefore a basic beta multiplier circuit which we were anyway going to use as an inductor in case of current mode, can exhibit inductive input impedance for some frequency range if properly designed. So our next task becomes how to design the beta multiplier.

So that we will have a substantial and a required inductance which should be in the order of hundreds of nanohenries.

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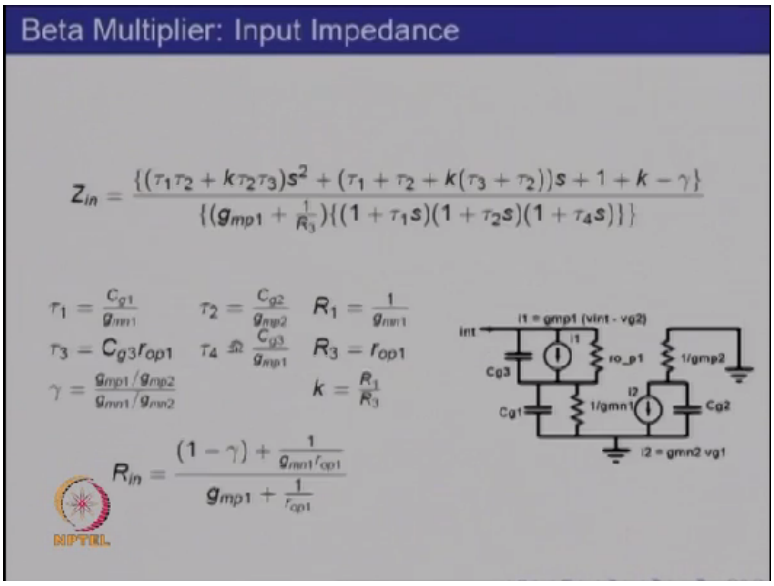

We can actually put up an equivalent circuit for the beta multiplier. These are essentially the two active parts of this and the active circuit can be represented with this with the two gate capacitances Cg1 and Cg3 coming here and Cg2 coming here and this is the Gmp2 of transistor 2. Just to refresh your memories, this is Mp1 and Mn1 and Mp2 and Mn2, these are referred to as 1, 2, 3 and 4 in this circuit.

So this is Mn1 and this is the capacitance across that and these capacitors play an important role in determining the equivalent inductance. This network is a little tedious to solve but it can be solved given enough patience and we have in fact done this and eventually you get the input impedance of this at this point where we connect the interconnect.

The total input impedance is given by this somewhat longer expression. The component of this expression involve various time constants and that old Gamma factor that we had define which is a ratio of ratios here. So we have essentially Gm by C behavior here, so the time constants are the C by Gm's of various components here. This is for transistor 2, this is transistor 3, this is transistor 1.

The various resistors are the one by Gm's or the output resistances of various transistors and then we have defined 2 additional parameters, the k is R1 by R3 which is essentially this divider and Gamma which is that ratio of ratios which makes the beta multiplier so robust. Notice that when

we had done the earlier analysis. We had ignored the output resistance of all the current mirrors and as a result, these two terms were missing and the effective input resistance that we had got at that time was one minus Gamma upon one by Gmp1 into one by Gmp1.

Now we have made a more careful analysis compared to the previous one and included the output resistances of all the current sources and when we do that then this is the equivalent circuit we get, this is the input impedance we get and once we define these intermediate values, this can be put down in terms of these.

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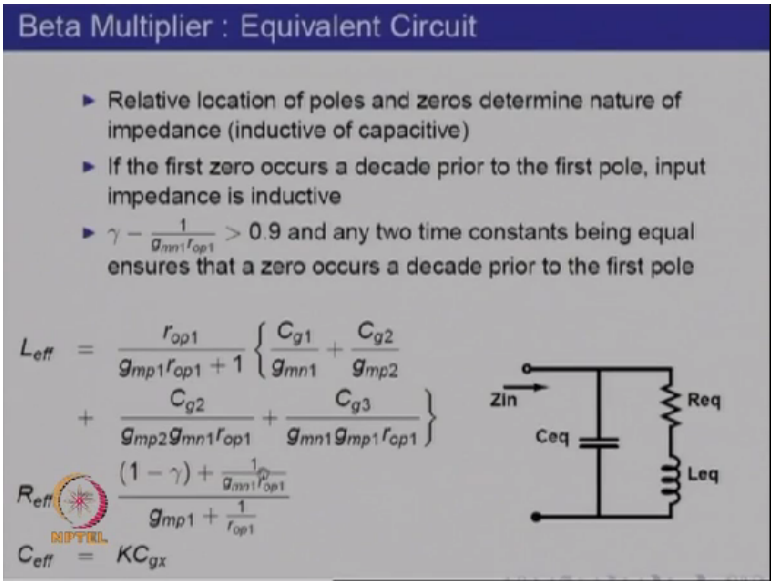

Now this has various poles and zeros and the relative location of poles and zeros determine the nature of the impedance which can be inductive or capacitive. If the first zero occurs a decade prior to the first pole, then the input impedance is indeed inductive. This means that this term Gamma minus 1 upon Gmn1 into R output 1 should be greater than 0.9 and if any two time constants are equal, that will ensure that a zero occurs a decade or so prior to the first pole.

This gives us the design equation. Once we do that, then we can further simplify the input impedance equation and the effective L comes out this value. It also has a resistive component and a capacitive component and the actual equivalent circuit is given by this where we have this R equivalent, L equivalent and C equivalent. Recall that what we want is only the R equivalent and L equivalent.

But our advantage is that the C equivalent comes in parallel with the line capacitance. The line capacitance is in any case large and therefore even though we did not want it and got this capacitance, this capacitance will not make too much difference. In short, by proper design of a beta multiplier, we can get a circuit which terminates this RC line so that this C becomes part of that line RC and which terminates this line.

Therefore, in the kind of configuration which we originally wanted and this will then compensate for the low pass filter of the line all the way up to this point.

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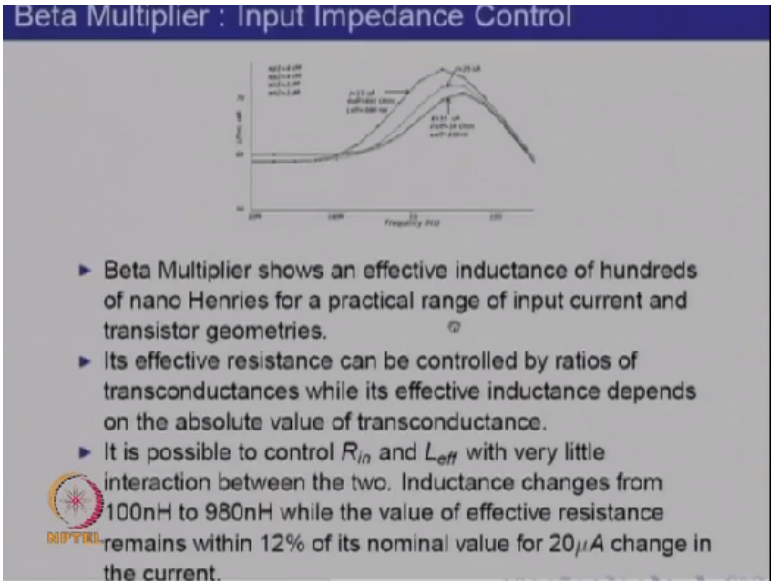

Obviously, these terms will then become frequency dependent and we are interested in a frequency range which corresponds to our data rate and which is of the order of gigabits per second and essentially that is this decade. This is one giga, this is 10. So essentially we are interested in this range and this is the Z and this peaking that you see, is the inductive peaking and the inductive peaking depends on the amount of current that we give to the transistors which in turn determines their Gm and as we have seen before.

The Gm determines the impedance of these circuits. So we can summarize that algebra as saying that the beta multiplier shows an effective inductance of hundreds of nanohenries for a practical range of input current and transistor geometries. These currents are not too shocking. They are

like of the order of 25 microohms to 35 micro ohms.

So it will not cause too much power consumption and by using appropriate geometries and currents of the order of tens of microamperes in the range of 30 microamp. We can indeed get the amount of inductance that we need in order to improve the bandwidth. It is also possible to control the input resistance and the effective L with very little interaction between the two and the inductance changes from about 100 nanohenry to 980 nanohenries.

While the effective resistance remains within 12% of its nominal value for a 20 microamp change in the base current. So this gives us a very good handle on getting the inductance that we need. This is indeed the range of inductances which we want without changing the terminating resistance too much.

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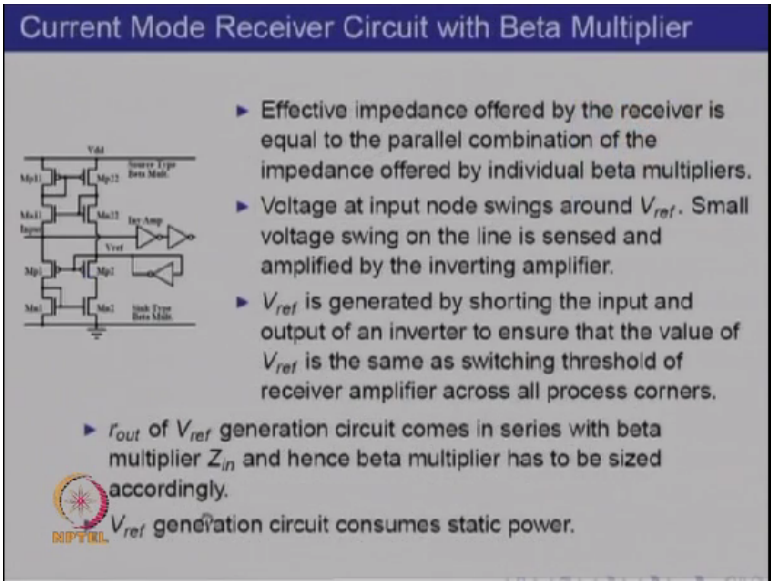

Once we have done that, we can actually come with the actual design. Notice that we are using actually two beta multipliers, one for positive going in coefficients, the other for negative going in coefficients. This shorted inverter essentially provides the reference voltage at which this line will be maintained by the beta multiplier. So this provides the DC reference for these beta multipliers and indeed for the line voltage.

So this line will be maintained at a common mode voltage which is determined by this reference

voltage generated by this shorted inverter. The output then is amplified by these inverting amplifiers and the low swing voltage at this point will then be converted to a rail to rail signal here. Notice that apart from the power generation in this circuit, this shorted inverter also will consume static power and the Vref generation circuit.

It does consume static power; however, when we report various performance parameters of this, we will include the power consumed by this and this circuit in the driver power that we claim.

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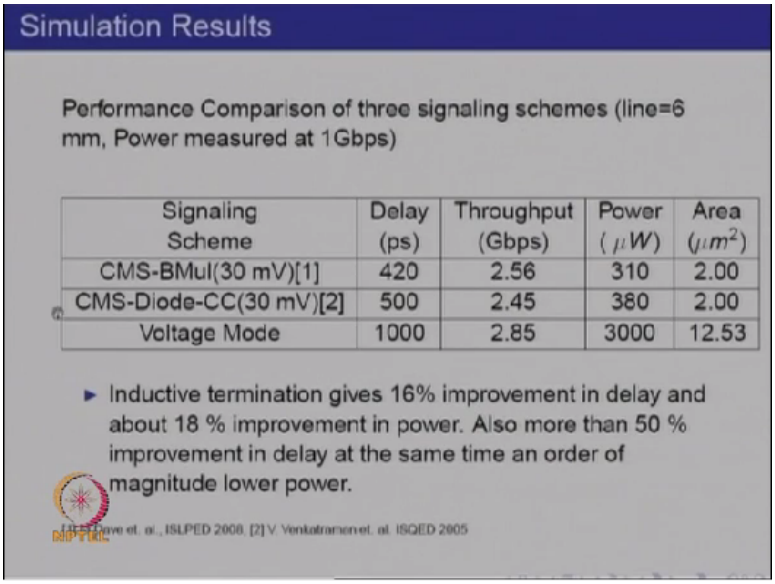

So here we present a comparison of three cases. One is the buffer inserted voltage mode, the other is the beta multiplier termination and third if we just had a diode connected current mode system, that means the terminating resistance is just provided by diode connected transistors. These are taken from these references and reference one is in fact our own work. As you can see the voltage mode has a very large delay, about thousand picoseconds.

Just going to the plain current mode reduces this delay to about 500 picoseconds. This is a plain classical current mode line in which the termination resistance is provided by a diode connected MOS transistor. And finally the delay of the beta multiplier case is 420 picoseconds. The throughput actually goes in the opposite direction. The throughput of the diode converted case, the diode terminated case is the lowest at 2.45 gigabits per second.

The throughput of the scheme with the beta multiplier which we have suggested, comes out marginally higher than this, it is about 2.56 gigabits per second. The voltage mode is actually capable of very high throughput. The throughput possible in this case is 2.85 gigabits per second but this comes at the cost of immensely high values of power, that means it will require 3000 microwatts of power in order to get this throughput.

The power consumed in case of the two current mode options, one with the diode termination, the other with the beta multiplier termination is much smaller. It is between 300 to 400 microwatts. The diode termination circuit takes 380 microwatts and the use of the beta multiplier actually reduces the power to 310 microwatts. So there is almost an order of magnitude of power between this and should we want to match the throughput offered by this voltage mode.

It should be possible using the beta multiplier configuration also. However, in that case the power will go up slightly. It will still remain much lower than the 3000 microwatts required by the voltage mode option. The area also shows much better figures here. The two current mode circuits consume hardly any area. Remember no buffers are required down the line, where as the voltage mode requires buffer insertion along this line.

The line is 6 mm long and many, many buffers will have to be inserted and therefore the silicon area taken up by that is quite considerable, it is about a factor of 6.5 higher than the area taken by the current mode. So in short, inductive terminations gives 16% improvement in delay and about 18% improvement in power and this is compared to the ordinary current mode. Also more than 50% improvement in delay at the same time, an order of magnitude lower power compared to the voltage mode.

Having looked at inductive termination, we now look at other techniques of improving the current mode transmission and one of these is that of dynamic overdriving or pre-emphasis. After all we have a low pass line and what we are looking for is a high pass characteristic in order to combat the attenuation of high-frequency signals by the line. One possible way was what we have seen that is inductive termination but now we look at yet another way which has been suggested.

Now if a line is sitting steady at 1 or 0, obviously the signal has very little high-frequency component. High-frequency components come in because the lines switches is at a high rate from 0 to 1 or 1 to 0. Therefore, one way of boosting the high-frequency component in advance before it can be attenuated by the line, is actually to pre-distort the signal in such a way that the distortion is in the opposite direction to what the line will bring about.

We do this by a pre-emphasis circuit and the pre-emphasis circuit essentially dumps a lot of extra power only when there is a transition from 0 to 1 or 1 to 0. This actually makes sense. If the line is sitting steady at 0 or 1, then it does not require too much power. It is only when you have to change the state of the line with its large associated capacitance from 0 to 1 or 1 to 0 that you have two either put in or remove large quantities of current.

Therefore, if we have a smart driver which puts in high amount of power only selectively only when it is needed, namely when there is a 0 to 1 or 1 to 0 transition, in that case the overall power consumption will be kept in check. At the same time, we will be able to send data much faster. It is this idea which is used by the dynamic overdriving techniques.

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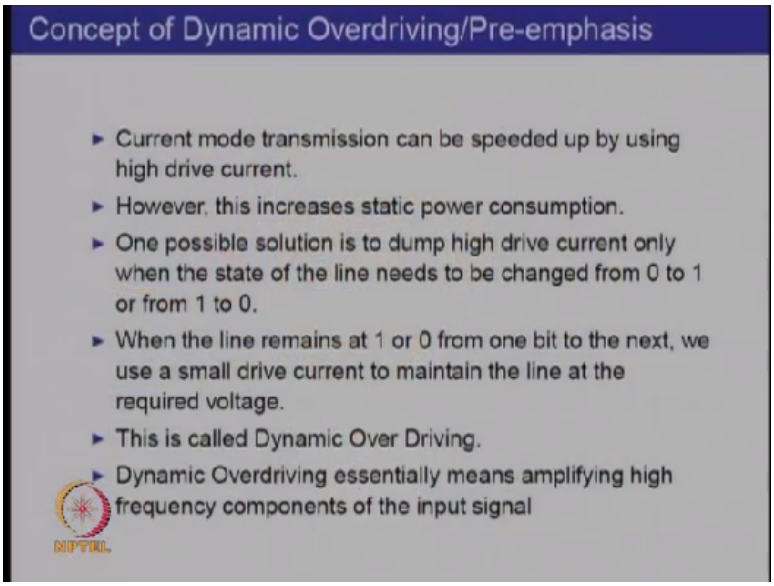

So this is what we are saying that when the line remains at 1 or 0 from one bit to the next. We just use a small drive current to maintain the line at the required voltage; however, when there is

a change from 0 to 1 or 1 to 0, we either dump or remove current and large quantities of it at that time.

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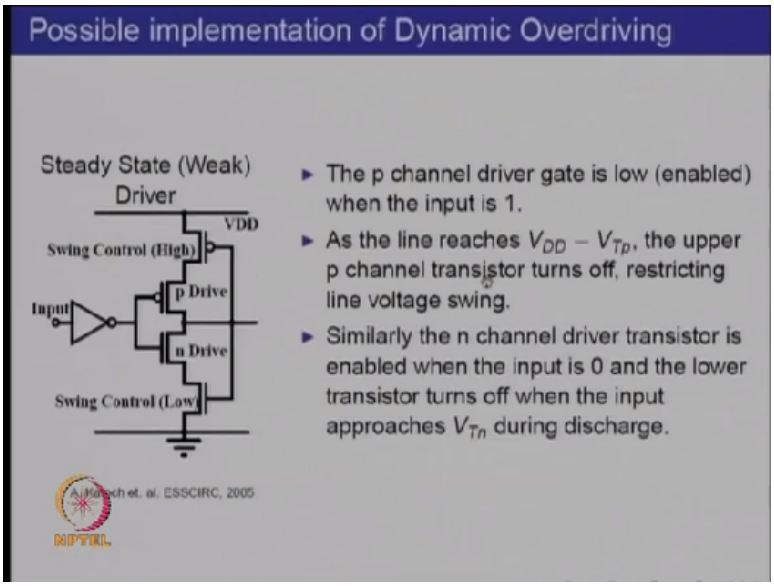

That means now we need two different kinds of drivers, one is the weak static driver, the other is the strong dynamic driver. The strong driver will come on only when there is a transition. The week driver will make sure that adequate power is supplied even when there is no transition at the input. Let us look at the week driver first, this week driver is taken from the work done by Atul Katoch et al from the Philips laboratories.

And this paper was originally published in the European solid-state circuits conference in 2005. The full-scale digital input is applied here. So the traditional rail to rail swinging input appears at the input of that buffer. We now need a special driver which will not force the output all the way to VDD or all the way to ground. Remember this is the week driver and this is largely used when the input remained steady at 0 or 1 for multiple bits.

If you did not do a careful design, what will happen is that this line, even though week, will continuously dump current or continuously sync current till the line is taken to a voltage which is close to VDD or close to ground and we do not want that. We want this drive to stop as we start approaching VDD or ground and that is ensured by the circuit configuration suggested in this paper.

If you look at this circuit, these two transistors, in short, form a traditional inverter, this is a p channel transistor and this is an N channel transistor. So therefore there is not much to understand in this part of the circuit. The other two transistors act as witches controlled by the bus voltage itself. Now consider the case that we were trying to drive the line high, that means the input is at 1.

When the input is at 1, this node because of the inversion will go down to 0 and it will go all the way down to power supply because this is a traditional inverter. Now if this voltage goes down to 0, then this transistor will turn off. Because this transistor is off, there is no current taken from the line towards ground. On the other hand, because the output is at 1, this p channel transistor turns on, it starts pouring current into the line which is largely RC type which starts charging up.

As the line charges up, this particular switch, remember the line was originally low and that is why this switch was also on. As the line charges up as we approach VDD minus the absolute value of VTP, the effective negative bias on this becomes less than VTP. As a result, this transistor now turns off and even though this is an inverter, the power supply from the inverter has been taken away and therefore this driver stops driving the line towards VDD.

In other words, for voltages from the resting voltages close to VDD by 2, to VDD minus VTP, this upper transistor is on and therefore this acts like an inverter and dumps current into the line. This continues till this voltage reaches VDD minus VTP. Once we reach this voltage, the upper transistor cuts off and now there is no drive available to take the voltage any higher, that means the output is automatically limited to going up to VDD minus VTP and no higher.

Exactly the same thing happens when you want to drive this line low. Suppose the input is 0, this is a traditional inverter and therefore this output will go all the way to VDD. Because this point is at VDD, both of the p channel transistors will be off. Recall we are trying to drive this line down to low values now and therefore we want to discharge the line down to low values which is done by the N transistors.

Because the input is 0 and this node is at 1 which is close to VDD, this N channel transistor will now turn on. The line is presumably high otherwise why are we trying to discharge it. So because the line is high, this transistor is also on as a result this series combination is now on and it starts discharging this line towards ground. This discharging will continue as long as the line remains above VTN.

As soon as a voltage goes to VTN and drops below this, this transistor will now turn off and this will discontinue the discharging of the line. As a result, we have seen that this weak driver accepts an input which is rail to rail, the standard logic kind of input, it drives the output like an inverter but makes sure that the output high value remains at VTP below VDD when charging and remains a VTN above ground in case of discharge.

Therefore, full charge and discharge is not possible and this line has limited swing from VDD minus VTP TO VTN. Should we want to control the swing even further, we could actually use two transistors in series here and then we will get a 2 VTN draw.

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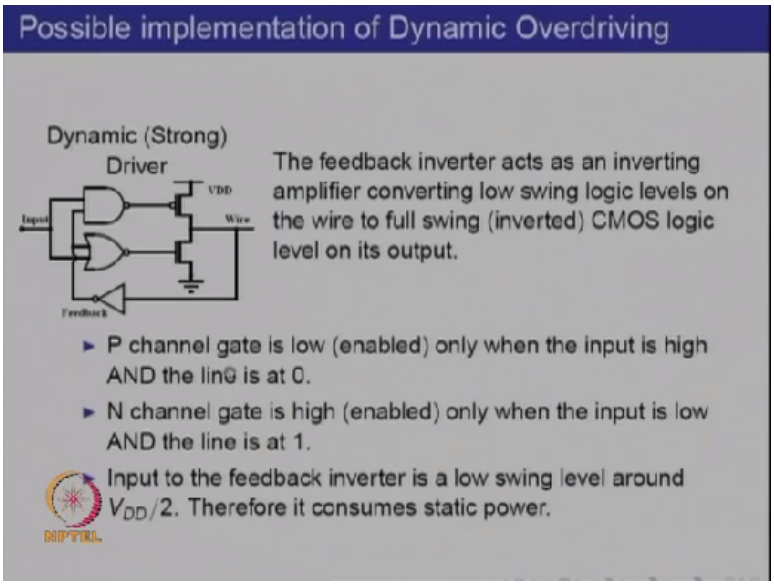

That was the weak driver. So the job of the driver was essentially to ensure that the input is buffered to the wire. The only difference being that while the input will swing from rail to rail, the wire will swing over as low swing region. The dynamic driver needs an arrangement so that it turns on only when there is a transition.

So let us look at this circuit. This driver is a traditional inverter driver. These transistors are made strong so that it can dump or withdraw large amounts of current from the wire. We use the feedback inverter here and this feedback inverter apart from inverting the logic, converts this low swing value on the wire to a full swing output, that means this buffer is actually required to amplify as well and therefore does consume power unlike standard CMOS gates which do not consume static power.

This one however is bias to be near VDD by 2 because this wire rest near VDD by 2 and therefore it continuously draws current; however, there is sufficient amplification here so that a relatively small swing on the wire results in a full digital swing at the output. This feedback value and the input are combined with this NAND-NOR logic which ensures the drive is applied only when there is a transition. Let us analyze the functioning of this strong driver a little better.

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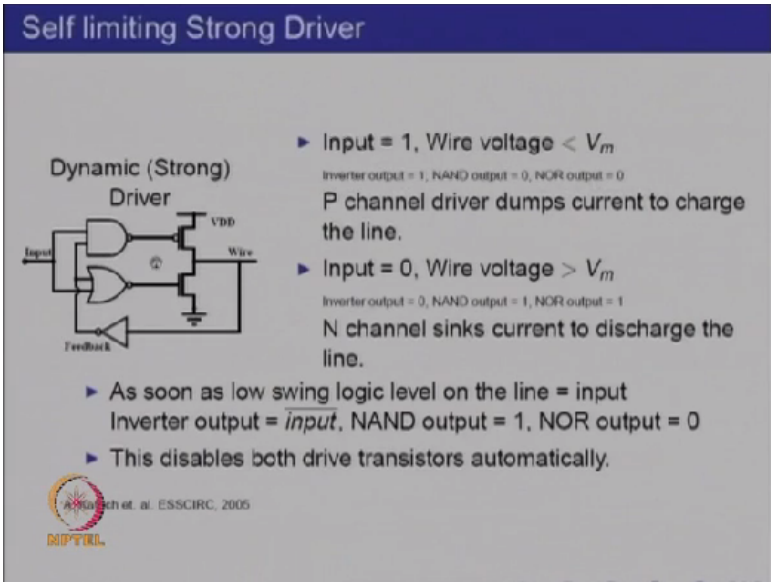

Consider the case when the input is 1 and the wire voltage is low, that means there is a transition, the wire is resting at 0 and the input is 1. Because the wire is resting at 0, the inverting output is 1. So the digital input is 1 and this feedback value is also 1. Because both of these are 1, this NAND goes to 0. Also because both are 1, the NOR also goes to 0, that means both these inputs are at 0 and this circuit acts like an inverter with both gates shorted and returned to 0.

As a result, it starts charging up the output towards 1 and because these are very strong transistors, we have applied strong additional drive to the wire when there is a 0 to 1 transition. What happens when this voltage reaches 1. Remember this feedback inverter will now go to 0, that means the input is at 1 and the feedback is at 0. The line has now reached 1; therefore, this feedback voltage will become 0.

When this is 1 and the input remains at 1, this being 0 is sufficient to force this NAND to 1 and if this NAND goes to 1. The upper transistor turns off, that means if once this output becomes 1, that by itself irrespective of anything else, is adequate to make this 0 and a 0 is adequate to make this 1 by itself and that is adequate to turn this transistor off. On the other hand, if the output has now reached 1, then this point is at 1, the input is at 1 and therefore this output remains 0.

Therefore, the N channel is off. In other words, when there is a transition for a short time, when there is a 0 to 1 transition for a short time, the p channel turns on and dumps current into the wire. As the wire voltage rises and actually becomes 1, this configuration automatically turns off and now both the transistors are off. As a result, this wire is now maintained at 0 or 1 by the weak driver that we had discussed earlier.

Now let us consider the other case that means the previous output was 1 and the input is now 0. Because the input voltage was 1, the wire voltage is greater than the trip value or the mid value of this feedback. As a result, because this voltage is actually high and we are trying to drive it to 0, this high produces a 0 here. In other words, the digital input is 0 and this voltage is also 0. If both of these are 0, this ensures that the NAND is at 1.

And therefore the p channel transistor is off. But since both are at 0, the NOR output is 1 and that turns this transistor on. Once this transistor is turned on, it starts discharging the bus and this is the strong transistor, very wide transistor, as a result. It will take away current very quickly from this wire bringing it below VM. As soon as this wire is brought to a 0, the feedback value will become 1.

Now the input is at 0 and the feedback is at 1. A 0 input means that this NAND is guaranteedly

high irrespective of the feedback; however, since the output has now reached 0. The feedback value is 1 and that by itself is enough to drive this output to 0 and therefore the drive is now removed from the N channel transistor. That means both transistors are off and now we shall not consume any more power in keeping this wire at 0 or 1.

So in short, this NAND-NOR combination ensures that power is applied of the proper kind to the wire only for a short while, while it remains at the wrong digital value. If both the values are equal then because of this inverter, both these values are unequal, that means once the wire has reached the desired value equal to the input then these two are guaranteed to be unequal and that means exactly one of them is 0, the other is 1, it does not matter which is which.

If the two inputs are unequal that at least one of them is 0 and that ensures that the NAND output is 1 and the p channel transistors of off and if the two are unequal, it ensures that at least one of them is 1 and that is sufficient for the output of this NOR to go to 0 and that ensures that the N channel transistor is also off. So essentially what it means is that once the wire logic value in low swing becomes equal to the input logic value.

Then, this drive is automatically removed and both the p channel transistor and the N channel transistor are off. So therefore the high drive provided by the strong driver is applied only as long as the wire and the input are different values. Once the wire acquires the input value, this guy is turned off and now will not be turned on unless an input different from the current value namely during a transition.

So when an input like that arrives, only then power will then be used in these and either a current will be dumped or a current will be sunked depending on whether the input is 0 or 1. So this is the basic operation of this dynamic or strong driver. There are many other considerations which are possible for this dynamic or strong driver and we shall look at these configurations as well a little later.

However, this one using feedback makes it clear how we continuously monitor the line and as soon as this line has reached the desired logic value. No further power is consumed by the strong

driver, it automatically turns off. This gives us a very interesting idea. Remember dynamic overdriving is done at the transmitter. Inductive termination is used at the receiver. So should we try to combine both and apply dynamic overdriving at the transmitter and inductive termination at the receiver.

We examined this suggestion and did computations to see whether additional improvement is brought about by this combination.

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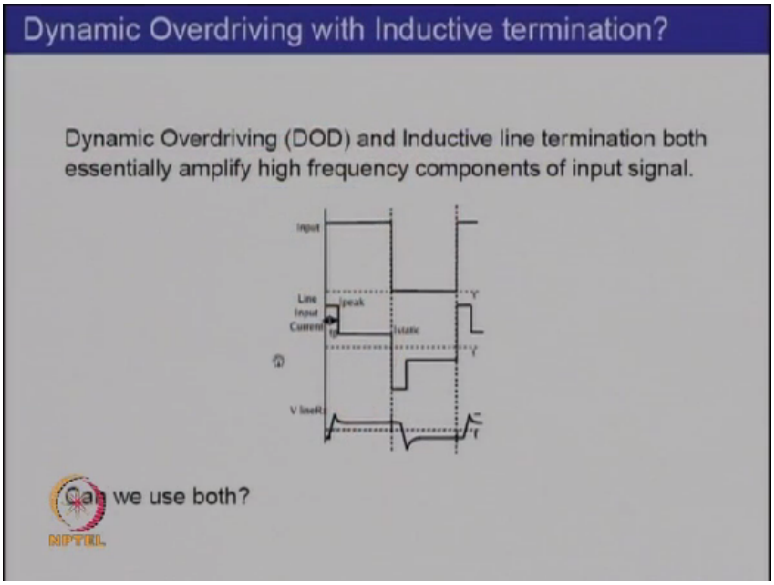

Here is the waveform of the input digital value and here is the effective drive applied to the line. During this short time when there was a transition, we have seen that the strong driver turns on and the total current dumped into the line is very large. Ones the line reaches the value 1, then the strong driver turns off and now only a small static current is provided by the weak driver.

When that is a 1 to 0 transition on the input then our line is actually coasting at 1 and we need to discharge it and that is done by a very large drive which is provided by the strong driver now which detects this 1 to 0 transition as we have seen in detail just sometime back and therefore essentially the N channel transistor is turned on very heavily. this means a large amount of current is taken out of the line for a short while.

As the line discharges and just comes below the apparent 0 for the low swing inverter, then the N

channel transistor turns off and now there is no further drive applied. So the shape, by the way this is a plot for the current which is down or removed from the line and negative value means current is removed and it has this shape, a positive value means current is dumped and it has this shape. This dotted line represents 0 current.

So therefore if we use the dynamic over driver, then this is the shape of the current pulse which is then applied to this line. If we now integrate this into the RC which is represented by the line, then you get a slight overshoot here but essentially a flat curve and a slight undershoot but then a flat curve maintaining the line at 0.

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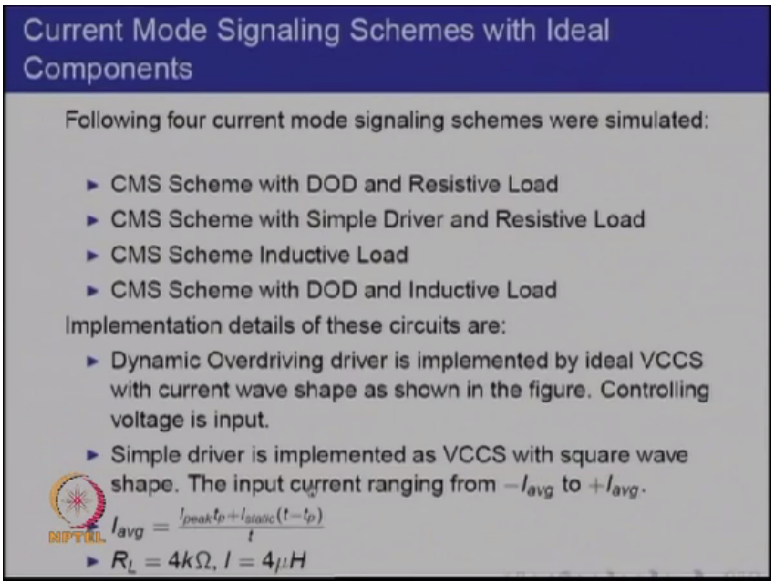

The question that we now want to answer is whether both can be used and to answer this question, we simulated 4 combinations. One of these combinations, the first one has the current mode scheme with dynamic overdrive on the transmitter end but a pure resistive load. This is the pure CMS scheme with dynamic overdrive. We also had a control signal which uses the current mode scheme with a simple driver without any dynamic overdrive and with a resistive load.

Then we designed the circuit which uses the current mode scheme; however, it uses an inductive load and finally a CMS scheme which has both namely a dynamic over driver on the transmitter end and inductive load on the receiver end. Now we only want to know whether it is worthwhile and therefore we do not use actual circuits here. We use macro models. So the dynamic

overdriving driver is implemented by ideal voltage-controlled current sources and with the current wave shape as we had just seen.

So the controlling voltage is the digital input. The simple driver is implemented as a voltage controlled current source with a square wave output shape. If the input is 1, it provides certain amount of current. If the input is 0, it provides a certain amount of negative current. Therefore, the input current ranges from minus AI average to plus I average. The I average is given as the weighted sum of I peak here, I peak is the current provided by the strong driver times the time for which the strong driver is on plus I static times T minus The patient.

So this weighted average over the time T, that is I average and the input average current ranges from minus I average to plus I average.

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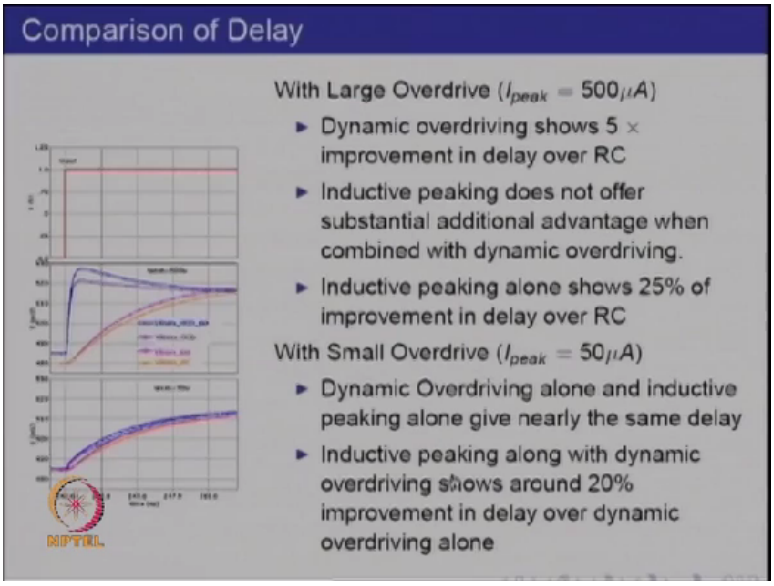

Once we do these simulations, this top curve is in fact the input given as a voltage. So this is the input voltage plotted as a function of time. Now we have 4 curves here. The red curve is the line voltage at the receiver with inductive loading. The yellow curve is the line curve at the receiver but with just resistive loading. Notice that these two curves are very similar; however, the inductive loading does improve the speed, so that comes out quicker.

At the same time, the two dynamic overdriving options are these two and while this is plain

dynamic overdrive without inductive. This is the inductive. However, notice that in the two cases, the rise time remains roughly the same and this is as a function of I peak. The voltage fluctuation on the line caused because of switching. Now we operate these under two separate conditions.

Once when the overdrive is very large like 500 microamps for a short time, the other when there is a small overdrive 50 microamps. Our results are that if you were using strong overdrive which is what you will do if you want very high-speed. In that case, the inductive peaking does not offer substantial additional advantage when combined with dynamic overdriving. As you can see here, the two show practically the same rise time and therefore the advantage of inductive termination is not that very high.

On the other hand, if the overdrive is small, in that case, the improvement is better and then it is worthwhile having inductive peaking. We will stop this lecture here. What we have done is, we have seen the effect of inductive loading and the effect of dynamic overdrive, these two combined can be used one at the transmitter end and the other at the receiver end. However, our studies show that if you want a high-speed link which will require substantial overdrive at the transmitter end.

Then the incremental advantage offered by inductive loading is not very much and then it is not worthwhile adding inductive load. At the low power spectrum, however, you would benefit by having an inductive loading. So in short whether to use both or not, depends on whether you are at the low-power low-speed end of the applications or high-power high-speed end of the applications.

We shall look at a few other dynamic overdriving solutions and then go over to the capacitive driving solution in our next lecture. We stop this lecture here.