

**Advanced Machining Processes**  
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**Week - 10**  
**Lecture – 25**  
**Silicon and processing of Silicon - I**

So, welcome back. Today I would be talking on this microsystem's fabrication by advanced manufacturing processes in the section that I would be dealing today is, what is silicon and how do you process silicon using advanced manufacturing techniques. So, let us now see of some of the materials which are very amenable to the use, you know in developing into their use of developing microsystems. So, silicon of course, is one of the principal materials which are used for microsystem fabrication, because as I mentioned earlier that the traditional processes really are the, sorry the non-traditional processes on silicon are nothing but borrowed from the microelectronic industry. And therefore, being a microelectronic material the fallout processes which really comprise of MEMS processes are amenable to fabrication of silicon. Then of course, quartz and glass, because in most of the cases of microsystems, you sometime need optical transparency and therefore, glasses and quartz are the next line of materials amenable to the, you know can be classified as MEMS materials or microsystems materials.


Then another whole lot of class of materials which are nowadays increasingly used for microsystems fabrication of polymers and then polymers particularly this PDMS or polydimethylsiloxane which is considered to be a very, very bio-friendly material is most used particularly in biomedical MEMS or biomedical microdevices. And then of course, PMMA polymethyl methacrylate which is also an E-beam resist and it is used increasingly for E-beam lithography and other applications. Then this material of Teflon, where Teflon is actually a commercial name of a material available from DuPont, and this Teflon is very, very hydrophobic and it has excellent applications again in the biological world. And so therefore, Teflon is another very amenable material MEMS material which is used mostly for fabrication of microsystems.

And then of course, there is this whole new domain of microsystems which is using biological entities like cells, proteins, or DNA and these are also some of the very, very frontier research areas in the bio MEMS as to how to micro manipulate or nano manipulate sometimes the biological entities for fabrication or advanced manufacturing of MEMS at this particular scale. So let us begin with the silicon. So, silicon of course, is the most popular MEMS material obtained so far and silicon and its compounds, variety of compounds like oxides, nitrides, polysilicon, etc. can be very amenable use for microsystems fabrication. Not only that you can categorize these whole class of materials based on the amount of you know their range of order into crystalline, polycrystalline, or amorphous materials where the definition of these terms are kind of parallel to whatever you know conventional definitions

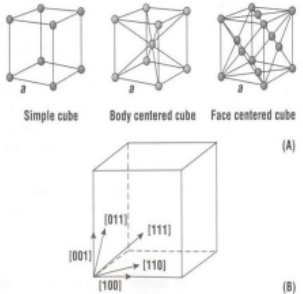
are.

Single crystalline means that there is one particular kind of crystal with the repetition of unit cells and there is no break of this crystal whatsoever. Polycrystalline is that the crystal growth takes place at several centres, and it formulates into grains of different crystals with grain boundaries in between. An amorphous is where the range of order is rather longer where, shorter where there is no orderliness at all, and it is very randomly denoted and so these class of silicon oxide, nitride, and silicon as such, or polysilicon can be categorized into these various forms and domains. So, material like silicon dioxide, for example, are amorphous which means that they do not possess any long-range order. So that is what is basically the categorization of silicon and let us look or delve into a little bit of crystallography and crystal structures.

**Crystallography and crystal structure**



- Crystals are described by their most basic structural element, the Unit Cell.
- Crystal is a regular array of such units repeated in 3-dimensions in a regular manner.
- The unit cell of interest have cubic symmetry with each edge of unit cell of the same length.



Simple cube    Body centered cube    Face centered cube

(A)

(B)

- The 3 commonly used types of cubic crystals are Simple cubic, Body Centered Cubic and Face Centered Cubic crystals.
- The directions in a crystal are identified using a Cartesian coordinate system [x,y,z].
- For a cubic crystal the faces of the cell forms planes perpendicular to the axes of the coordinate systems.
- For ex.: The symbol (x,y,z) is used to denote a particular plane that is perpendicular to the vector that points from the origin along the [x,y,z] direction

When we talk about especially single crystalline silicon, crystals are described by their most basic structural element, the unit cells as most of us know and it is a regular array of such units repeated in three dimensions in a very regular manner which comprises of a crystal and the unit cell of interest have it is a cubic symmetry, and each edge of this unit cell has the same length. So you can divide these into different classes of crystals like simple cubic where you can see there are about 8 atoms on the 8 corners of this particular cube, body centered cubic where you have atoms on the corners as well as one in the centre of the whole cubic lattice and this is what one unit cell would comprise of or look like and a repetition of all these unit cells in the three dimensions would typically result in what you call a single crystalline material. And then you have face-centered where these faces also have some atoms apart from the corners and there is no atom in the centre of this particular unit cell. So, these are some of the classifications of how cubic crystals can be divided as and just to reiterate or just to you know memorize some of the fundamentals which you probably may have obtained earlier. These, the crystals are really represented by directions, and they are identified using Cartesian coordinate system and the square bracket here as you are seeing is

indicative of the direction in which the crystal would grow, you know so it is the direction of growth of the crystal.

So if I say that it is a 1 0 0 growth that means it is growing the crystal is growing in the x direction if it is 0 1 0 it is growing in the y direction similarly if it is 0 0 1 it is growing in the z direction and not only that if you know you can change the planes if the growth is along a certain plane then it can be a 1 1 0 or it can be let us say you know 1 0 1 or a 0 1 1 which corresponds to different planes of the growth and then there can be a very interesting growth along the 1 1 1 direction which means that it is something like a triangle here as you can see. So, the 1 1 1 direction typically is perpendicular to this particular triangle, so the direction of growth is perpendicular to this particular direction. So, whatever it is the directions are represented by these square brackets and it is a sort of sign convention to do that, and you know if you want to represent the plane, a particular plane that is perpendicular to the vector square bracket xyz you represent that by this round bracket xyz which comprises of the plane of which xyz was a direction of. So, this is the plane ground bracket, and this is the direction square bracket and then of course a set of such planes are represented by these third bracket and these set of planes would be meaning all planes of type round bracket xyz represented by the third bracket xyz. So that is the sort of nomenclature which you use for you know systems or for identifying silicon as such.

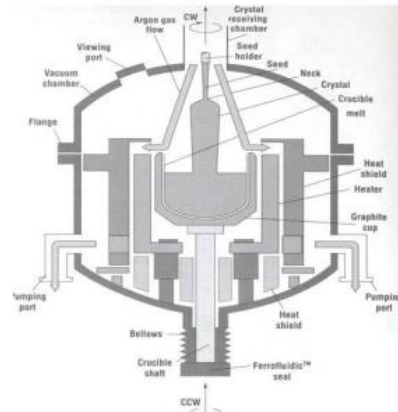
So let us now look into a little bit different aspect of how you can actually make single crystalline silicon and in context of that the most important method that is illustrated in literature very often is the Czochralski (CZ) growth method in which silicon can be obtained from polycrystalline silicon and 99.99 percent pure polycrystalline silicon which is fused and this fusion process is by thermal means there is a crucible which is indicated here in this figure which comprises of a central cavity and this cavity as I am illustrating by this border here contains the silicon material, the polycrystalline silicon fused material, and this crucible so-called is basically capable of rotation. So, you can rotate the whole crucible and also it is inertly filled so that a chamber here is evacuated using pumping mechanisms as illustrated here and here and then you can fill the whole environment or atmosphere of this fused silicon container with argon or an inert gas so that it ensures the non-inclusion of material like oxygen or nitrogen into the silicon lattice. So, it is extremely pure process and there are certain foundries in the world like one example is MEMC which is based in St. Louis at Missouri which actually manufactures some of these silicon wafers, high purity single crystalline silicon wafers.

So, the way the processing goes is that when this crucible is rotated and then there is something called a seed crystal which has been obtained from an earlier process and the seed can be probably a very small crystal of certain direction or grown in a certain direction let us say the 100 directions. So, this seed has been grown from an earlier process, it is a pure crystal, and this seed is inserted into this melt somewhere here as can be illustrated and as is illustrated here. And so, therefore, the rotation, the relative rotation between the seed and the crucible and you know can be varied by varying the relative RPM, and what is important here is that as the seed goes and dips into the material and the seed is slowly pulled out it tries to drag along with it a part of the silicon melt and the moment the silicon melt comes out into the open atmosphere it is no longer you know a part of the crucible and therefore it can as

## Single Crystalline silicon formulation (Czochralski's growth method)



- Single crystal silicon is formulated with Czochralski growth method.
- A small seed crystal with a given orientation is dipped into a highly purified silicon melt.
- The seed is slowly pulled out of the melt while the crucible containing the melt is rotated.
- The material is polycrystalline silicon and is 99.9999% pure.
- The poly is loaded into a fused silica crucible that is contained in an evacuated chamber.
- The chamber is back filled with inert gas and the crucible is heated to 1500 deg. C.



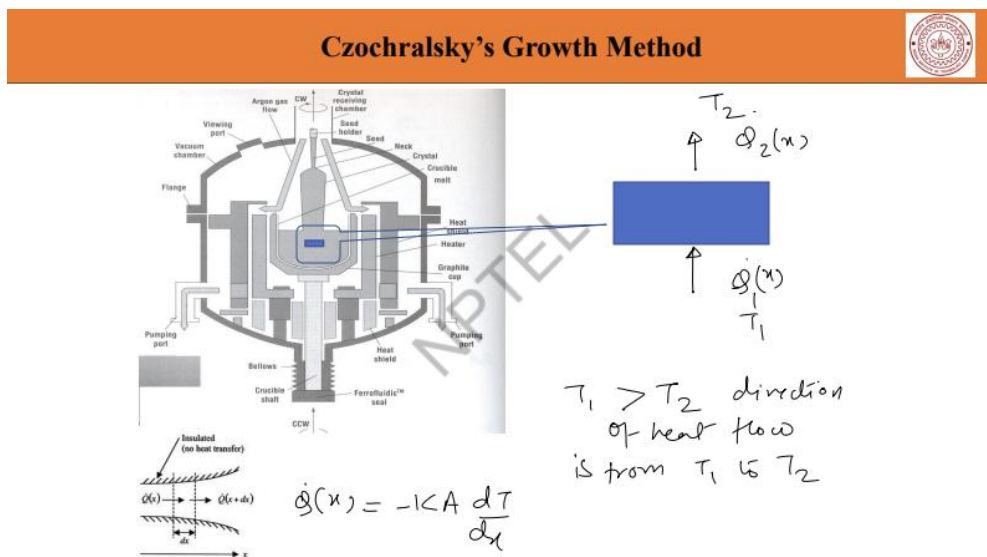
The seed crystal is a small chemically etched crystal lowered into contact with the melt. This must be carefully oriented since it will serve as the template for growth of the much larger crystal.

well, solidify. So only advantage here is that the solidification, the rates of this pulling can be balanced with the rate at which the relative rotation happens between the crucible and the seed, and many other parameters are in a control manner. So, the rate at which the solidification front is being used is very small.

So, the solidification sort of cools off you know you can really tailor it or fine tailor it in a manner so that the growth takes place in the same direction as the direction of the seed crystal. So, this is the Czochralski's crucible process. So, the seed is the mother crystal which would eventually result in formulation of a bowl of material as can be indicated by this outline that I am drawing here and this all material in this bowl is grown in the direction of the seed crystal and the parent direction is kind of grown into this particular bowl. So once this bowl is extracted you can actually cut this bowl into pieces, and you can fine polish them and there are lot of methodologies like CNC wire cut EDM or some other instruments which are used for fine sizing or may be even band saw which are used for fine sizing these wafers. Typically these wafers can vary between 400 microns thickness to about 900 microns thickness.

So some other nitty-gritty of this process is that the chamber is actually filled with, it is back filled with inert gas and the crucible is heated up till 1500 degree Celsius and the seed crystal is really small chemically etched crystal and lowered into the contact with the melt so that the melt can grow in that direction. It has to be carefully oriented because this sort of serves as a template for growth of the much larger crystals later on. So that is how the Czochralski's growth method or growth process is actually executed. Now let us do some mathematical modelling for this process which can give us an idea of how you know the liquid-to-solid conversion can take place in terms of latent heat of solidification and we can just do a simple one-dimensional heat flow analogy to understand the situation. Let us say you have a crucible here in this particular example and we are considering this particular zone here as you can see which is also called the zone of fusion.

Zone of fusion because sort of you know this is the zone where there is a presence of both the states the liquid state which is into the crucible and then the solid state which is a part of the seed which is getting withdrawn and so it is a sort of semi-solid semi-liquid kind of zone that we are considering. So, if we apply the Fourier's law of heat conduction, so  $Q \cdot x$  or the rate of flow of heat as a function of  $x$  or in the direction of  $x$  is really proportional to the interfacial area across which the heat is flowing. So, the interfacial area in this case can be thought of as going into the plane of this slide. So, this is the area across which the heat is flowing, so this is also known as the heat phase and then it is also proportional to the temperature gradient which exists in the material in the direction of flow of heat. So, in this case for example, if the temperature here is  $T_1$ , the temperature here is  $T_2$ , so temperature here is  $T_1$ , temperature here is  $T_2$  and of course, in this particular case  $T_2$  is more than  $T_1$  which enables the heat to flow from the direction of  $T_2$  to  $T_1$ .




So let us say in this particular zone of fusion that is in question, we have a temperature  $T_1$  which is actually higher than  $T_2$  in this particular case which is that of the liquid part of the zone of fusion. So the temperature of the liquid part is  $T_1$  and the temperature of the solid part of the withdrawn seed and the bowl formulated on the seed as a template is basically  $T_2$  as illustrated here and  $T_1$ , of course, is greater than  $T_2$  which enables the direction of heat flow in the positive  $y$  direction as you can see here, because of the heat flows from  $T_1$  towards  $T_2$  and we need to just investigate how the rate of heat flow here into the zone of fusion from the liquid side and the rate of flow out of the zone of fusion to the solid side would be balanced with each other and this heat loss which is happening you know is also a cause of the formation of the solid which means that you know in a solid state as you know the bond energy is always higher and therefore there is a heat of formation of the solid which is lost you know it is called the latent heat of formation of the solid. So, the difference between the rate of heat flow into the zone of fusion and out of the zone of fusion is really the quantity of heat which is lost in formulating the solid from the liquid state. So if you modulate in that manner let us say for example, if we assume completely one-dimensional heat flow in this particular case we can write the heat equation as minus  $K l A dT$  by  $dx$  in the liquid side, the minus shows that the heat is always from the higher the you know the towards

the lower temperature from the higher temperature side which is also we defined by the law of thermodynamics. So  $K_l$  is the conductivity, the thermal conductivity of the liquid melt,  $A$  is, of course, the interfacial area of the zone of fusion and  $\frac{dT}{dx}$  is temperature gradient available across that interface between the liquid onto the crucible and the zone of fusion and of course, this heat goes into the zone and the heat which is lost from the zone of fusion into the solid can be defined as minus of minus  $K_s A$  where  $K_s$  sorry where  $K_s$  is basically the thermal conductivity of the solid material times of interfacial area between the zone of fusion and the solid  $A$ .

We assume the area to be same in both the cases for simplicity of the model here times of  $\frac{dT}{dx}$  where temperature gradient in the solid while the heat flows from the zone of fusion into the solid. So that is the difference of heat flow into the zone of fusion and outside the zone of fusion and this net heat loss here is somewhere recorded as the solid formation or you know the heat of formation of the particular solid. So, if we assume that the rate at which the solid material gets formulated is  $\frac{dm}{dt}$  as you can see in this particular illustration here and  $L$  being the latent heat of formation which is in terms of how much mass per kg, how much heat is lost in order to formulate the solid. So,  $L \frac{dm}{dt}$  is really nothing but the amount of heat, the rate of heat or the rate of heat loss in terms of formation of the solid bonds. Rate of heat loss can be equated in terms of heat going per unit time into the zone of fusion minus heat going away from the zone of fusion per unit time.

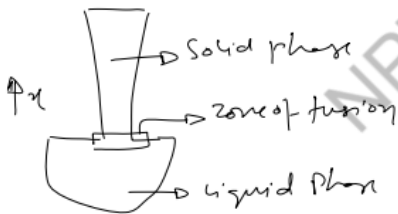
So you can really equate both these equations and that formulates a basis of the Czochralski's growth process because you know heat flowing in here represented by the first term, heat flowing out here represented by the second term, and in between whatever is happening in resulting in this formation of the solid phase the  $L \frac{dm}{dt}$ .

**Czochralski's Growth Method**



Assuming completely one dimensional heat flow

$$\left( -K_l A \frac{dT}{dx} \Big|_l \right) - \left( -K_s A \frac{dT}{dx} \Big|_s \right) = L \frac{dm}{dt}$$



$K_l$  = thermal conductivity of liquid  
 $K_s$  = thermal conductivity of solid

$A$  is the cross-sectional area of the zone of fusion  
 $\frac{dT}{dx}$  is the thermal gradient in 'x' direction

So that is really what this Czochralski's process is about  $\frac{dT}{dx}$  of course is the thermal gradient in the  $x$  direction from the either from liquid to the zone solid zone of fusion or from the zone of fusion to the solid and  $K_l$  and  $K_s$  are respectively the thermal conductivities of

the liquid state and the solid state of silicon. So let us refine this equation a little more by assuming that you have  $\rho$  as the density of the solid in this particular case and of course,  $A$  the area of the zone of fusion defined by a constant  $A$  is the interfacial area and constant  $A$  is the interfacial area and if we assume that  $dx$  length of solid material is formulated because of this heat transfer process. So  $dm$  really the differential amount of mass is nothing but the density times of the volume  $A dx$  which is created by virtue of pull out from the zone of fusion into the solid state. So, if we equate the new term obtained for  $dm$  into the earlier equation we have  $L$  times of  $\rho$  times of  $A$  times of  $dx$  by  $dT$  which is nothing but the pull rate, the pull rate of the seed crystal in terms of the rate of displacement of the solid state.

So, this is the displacement of the seed with respect to the crucible. So, this is the pull rate. So,  $L$  times  $\rho$  times  $A$  times of pull rate is nothing but the heat transfer equation which is  $K_s A dT$  by  $dx$  solid minus  $K_l A dT$  by  $dx$  liquid. We have just taken the negative of negative and so therefore that is why the equation has changed sign. So, if we were to assume that our pull rate is maximum for the purpose of high-yield production we should have a situation where this negative component should go to zero.

### Czochralsky's Growth Method



$$\left( k_s A \frac{dT}{dx} \Big|_s \right) - \left( k_l A \frac{dT}{dx} \Big|_l \right) = L \frac{dm}{dt}$$

$$dm = \rho A dx$$

$$\therefore L \rho A \frac{dx}{dt} = \left( k_s A \frac{dT}{dx} \Big|_s \right) - \left( k_l A \frac{dT}{dx} \Big|_l \right)$$

Left hand side is maximum if

$$k_l A \frac{dT}{dx} \Big|_l = 0$$


or, the latent heat in the zone of fusion is the only heat that is diffusing through the solid.

So therefore, typically whatever is coming as heat into the zone of fusion is really the amount of heat going away from the heat of fusion zone of fusion. So that is typically a case in one-dimensional heat transfer. So, this whole equation is a maximum on the left side only if this liquid heat transfer from liquid into the zone of fusion is zero or the latent heat really in the zone of fusion is the only heat that is diffusing through the solid. And so therefore, this is a one-dimensional case where you have the maximum pull rate  $V_{max}$  represented by  $KA$  by  $L$  times of  $dT$  by  $dm$ . Or  $K$  divided by  $\rho L$  we are just putting the value of  $dm$  here  $\rho A dx$  times of  $dT$  by  $dx$  and this  $dT$  by  $dx$  mind you is in the solid domain as the heat emanates from the zone of fusion into the solid.

So, the maximum pull rate is really proportional to  $dT$  by  $dx$  or the temperature gradient from the zone of fusion onto the solid. The solid material and so therefore, one may argue that if

you have a very large  $dT$  by  $dx$  it would result in maximum yield or maximum pull rate which is actually not the case. So normally the maximum pull rate is never used and what happens is that the that is because if you give it very less time to formulate then there is always a tendency of a lot of point defects particularly in the zone of fusion near to the melt and therefore, the point defect density would go up very high if the  $dT$  by  $dx$  increases. So quick cooling would help to sort of on one hand create a lot of defects into the next formulating zone from the liquid.

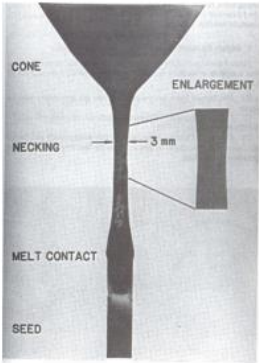
### Czochralsky's Growth Method



$$V_{max} = \frac{dx}{dt} = \frac{KA}{L} \frac{dT}{dx}$$

$$= \frac{K}{\rho L} \frac{dT}{dx} \rho$$

Thus, the maximum pull out rate is a proportional function of  $\frac{dT}{dx}$  within the solid.




- In reality, the maximum pull rate is not normally used.
- The crystalline quality is a sensitive function of the pull rate.
- The material near the melt has a very high density of point defects. So quick cooling would help to prevent these defects to go into the formulating crystal.
- However, too much gradient may create large thermal stresses and thus dislocations, particularly in larger diameter wafer.

Although the defects may not be going into the solid crystal because you have very less time given for the cooling process to take place or the solidification to take place. However, another aspect of this huge too much thermal gradient is also creation of large thermal stresses within the solid which would rather create dislocations and particularly this is true for larger diameter wafers that the dislocations are very, very prominent because of that. So, it is really a trade-off between the pull rate and the way that the defects would go into formulating the crystals or the amount of thermal stresses that the crystals can handle and this together would define how much pull rate is really needed and it is really not a yield decision sometimes, yield based decision sometimes. It is basing itself on the purity of the material particularly where because we are growing single crystalline silicon here, purity of the material in terms of point defects, high the density and also thermal stress created dislocations etc. So, it is a function of a lot of other quality parameters for the wafer apart from the yield.

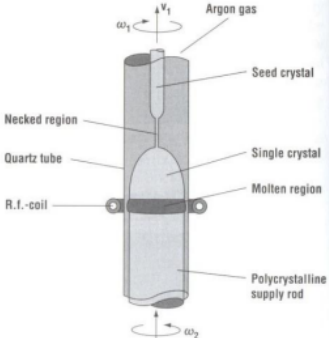
So that is how the Czochralski's growth process works. So, the other method which is of some prominence is basically the single, you know it is called the float zone method which is again another very important method for realizing single crystalline silicon. So, in this particular method also called the float zone method, you know it is a, it is basically used for extremely high purity silicon growth although downside of this particular process is that you cannot really go above a certain diameter of production of wafer-like in Czochralski's you could go up to any extent including 8 inches or you know 5 inches bigger size wafers are also



possible. In this particular case, it is only limited to smaller size wafers and the process for production really is similar.

**Single Crystalline silicon formulation (Float zone method)**


- This method is used for extremely high purity silicon growth.
- A rod of high purity polycrystalline material is held in a chuck while a metal coil driven by a high-power radio frequency signal is slowly passed along its length.
- Alternatively, a focused e-beam can also be used for heating the rod.
- The field setup by the RF power leads to eddy currents and joule heating and the material is melted.



- To enhance the growth along the preferred crystal orientation a seed crystal is injected into the top of the molten rod.
- In this technique a thin neck of 3mm diameter and 10-20mm long is pulled and the pull rate and the temperature lowered to shoulder the crystal out to a larger diameter.

You have the concept of a seed crystal in this method as well as we had in Czochralski's however, in this particular case as you can see there is a polycrystalline rod which is being pushed into the small orifice here and by means of non-contact mediated heating like an RF mechanism may be you heat this particular surface of the wafer to almost its melting temperature while pushing the polycrystalline rod all the way into the orifice and on the other side you lower the seed crystal into the, into the this orifice here and you lower it and the seed crystal is actually used as a template for formation of growth of this polycrystalline material being pushed through the orifice onto the other side.

So, from the naked region really in this particular region the seed crystal grows and makes you know a single crystalline silicon of the type of seed crystal from the polycrystalline melt which you are pushing through this particular orifice. So, both the rod as well as the feeding rod as well as the wafers are moving at certain omega velocities and one good advantage here is the uniform heating. So, there are very less thermal stresses and as such no thermal stress-related dislocations which is otherwise the case in Czochralski's method where there is a huge thermal gradient available because it is essentially a contact mode heating. Here most of the heating means are RF-based so that this non-contact mediated and there are no thermal dislocations whatsoever in the particular crystal. So, that is another method of formulation of single crystalline silicon known as float zone method.

So, the other material of importance of you know for to the microsystem fabrication is has been indicated is glass. And glass is actually chemically silicon oxide, and the content of silicon oxide however varies from different glasses. For example, soda lime glass would contain about 68 percent of silicon oxide, borosilicate another variety of glass would contain about 81 percent and the highest and the purest form of glass is the quartz really it is fused silica which is actually 100 percent silicon oxide. And basically, there are certain other metal

oxides along with silicon oxide which are present which would determine the optical transparency or clarity of the glass to you know the whole UV vis, UV visible region of the spectrum. And so therefore, certain characteristic metal oxides and metal ions would emit their own signatures making glass unclean and absorb at certain frequencies whereas quartz being the purest or the highest form of glass will not absorb any of these wavelengths and would have a clean background as such.

So, glass itself has a variety of desirable properties for example, it has high mechanical strength, it has high electrical insulation, transparency, high chemical resistance which are all amenable to microsystems. So, therefore, glass sometimes can be used for packaging microsystems typically. And commercially available glasses are now available freely like you know which can be photo patterned. Foturun is one such glass can be directly photo-patterned on to the substrates. And therefore, you know with glass also you can actually use photo chemical machining or PCM to you know result in a variety of features and structures at the microscopic length scale.

So, for etching glasses for creating crevices, cavities, features, structures of the micro-scale within such glasses you normally use buffer HF solution, which is actually a solution of HF along with ammonium hydroxide and water. So, that is what glasses are or that is how glasses are important for the microstructure domains. Let us also look little bit into the wafer specifications of silicon wafers and so on. So, essentially how they are prepared from the bowl which are being obtained either by Zochralsky's method or by the float zone method. So, the bowl is first characterized for resistivity and crystal perfection, and these are done by various electrical tests on the bowl.

Then the seed and tail are cut off the bowl and they are mechanically trimmed to proper diameter. And then of course, then finally, there is a finish trimming operation on to the final wafer diameter since additional etching will still need to be done on those bowls.

### Wafer specification and preparation

- The boule is first characterized for resistivity and crystal perfection.
- Then seed and tail are cut off and the boule is mechanically trimmed to proper diameter.
- The diameter at this point is slightly larger than the final wafer diameter, since additional etching will still be done.
- For wafers 150mm or less, flats are ground the entire length of the boule to denote crystal orientation and doping type.
- The largest flat called the primary, is oriented perpendicular to the <100> direction.

(a)

(b)

Cleanliness (particle/cm <sup>3</sup> )	<0.03
Oxygen concentration (cm <sup>-3</sup> )	Specified + - 3%
Carbon concentration (cm <sup>-3</sup> )	< 1.5 × 10 <sup>17</sup>
Metal contaminants bulk (ppb)	< 0.001
Grown in dislocation (cm <sup>-2</sup> )	< 0.1
Oxidation induced stacking faults (cm <sup>-2</sup> )	< 3
Diameter (mm)	≈ 150
Thickness (μm)	625 or 675
Bow (μm)	10
Global flatness (μm)	3
Cost (\$/cm <sup>2</sup> )	0.2

So, for wafers 150 mm or less flats are ground through the entire length of the bowl to denote crystal orientation. So, if you have 1 0 0 direction you will have that flat pointing out as a plane towards the plane perpendicular to the bowl. To indicate the perpendicular direction as the direction of growth of the particular crystal. So, most of the silicon wafers that you get from industry would have one or two cuts indicative of certain specifications, particularly growth-related specifications of the silicon wafer. So, the thing that has to be remembered is the largest flat which is also known as the primary flat in such a circular wafer is oriented always perpendicular to the 1 0 0 direction. So, therefore, it is actually the x direction in a right-handed coordinate system Cartesian coordinate system and the flat is always perpendicular to the x direction and that indicates the direction the other directions of the crystal. So, in comparison to that flat you can record what is the 1 1 1 direction or 1 1 0 direction or 1 0 1 direction or any other direction with respect to this x direction. So, one thing has to be very carefully seen or observed in any silicon wafer which comes from such a foundry you will have to first see what is the largest flat and that is called the primary flat and it is always oriented perpendicular to the 1 0 0 direction.

Apart from that there are several other specifications of relative importance for example, you can actually have cleanliness in terms of particles per centimetre square on the surface area, you can have indication of oxygen concentration per centimetre cube that means this per unit volume, carbon concentration per unit volume, metal contaminants in terms of parts per billion within the crystal lattice and then also you can have per unit area what are the growing dislocations, sometimes these are very well measured using sophisticated non-contact mediated optical characterization tools like interferometry, etc. Then you can also have an idea of oxidation-induced stacking faults and that can be in the bulk of the wafer, so that can be per unit volume. Apart from that some normal specifications like diameter and thickness of the wafer or the bow which is nothing but the way that the wafer is warped or bent sometimes and then aspects like flatness and cost. So, these are all indicated in a wafer box which comes from such a manufacturer or a foundry of silicon. So, these are some of the specifications which normally the manufacturer supplies, and then with this specification on and the direction of the flat one can characterize the wafer very well.

So now, once we have had a good introduction to silicon and glass, let us look at some of the MEMS fabrication techniques which are really available. So, it is really all about fabrication of micro nanostructures inside silicon or glass or some of the materials amenable for MEMS fabrication that we are concerned with. So, it is formation of structures which could be actually used for sensing or actuation purposes at the micro-scale. So, that is the purpose of this kind of fabrication. And the idea is that this microstructure so formulated should be able to process some signals, it can be electrical signals, or it can be non-electrical like mechanical signals which can be somehow processed by means of transduction of these features or you know micro structured elements.

And for production of these, you have to use some conventional and some new semiconductor manufacturing techniques in the MEMS region. And some of these manufacturing techniques could be something like chemical machining like etching, it could be gas-based or based on some chemicals, it could be deposition where you can deposit a metal film or a resist film on the top of some of these wafers. And then of course, photolithography where you can use the power of optical signals or light to actually carve and find out different features, sizes and structures onto these films. And then you can use a variety of other processes like oxidation, epitaxy, etc. which are planned like for example, epitaxy could be used for growth of single crystal silicon or oxidation as a matter of fact is thermal process whereby you can actually entrap oxygen in silicon and at the cost of silicon you can get a layer of silicon oxide or silicon dioxide.

So, these are sort of conventional semiconductor manufacturing processes which have been merged into the MEMS domain or microsystems fabrication domain. Apart from that there are deep RIE or deep reactive ion etching which is a very new technique in the micro-systems domain. And then of course, thick plating which is also used this is electroplating which is a sort of electrochemical machining operation where you can actually deposit films of certain size. And so therefore, these are the two other domains which are very commonly used for MEMS systems or microelectromechanical systems. Apart from that of course, there are these non-traditional processes like USM, AJM, EDM and ECM which have been very recently incorporated for doing activity in fabrication of the microsystem or micro-manufactured components or devices.

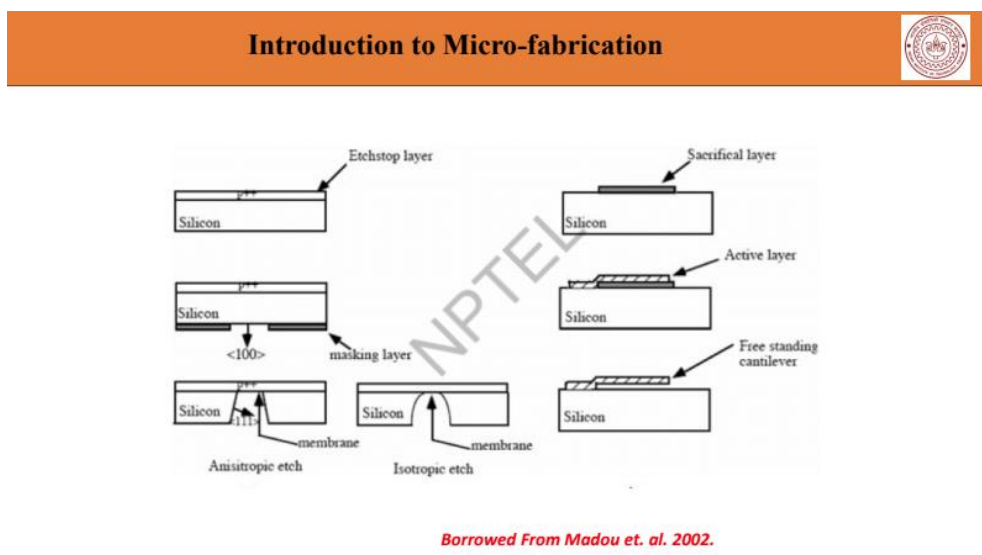
So, if you look at all these machining processes in bunch, they can be categorized either as bulk micromachining processes or surface micromachining processes and the bulk processes really are about the subtractive removal of material or subtractive processing of material from a wafer surface. For example, in this particular illustration here or cartoon here you can see this right here is a section, a cross-section of the silicon wafer and you are trying to selectively etch off the material from this wafer. So, there can be, for example, a protective layer here which you have etched out and created a small crevice or a cavity. So, another example is this particular etch pit here which is a high aspect ratio structure, and this can be obtained by a process called deep reactive ion etching where the power of plasma can be used for driving atoms in a particular direction. So, that they can knock off the surface atoms here and then based on that high aspect ratio structures can be formulated.

The third example as illustrated here is again a very interesting example where there is a P double plus layer which has been impregnated here using an implantation or some doping technique and then as an anisotropic etch which actually goes on from the backside here and the material is selective to only silicon and so to P double plus. So, therefore, whenever the etchant actually comes and hits this area it actually leaves a membrane here, a thin membrane here, because it is not able to etch this part it is selective to P double plus as I already mentioned, and the remaining silicon is etched away. So, this is another way of getting what you can say thin film pressure sensors, and this is also known as bulk micromachined

pressure sensors. So, why it is bulk is because you are subtractively removing material from the volume of this particular wafer and that is why bulk micromachining is a subtractive process it is a material removal mechanism. On the other hand, surface micromachining is an additive process where you do not really remove the material from the bulk of the wafer, but you keep on adding different layers of materials onto the top of the wafer because of which you can create these features and structures.

To exemplify some let us look at this illustration here as can be represented. So, here for example, this is a polysilicon layer which has been put in a manner so that you had a sacrificial layer in this particular region given by the dots, it could be a resist layer and then you have deposited the polysilicon layer on the top of this resist layer and then later on you can remove the resist layer away because polysilicon is a high strength material so that you can have a channel on the surface on one side and buried within this polysilicon layer on another side. So, you can remove away this resist later on it just goes off thus resulting in this channel into the plane of the paper or plane of this transparency slide. So, this is an example of surface micromachining or additive micromachining. Other examples could be deposition of this pillars and pores by using either metals or photoresist where the structures so realized can be of some significance.

For example, all the metallic interconnects in electronic microelectronics circuitry is actually made using such metal imprints, it is called printed electronics, and it is again an additive micromachining process or a surface micromachining process. So, in a nutshell, machining can be divided into bulk where you are subtracting from the volume, and surface micromachining where you are adding material on the surface to do microstructures and features. So, these are the two broad categories of all machining processes that can be assembled to realize microsystems or microfabricated architectures.



For example, is a slide which has been borrowed from Dr. Mark Madou book on microfabrication. So, here it is showing how you can formulate a P double plus membrane,

and this has already been illustrated. So, you can actually formulate a small cavity here using resist and so this can be used as a etch window as and there can be an etchant which can be selective to P double plus which is actually highly doped positive silicon on the other side. And so, the material starts etching away in anisotropic manner thus formulating a 54-degree angle and based on this the, it just goes up to the selective layer which is the P double plus layer and stops the etching process thus creating a membrane. The other hand this side is showing how a microcantilever can be generated by additive micromachining where you have let us say a sacrificial layer over which you have put let us say a polysilicon layer like this and then you are removing the sacrificial layer away so that you can have a small cantilever which you have illustrated here in this particular example. So, these are some of the process flowcharts or logic diagrams for formulating some of these Microfeatures and microstructures in different illustrations.

So, if you look at the bulk micromachining technique, the first process that comes into existence is the etching and particularly wet etching where there is a chemical which is used for etching off the material. So, it is a subtractive technique again, the etchant is a highly, highly corroding, or eroding agent which engraves its wherever it comes in contacts, contact with the wafer and removes the material so that you can have these features etc. imprinted and the etching solution is basically very often used in all the microelectronic processing and also in MEMS processing. So, etching can be divided into two classes, one can be isotropic or homogeneous etching where the material removal is uniform as a function of the volume and there can be an isotropic etching where etching can be in a particular direction and the differences are in terms of etch chemistries as I will illustrate in detail in the following slides. So, let us look at isotropic etching and isotropic etching really as I mentioned before the etchant is able to remove or erode away material at uniform or homogeneous rate in all the directions.

**Subtractive Techniques**



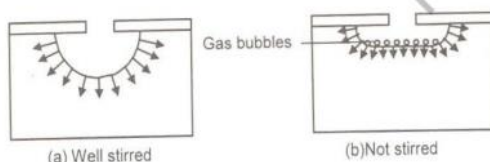
**Wet etching:**

Wet etching is referred to as etching processes of solid materials in a chemical solution.

Wet etching in microelectronics are mostly isotropic, independent of crystalline orientation.

Because of the under-etching effect, isotropic etching has drawbacks in designing lateral structures.

If the etch solution is well stirred, the isotropic etch front has a spherical shape.



Examples of Wet Etchant Recipes for Thin Films of Functional Materials (After [3])

Material	Etchants	Selective To
Si	HF, HNO <sub>3</sub> , CH <sub>3</sub> COOH	SiO <sub>2</sub>
Si	KOH	SiO <sub>2</sub>
SiO <sub>2</sub>	NH <sub>4</sub> HF	Si
SiO <sub>2</sub>	HF, NH <sub>4</sub> , H <sub>2</sub> O	Si
SiO <sub>2</sub>	H <sub>3</sub> PO <sub>4</sub> , NH <sub>4</sub> , H <sub>2</sub> O	Si
Si <sub>3</sub> N <sub>4</sub>	H <sub>3</sub> PO <sub>4</sub>	SiO <sub>2</sub>
Al	H <sub>3</sub> PO <sub>4</sub> , HNO <sub>3</sub> , H <sub>2</sub> O	SiO <sub>2</sub>

This for example, is an illustration where there is etch protective layer which is now emboldened by the red pen here and so this window here of the etch protective layer is able to give an access to the fluid to go into and start etching away the material which is underneath

this protective layer and in the process because it is a homogeneous process the material actually goes into the, into the material itself and it is able to remove this etch cavity and it starts etching in all directions resulting in this undercut. So, this layer here which has been formulated let us say if this distance is  $x$  this is also known as the undercut because this was not really intended for it was not planned and because of the homogeneity of the etching, the etching would happen in the lateral as well as the vertical direction which would always result in this kind of an undercut. So, when you design microsystems and the masks for the microsystems this undercut allowance has to be taken into account for the designing to happen. If the etching was not homogeneous for example, as illustrated here the etching may be a little more directional. So, in this case, for example, you can see the etch rates are more towards the side.

So, lateral etching is more and the vertical etching it would result in different shapes based on what is the directionality of the etching. And so typically if you had a very well stirred solution where whatever is coming out is going away from this etch window it would result in a homogeneous profile like this. If you do not have a stirred very well-stirred solution it would rather result in this because the amount of atoms which are coming out of this material would have a higher concentration here and thus diffusional restrictions would prevent further etchant to move away. And so, the rate in the vertical direction would be reduced in comparison to the horizontal direction. Let us look at some of these materials and the etchants which are used for the materials and what it is selective to.

So, etch selectivity again is a term which is used in reference to the fact that you know the, there are certain materials which may not be able to get etched away by the etchant solution. And in that kind of a case this material which is not affected by the etchant solution can be used as a protective layer to stop the etching process very accurately. And therefore, an etch stop layer or an etch selective layer is always preferred as the layer which would prevent the etching from happening any further. So, let us look at this table back again here. So, the material illustrated can be silicon, silicon dioxide, silicon nitride, aluminium so on so forth.

And then there are these etchants which are amenable to removal of these materials. For example, HF or HNO<sub>3</sub> or CH<sub>3</sub>-COH or for example, KOH they can remove silicon very easily. But as soon as the etchant meets a surface of SiO<sub>2</sub> it is selective to SiO<sub>2</sub>. So, it will not etch SiO<sub>2</sub> anymore or it will not etch Si anymore in this particular illustration where NH<sub>4</sub> and HF combinations are used. So, therefore, there are certain materials, certain etches which are etching away this material and it is selective to silicon, or it is etching away the silicon and it is selective to SiO<sub>2</sub>.

So, the combination of these can be used for a variety of etching architectures that can be realized accordingly. Thank you.