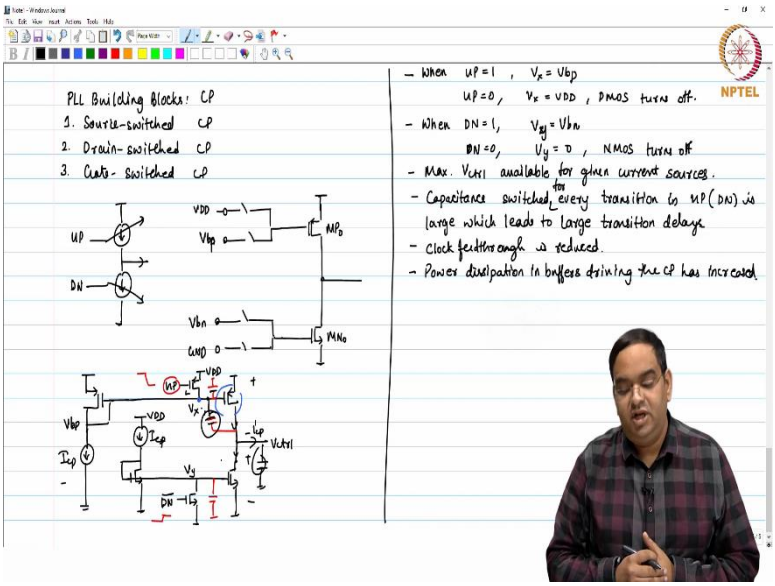
Phase-Locked Loops
Dr. Saurabh Saxena
Department of Electrical Engineering
Indian Institute of Technology Madras

Lecture – 53
Circuit-Level Design of Charge Pump: Part III

(Refer Slide Time: 00:14)



Hello, welcome to this session. We have been discussing PLL building blocks and we are looking at different kinds of charge-pumps. So, we will continue with our discussion. We have seen source-switched charge-pump, we have seen drain-switched charge-pump and now we will look at gate-switched charge-pump. So, it is like for an ideal current source, you can think, I disable the current source itself. With respect to UP signal, I am going to disable this current source.

Similarly, with respect to DN, I am going to disable this current source. Ideally, that is what we are going to do. So, I have a PMOS current source and an NMOS current source like this. I am going to, when I am going to disable the current sources, what I am going to do is, you can think about it, I am having potential V_{bp} and similarly potential V_{bn} and I am going to connect between this and I will have another switch. So, this is the switch which connects here and then I have another switch which connects to VDD and this is what I will do, ground or you can say zero potential.

So, V_{bn} is already there, V_{bp} and V_{bn} are the bias potentials which I generate and with these bias potentials, I enable or disable my current sources. So, this is MN_0, this is MP_0. So, how can I easily implement this? This is the way I have shown you is more of an ideal case. So,

what I will do is the following. I have a PMOS current source with a diode connected to generate the desired bias voltage V_{bp} and you will use only one current source, so you generate the other bias voltage also V_{bn}. So, this is what we generated.

Now, you have this particular voltage. Either you can add a switch or what you can do is you can connect directly to this PMOS. Similarly, you connect this to NMOS and at these nodes, you can have a PMOS switch which pulls this node to VDD. So, this is with UP. When UP is high, at that time, this node is, if I generate, if I call this node as V_x and this as V_y, so, you have V_x node equal to V_{bp} or whatever the bias voltage which is required here and in the other case, you will have this particular node generated to V_{bn}. So, this is $\overline{DN}$.

Now, there is one problem which you will see here that if I pull this node to V_{bp}, even my NMOS is not going to work. So, I have to keep a separate bias for both these cases. So, let me just do that. I can just remove this particular part from here and say somehow, I am going to have a separate current source of the same value and connect this to VDD. So, this is the same.

So, in this particular case, just look at it. When $UP = 1$, at that time, $V_x = V_{bp}$ because $UP = 1$, PMOS is not active, this node is pulled to VDD, the current source is off and when $UP = 0$, $V_x = VDD$ and PMOS turns off.

When you have $DN = 1$, at that time, $V_y = V_{bn}$ and when $DN = 0$, at that time, V_y potential is pulled down to 0 and NMOS is turned off. So, what you see here is that the gate voltage of the PMOS current source and the NMOS current source, these gate voltages are turned off by the switches which are controlled by PFD outputs UP and DN.

So, this is the way you can turn on or off the current source. When these two transistors are turned off, at that time, $V_{GS} - V_t < 0$ and then when you make the transition, at that time, when this gate voltage is pulled down to V_{bp} by the current source, it will take some time but your transistor will actually go from cut-off region to saturation region because the V_{DS} of the transistor is quite large.

The best part of this is for V_{ctrl}, you have maximum V_{ctrl} available for given current sources in the charge-pump. So, if you need wide voltage range for your V_{ctrl} in your PLL, you have the best option to use while using maximum V_{ctrl} available for given current sources.

Then there is a bad part of this which is that the capacitance which you are going to see at this node because this is the gate of the PMOS transistor. So, you think about it, every time you are

switching on or off the gate of the PMOS current source. So, the capacitance switched for every transition in UP and DN is large which in turn leads to large transition delays from UP to the current source. So, this is a bad part.

The good part here again, there are many good or bad parts which we see. The good part is that there is these large transitions, these clock transitions which are happening, they are happening here at UP and DN and since there is a large gap connected because of the gate itself, so the clock feed through which may come because of C_{GD} is minimized. So, clock feed through is minimum, is reduced, you would say.

Now, when you are changing this gate voltage from VDD to V_{bp}, if you want to make it fast and your switch sizes which are helping you to do so, those switch sizes have to be large and if your switch sizes are large, then the buffers which are going to drive these switches, they will also consume a lot of current. So, you can say power dissipation in buffers driving the charge-pump has increased as compared to your drain- or source-switched charge-pump.

So, what we have seen so far is three different kinds of charge-pumps, drain-switched, source-switched and gate-switched and depending on the application, depending on our requirement, we can use gate-switched if we need to have maximum range for V_{ctrl} and we are not worried about the speed of the transition from UP or DN to the final current output, we can use gate-switched. Source-switched is like one of the fastest charge-pumps which you can have. It does suffer from some amount of clock feed through and some amount of charge sharing also.

Charge sharing happens whenever you have a transition between two nodes or whenever you have a transition between two voltages on the same node, then because of the capacitors connected at that node, you will see the charge sharing. So, that thing happens there, it happens in all these cases. So, it is like it will happen here also that when this potential goes from VDD to V_{bp}, so, you will share the charge with the capacitor at the loop filter. You have this capacitor, you have this capacitor, one of the node potential changes, you will see the charge here. So, that exists in all these cases. You have seen the clock feed through and the region of operation for different sources.

Now, whatever we have done so far, we have only made sure that we have used the bias circuits also for the current sources that once all this dynamic is over, once the current settles, then $I_{UP} = I_{DN}$, that is what we have seen. But what we will see in the coming sessions is that this is, first thing is whether this will happen across the range of the control voltage or not, what

we will do and if there is a mismatch during the transition, what happens in the PLL. Those are the things which we will cover in the next session. Thank you.