Phase-Locked Loops
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Lecture – 42
Large-Swing Ring Oscillator: Part IV

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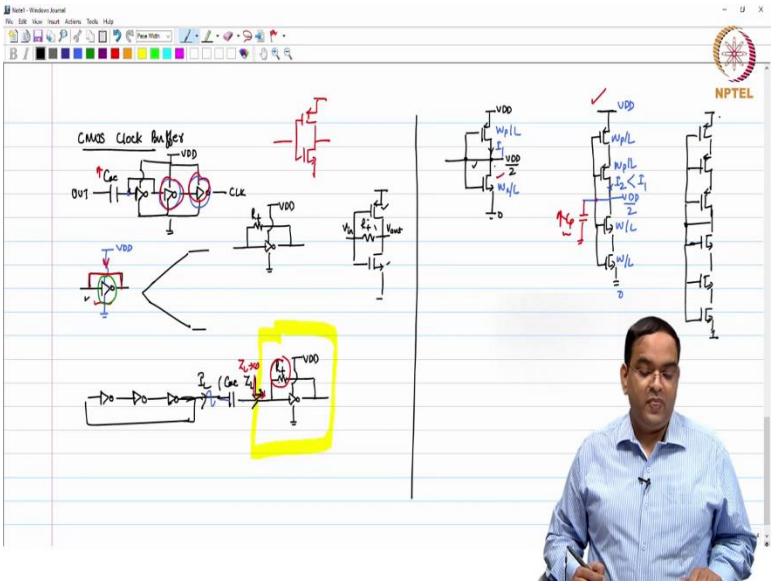

Hello, welcome to this session. In the previous session, we looked at clock buffer or you can say CMOS clock buffer where we buffered the oscillator output coming from the oscillator using an inverter like this and then connected here. We chose an optimum value of the capacitor C_{ac} which is the AC coupling cap and this was connected to VDD. This OUT is output of the oscillator and this is clock.

So, now, well, if you think about it, you will get the desired clock. The buffers will add some amount of noise. Now, this particular inverter, when you are doing a power optimized design, this particular inverter which you are seeing here, this inverter is conducting current, is always conducting current actually because your gate and drain are shorted, so both PMOS and NMOS, they are always conducting.

So, sometimes it happens that this inverter has a lot of power or current consumption. So, because this inverter has a lot of current consumption, there are two alternatives. One of the alternatives is

that in place of using this inverter connected back-to-back, you connect that using a large resistor. So, let me just draw it a little more clearly.

So, you have a resistor like this, well, this is connected to VDD and this is connected to ground and this is R_f. So, when you connect a resistor in feedback across the inverter, your input and output, this inverter is going to be biased for sure like this. So, it is going to be biased like this. So, PMOS and NMOS, they are still conducting current always and they are biased in saturation. Your DC operating point is in such a way that this potential V_{in} and V_{out}, they both are same with this feedback resistor.

The thing which changes here is that because you are having a resistor, large resistor here, so when you are going to connect your oscillator with this load, so you have an oscillator and when you connect this particular inverter, so you have an AC coupling cap like this. We have chosen the AC coupling cap in such a way that at our frequency of oscillation, this AC coupling cap acts like a short. So, for the frequency of the oscillation, it acts like a short.

So, you are loading your oscillator with this particular buffer, this is the buffer now. So, when you load it, the current which is going into this load will be minimized because the impedance is, earlier the impedance in this case which is seen by your oscillator is $\frac{1}{g_{mp}+g_{mn}+sC_p}$. Now, in that impedance, you get feedback resistor which increases the impedance seen from here.

Because it increases the impedance, so, the current drawn from the oscillator, the current which is drawn from the oscillator, I can call this as I_L, this current will depend on the impedance seen. And if you are loading with a very low impedance, that means a lot of current will go in driving that and it is also going to change the output frequency. Ideally, if I say that looking in the buffer case, the looking-in impedance Z_L tends to infinity.

Then your buffer will not actually load your, loading your system with infinite impedance, it is not going to change the frequency, it is not going to take any current from the oscillator. But when you are loading with this self-biased inverter in this manner, you have a low loading which draws current from the oscillator and changes the output frequency. So, to increase that impedance, we actually introduced this resistor R_f.

The current consumed within the inverter still remains the same as it was. So, there were a couple of problems as I told you. One thing is that the current which is consumed in this buffer and this still remains the same. We have not yet tried to address that. The thing which we address is the current drawn by the buffer from the oscillator. And in the same way, you can also say the frequency changes in the oscillator because of the buffer, those two things are minimized.

The second option which we have or which you can utilize, you want to bias this node or you can say you want because I am following up this self-biased inverter with inverters to amplify the signal. So, somehow I need to get this voltage here which is the same voltage as we get for the self-biased inverter, but I do not want to consume a lot of current by connecting in this manner. So, how to do that? Another option which we have is the following.

So, let us say when I had this inverter connected in this manner like this, I assume that this is VDD, this is 0 and this potential happens to be $\frac{VDD}{2}$. The current which is consumed will depend on your gate overdrive and threshold voltages. So, I change my top and bottom branch or you can say I starve this inverter itself in such a way that if I use two cascodes here or you can say if I increase the length of this device, both NMOS and PMOS, then the power consumption is going to be lesser.

So, what I do is increasing the length is typically same as this. So, in place of using the self-biased inverter as shown on the left, I go and use the inverter as shown to you on the right. So, if I do this, then I can very well design this circuit in such a way this voltage is also $\frac{VDD}{2}$. The current consumption in this circuit, so if I call this as current I_1, the current which is flowing here is I_1 and the current which is flowing here is I_2, and $I_2 < I_1$. I am using the same MOSFETs, let us say, $\frac{W_p}{L}$ and $\frac{W_n}{L}$.

So, this is $\frac{W_p}{L}$, size is the same. So, if I do this, then $I_2 < I_1$. So, you can reduce the current consumption in the self-biased inverter. But all other inverters which you are seeing here, all these inverters are going to be same as simple single inverter, we are not going to do anything to that. There is a trade-off in doing this. The trade-off in doing this is that when you connect more devices at the gate node, the parasitic capacitance increases.

You are having double the length, so surely you will have larger area, the parasitic capacitance will be more and because the parasitic capacitance increases, now to respond to the increase in the parasitic capacitance, you have to increase C_{ac}. So, there is a limit on this, you cannot overdo this. So, maybe you can think of going from cascode of two MOSFETs to cascode of three, but you know what you are losing now.

So, what you lose is the area for C_{ac} and more loading coming because of C_p. But you save on the power which is consumed in the self-biased inverter, that is what you do. So, surely you can use not more than two or three cascodes in your CMOS clock buffers. So, this is the way in which we can actually buffer our CMOS clocks used with the oscillators. Thank you.