Phase-Locked Loops
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Lecture – 24
Charge Pump PLL

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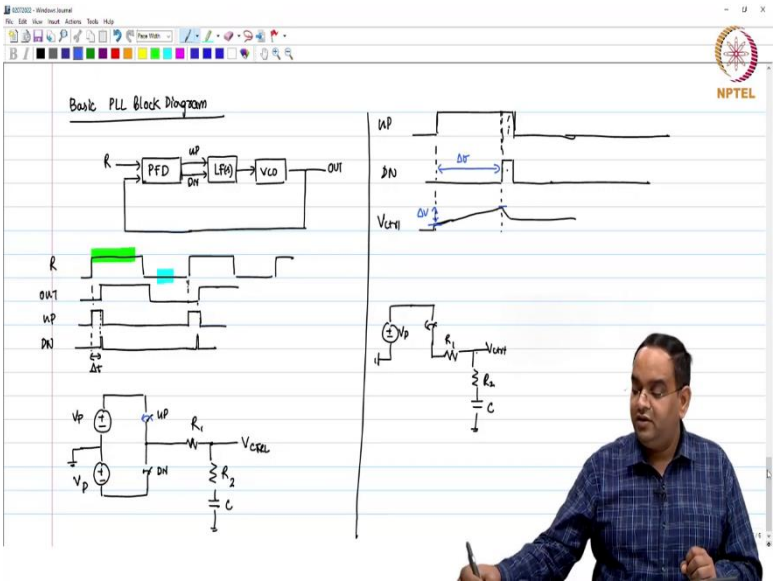

Hello everyone. Welcome to this session. Earlier, in the basic PLL, we have looked at different blocks for PD and PFD. So, let me just look at the basic PLL block diagram, I will first draw that. So, you have PD or PFD, now since we know that PFD is more beneficial when we want to detect the frequency and the phase error using the same block, so I will go with PFD now.

So, we have the PFD. The PFD output actually gives us two signals, UP and DN, and these UP and DN signals have to be somehow interfaced with the loop filter because the average of UP and DN signal has the information about the phase error. This goes to VCO and then you feed it back. So, this is the reference, this is the output.

So, the question which we have before us now is how we are going to convert these UP and DN signals to some voltage signals and then get it filtered by the loop filter. So, let us look at it what these UP and DN signals are and how they look like. So, for example, we have seen this, but I will just redraw it. So, you have this R signal and you have OUT signal, at any given time if you have a phase error, then your waveform may look like this. In response to this R and OUT signal, I am going to have UP signal like this, and this is periodic. So, I am going to have UP signal like this and then the DN signal will happen to be something like this, very

narrow but both of them come down at the same time. So, this is what I will have, practically this will happen.

Now, UP and DN signals, if you look at it, these UP and DN signals have the information about the phase error in the pulse width. I want to convert this phase error to a voltage, that is what I need to do because loop filter is going to process the voltage. So, I have a couple of options before me if you look at it. One option before me is, so UP and DN since they are digital signals, they have high and low, they can very well control the switches, so I come back to my switches.

So, I have a switch which is controlled by UP and I have another switch which is controlled by DN, depending on when my signal is high, high means like this and low is this value. So, do not consider anything else. High is this value, and low is this value, so it should be clear. So now, these UP and DN switches connect a voltage source, for example, V_P, let me just draw the circuit first, this is grounded, this is V_P, both are V_P, and then you have some filter here, R_1, R_2 and C, and this happens to be the loop control voltage. So, I converted from voltage UP and DN signals to the loop filter output, so let me just write this as V_{CTRL}.

So, if you look at it, what is going to happen during this case? This is one option in which we can convert the UP and DN waveforms to voltages. So here, I will just amplify the time during which UP is high. So, this is the duration for UP, and then you have DN signal, during the DN signal, let us say this happens. I will neglect this particular part but this is just the amplified part. During this time, both the switches are high. So, when UP signal is high what happens is that the switch which is controlled by UP signal gets closed. When the switch gets closed, your circuit becomes like this, switch is closed, you have this as ground, V_P, it connects closed switch, it connects through R_1, R_2 and C, this is V_{CTRL}. So, V_P gets connected to this circuit and the control voltage will vary depending on V_P, and it will vary only during the time the switch is closed.

So, I am not solving this particular part but I am just writing V_{CTRL} whatever the previous value it had because it has a capacitor. So, based on this particular capacitor, what you will see is that this voltage will increase and just drawing it, do not go by this curve, I am just drawing it like this. This voltage whatever voltage it has, it will be proportional to V_P for sure. I am not writing the exact equation but it will look like this. And then when both of them turn high, this voltage will effectively be zero. So, you are applying zero to this resistor, so your voltage may come down, when both of them may come down and then it will remain. This is what will happen.

Now, to implement this, so if you think about it, what we have done so far is that this information is passed to the control voltage with this kind of voltage change. So, effectively I am not writing this ΔV here in the equation, this ΔV is going to be proportional to the time Δt and also to the phase error which you have. So, this is like a voltage-based implementation for the phase error to the control voltage.

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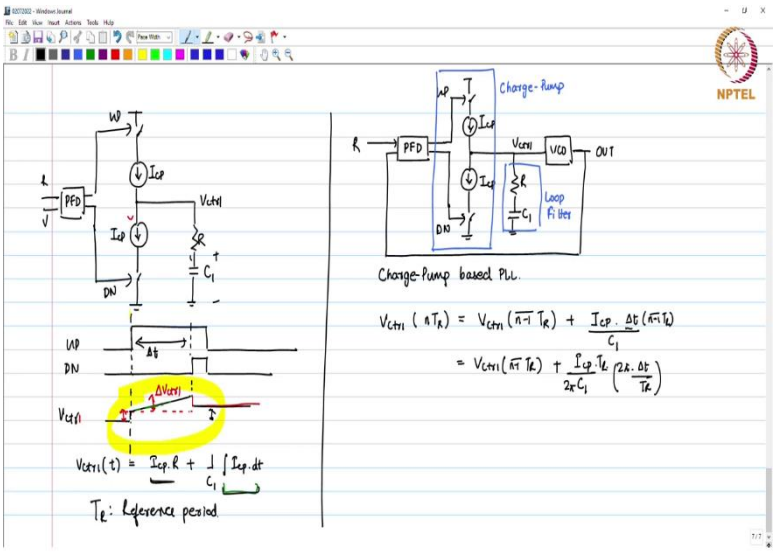

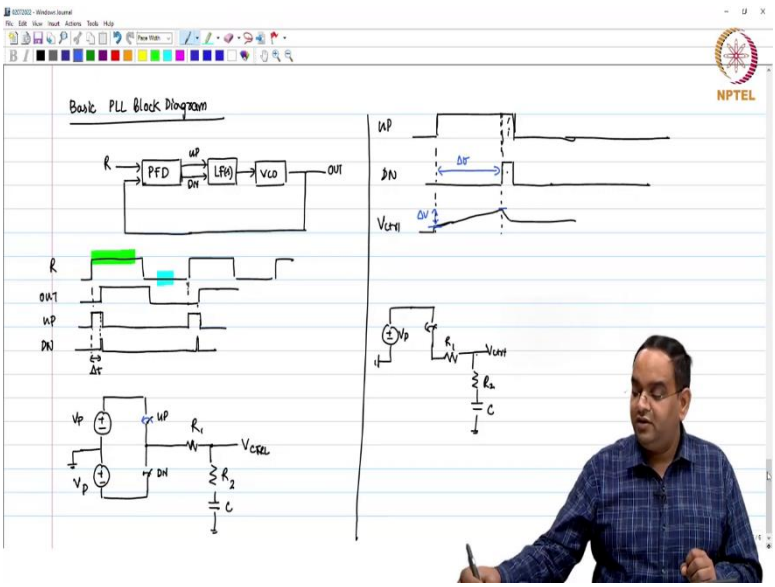

In contrast, you have a current based implementation where you again use two switches with two current sources like this. So, you have this switch controlled by UP, this switch controlled by DN, both the current sources are equal, and this is getting connected to the loop filter. Why am I using this loop filter? We will see it later but assume that this is the loop filter which we have right now.

You can recall actually that we need an integrator, so, the capacitor is playing the part of an integrator. We need the proportional path, so here resistor is playing the part of the proportional path. That is how we came up with this simple loop filter. Now, we are interfacing our PFD with the loop filter in place of the previous one using voltage sources, here we are using current sources, so this is what we have.

Now, in this case, again, you look at the same UP and DN pulses, so if UP happens to be like this, and DN signal is like this, these are amplified UP and DN signals, this is actually the phase error or Δt error. So, what will happen here is, when UP signal is high, your switch is going to be closed from the top side, the V_{CTRL} voltage will actually increase, it will increase like this. When UP and DN signals both are high, the current from the top flows to the bottom, no current flows to the V_{CTRL}, if no current flows, the voltage should actually remain constant.

So, previously I_{CP} was flowing, but now I_{CP} does not flow, so, you will retain the change in the voltage. So, this voltage variation which you have, ΔV_{CTRL}, this is also proportional to Δt. Previously, I did not write for the exact expression or exact waveform here because here you will see an exponential settling with respect to R_1 and R_2 whereas in this case, there is no exponential settling, the current directly goes through the loop filter.

So, if I want to write the exact equation, I can write it as follows:

$$V_{CTRL}(t) = I_{CP}.R + \frac{1}{C_1}\int I_{CP}.dt$$

So, this appears to be a very simple expression. You see $I_{CP}.R$, a jump here, and the continuous increase which you are seeing, that is this term.

So, this particular implementation appears and happens both to be easier than the implementation which you just saw before using voltage sources. So, what we are going to do is that we are going to use this particular implementation in our PLLs to convert the PFD output to control voltage.

Now, for the same thing, we need to find from this PFD to the loop filter. So, let me first draw the block diagram how our connections will look like. So, I have current source, then I have another current source with a switch and then it is like this, this is I_{CP} and this goes to a loop filter which is R and C_1 which is controlling our VCO and this is fed back, do this, this is your reference signal, this is your output signal, this is V_{CTRL}, these are your UP and DN signals.

So here, you have already seen the phase frequency detector. This block is called as charge-pump. It pumps the charge in the loop filter, this block is our loop filter. And this particular phase-locked loop is very standard and common and it is called as Charge-Pump based PLL. So, we have seen that how we use it here, now in order to analyze it, we need to know the gain of this charge-pump. So, this is a little tricky here that if you look at PFD plus charge-pump just here, let me remove these. So, these are UP and DN signals which are controlling the switches. So, this is UP, this is DN, you have I_{CP} and so on.

So now, you look at specifically, you focus on this part. If the previous instant happens to be, one thing which you are seeing is PFD is detecting the phase error every reference clock period. It is not detecting in between the reference clock period, it happens whenever you get the rising edge on reference. So, when you get rising edge on reference, you get rising edge on UP and so on. So, I can write,

$$V_{CTRL}(nT_R) = V_{CTRL}\big((n-1)T_R\big) + \frac{I_{CP}}{C_1}.\Delta t\big((n-1)T_R\big)$$

where, T_R is the reference period.

This voltage, whatever the phase error you have, for that duration, I am integrating the charge. This $I_{CP}.R$, you are seeing $I_{CP}.R$ during the transition, but at the end the voltage here, what you see at the end, this voltage change is only due to the capacitor. So, we get,

$$V_{CTRL}(nT_R) = V_{CTRL}\big((n-1)T_R\big) + \frac{I_{CP}.T_R}{2\pi\, C_1}\left(2\pi.\frac{\Delta t}{T_R}\right)$$

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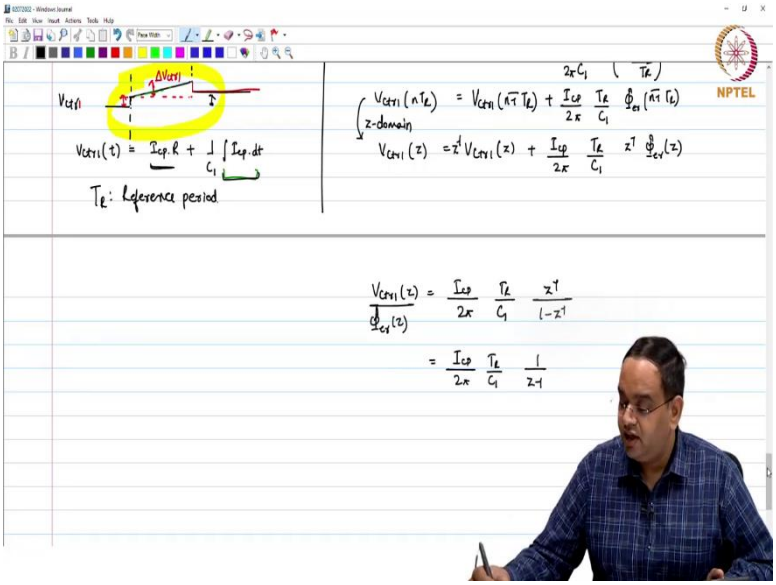

So, we have,

$$V_{CTRL}(nT_R) = V_{CTRL}\big((n-1)T_R\big) + \frac{I_{CP}}{2\pi}\frac{T_R}{C_1}\varphi_{er}\big((n-1)T_R\big)$$

I am writing this in a discrete form right now because that is how things change. I am looking with the average control voltage change at every reference cycle. I will convert it into z-domain because it is a discrete domain. So, we get,

$$V_{CTRL}(z) = z^{-1}\,V_{CTRL}(z) + \frac{I_{CP}}{2\pi}\frac{T_R}{C_1}z^{-1}\,\varphi_{er}(z)$$

$$\frac{V_{CTRL}(z)}{\varphi_{er}(z)} = \frac{I_{CP}}{2\pi}\frac{T_R}{C_1}\frac{z^{-1}}{1-z^{-1}}$$

$$\frac{V_{CTRL}(z)}{\varphi_{er}(z)} = \frac{I_{CP}}{2\pi}\frac{T_R}{C_1}\frac{1}{z-1}$$

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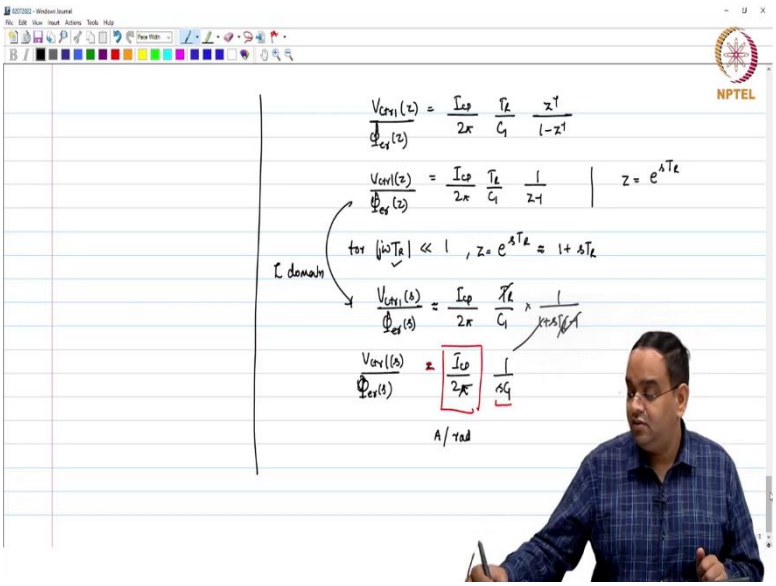

Now, this is the transfer function from the phase error to the control voltage when you are assuming that the phase error information is actually getting converted to the voltage using the charge pump, and in this particular case I have neglected one thing that when I am writing this V_{CTRL}, I am only looking at this change from the previous value. So, in two reference cycles, what was the value in the previous reference cycle, and what is the value in the current reference cycle, that change. This analysis is neglecting actually this part. If you take this into account, it becomes little cumbersome, so I will just neglect that part right now.

So, here, we have,

$$z = e^{sT_R}$$

$$\text{For } |j\omega T_R| \ll 1,\ z = e^{sT_R} \approx 1 + sT_R$$

So, I can convert this into s-domain and write it as,

$$\frac{V_{CTRL}(s)}{\varphi_{er}(s)} = \frac{I_{CP}}{2\pi}\frac{T_R}{C_1}\frac{1}{1 + sT_R - 1}$$

$$\frac{V_{CTRL}(s)}{\varphi_{er}(s)} = \frac{I_{CP}}{2\pi}\frac{1}{s\,C_1}$$

All this math is to tell you that from phase error to the control voltage, if I assume that the role is played only by the capacitor, then what you are seeing is that from the phase error to the control voltage, there is a gain of $\frac{I_{CP}}{2\pi}$. So, what are the units for this, you will see that the unit of $\frac{I_{CP}}{2\pi}$ is A/rad.

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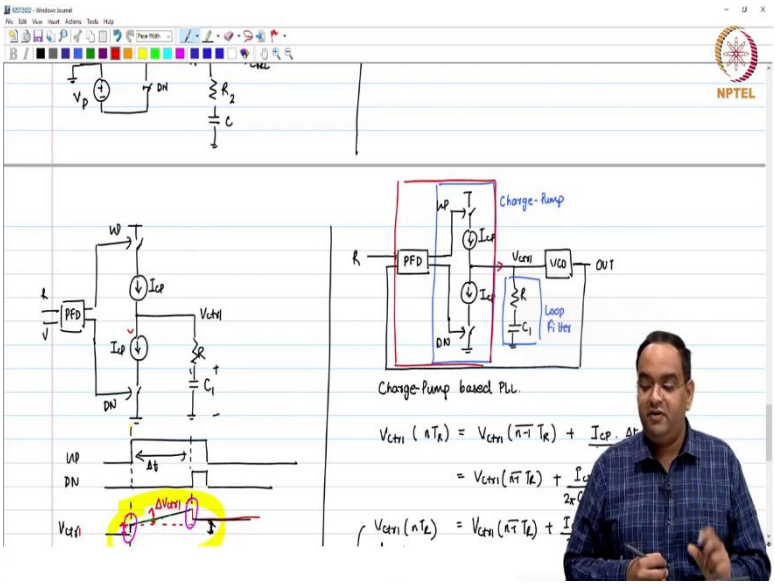

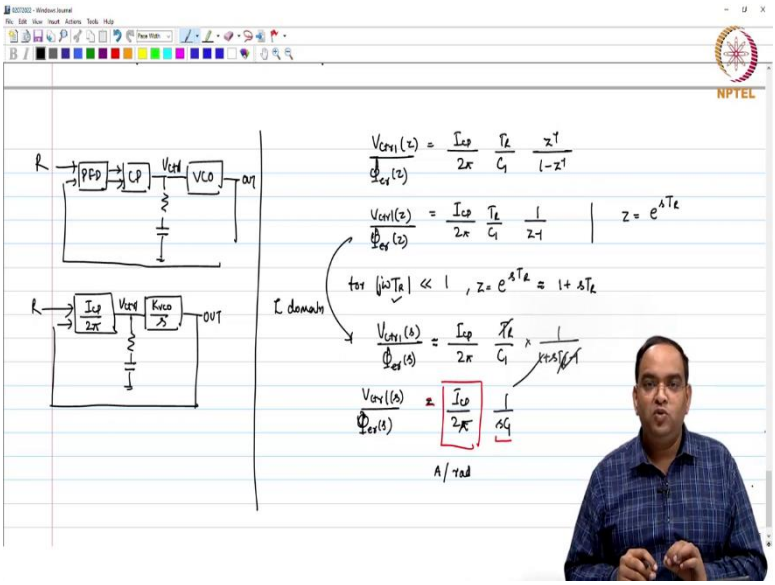

So, this whole block, I will mention it again, this whole block, PFD plus charge-pump can be treated as one single block with gain as $\frac{I_{CP}}{2\pi}$. So, I can model both our PFD plus charge-pump, CP is normally used for charge-pump, goes into the loop filter, controls the VCO and feeds back. The gain of PFD plus charge-pump is $\frac{I_{CP}}{2\pi}$, that goes to loop filter and we can use Laplace domain to analyze this block now which we will see soon in the next session. So, this is OUT, this is R.

So, what did we do? We introduced how to convert the PFD output to the control voltage, we saw two options, we found that the charge-pump based option appears to be much easier to implement. So, then we implemented charge-pump using ideal switches and ideal current sources right now. We figured out the combined gain of PFD plus charge-pump and then we derived the small signal model of a simple Type-II, there is an integrator here, Type-II, Order 2, charge-pump based PLL. Thank you.