Phase-Locked Loops
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Lecture – 22
Phase Frequency Detector

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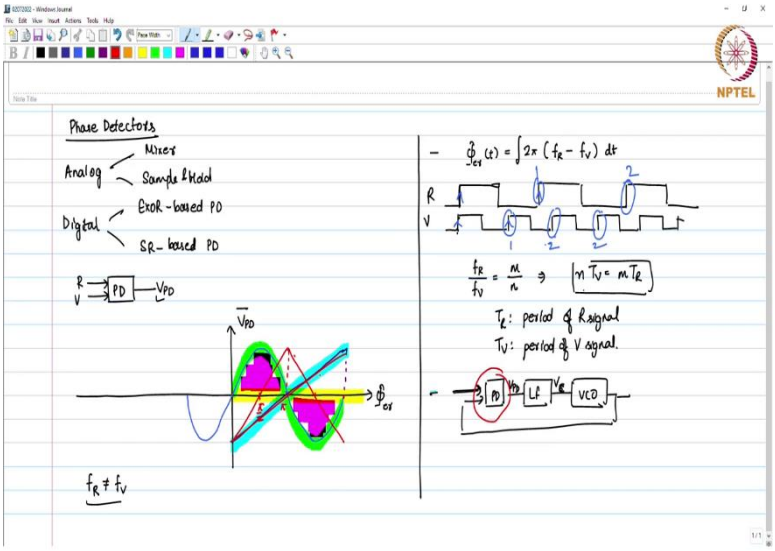

Welcome everyone. In the previous session, we talked about the phase detectors and we discussed analog and digital phase error detectors. So, just a brief recap. So, we looked at phase detectors and there were analog and digital kind of phase error detectors. You have seen two of them as analog and the other two as digital. This is mixer-based or sample and hold based and the other one which you looked at was Exclusive-OR gate based PD and S-R flip-flop based PD.

So, with all these phase error detectors, we actually measured the phase error between the input and the output signals. Now, when you are using these phase error detectors in a PLL, you have to detect the phase and frequency both. So, in that particular case, when you have phase and frequency both, we need to check whether these phase error detectors will be able to detect the frequency error or for that matter whether the frequency error which they can detect is large or small.

So, we need to check those things. So, just consider the phase error detector PD, either of these, we will look at both of them, all of them actually. You have R and V signal and what we used to get is V_{PD}, whether we are getting V_{PD} after subtraction between the UP and DN signals in

case of S-R based PD or the digital one where you have Exclusive-OR gate PD. So, the phase error detector output which we plotted was $\overline{V_{PD}}$ versus phase error and this is something which we have seen that there were sinusoidal phase error detectors which we saw.

Then, there were the ones which we saw earlier was EXOR based where you have your output going like this. So, this is $\frac{\pi}{2}$, this is π. So, you had the EXOR based PD and you have also seen S-R latch based PD which was something like this. So, for all these phase error detectors, let us look at the interesting part about them which is whether they can detect the frequency error or not.

Now, consider these two signals, R and V, and assume that $f_R \neq f_V$, the two frequencies are not same. If it is sinusoidal, then you have seen if the two frequencies are not same, the phase error will keep on increasing, if you are just looking at the phase error detector alone. If it is in a closed loop, then based on the loop operation, you will recover the frequency but here we are looking at whether we can detect the frequency error by using the phase detectors.

So, in this particular case, as we write, so, if $f_R \neq f_V$, the phase error will keep on increasing for sinusoidal signals which you have seen. In case of sinusoidal signals,

$$\varphi_{er}(t) = \int 2\pi(f_R - f_V)\, dt$$

That is what you have for sinusoids. So, what is going to happen for the phase error detector if you give sinusoidal signals, the phase error keeps on increasing in this direction and V_{PD} output which you are looking at over a period of time, you will see the V_{PD} output has a sinusoidal waveform.

Now, what is so important about this sinusoidal waveform? If you look at V_{PD} which is varying in the manner I have shown, then the average value of V_{PD} is equal to zero. So, for a stand-alone phase detector, if you have a frequency error at the input, the average value of the phase detector output over a given period of time is going to be zero. This makes sense also, just looking at the plot what you see here is that you are having the average value of V_{PD} as phase error keeps on increasing, you see from the top and bottom curves, the area under the curve is equal to zero.

Similarly, what is going to happen when you have a square wave? So, let us just take a look here. So, you have, let us say, S-R flip-flop based and this is R signal and then I have V signal,

maybe it may start with the same point but you can have this as a V signal. So, you will detect phase error, there is a very clear frequency error which you can see with respect to V signal. So, for the first cycle, you see there is no error, for the second cycle, you see the error between these two edges, for the third cycle you are going to see error, third, this and this both are actually going to give you DN signal and then you see error with respect to this. So, 1, 1, this is continued and then you see a lot of error. So, this error will keep on increasing and depending on the frequencies, what you will see is, for example, if f_R and f_V, they are different frequencies, then whatever ratio they have $\frac{f_R}{f_V}$, just for example, I am writing that ratio as follows:

$$\frac{f_R}{f_V} = \frac{m}{n}$$

$$\Longrightarrow nT_V = mT_R$$

where, T_R and T_V are clock periods for R and V signal respectively.

So, by writing this ratio $\frac{f_R}{f_V} = \frac{m}{n}$, what I have told you here is that $nT_V = mT_R$ and after that this is going to repeat and when you see this over n times T_V period or m times T_R period, you will see that you are actually spanning the whole curve. You will actually span this whole curve over a given period of time. That time is equal to nT_V or mT_R. So, as the phase error keeps on increasing, V_{PD} also keeps on changing and when you take the average of V_{PD} over a given period of time, what you will see that average is equal to zero.

So, it will not be able to detect large frequency error in any case, even if sometimes the frequency error may even be of the opposite sign. So, the problem here is, so, first just understand this particular part that because I have been using phase error detectors in the previous simple PLLs where I used to recover the frequency error also whichever we had. But here now I am saying the same phase error detector is not able to detect large frequency error.

So, you may see an ambiguity, but let me clear that. So, previously in the PLL where we use the phase error detector PD and loop filter with VCO, the loop filter was Type-II loop filter and so on. The PLL was Type-II PLL and in this particular case or the assumption we had that initially we had the frequency error, based on the frequency error, we will get V_{PD} and this V_{PD} output voltage gets filtered by control voltage and you recover the frequency error.

So, we have seen multiple cases where your phase error exceeds 2π, then also you recover or your phase error does not exceed 2π and then also you recover. So, all those things were happening in the closed loop. In the closed loop, if you have the loop filter with an integrator, you were able to do so but stand-alone if you look at the PD, average value of this PD will not be the same, will not tell you about the frequency error and the actual reason is the frequency error is large, you will span this whole stuff and the average value gives you zero. So, that is the thing. So, what we are looking here is, is there a block which can give me the correct frequency error value so that I can detect the frequency error and correct for it as soon as possible.

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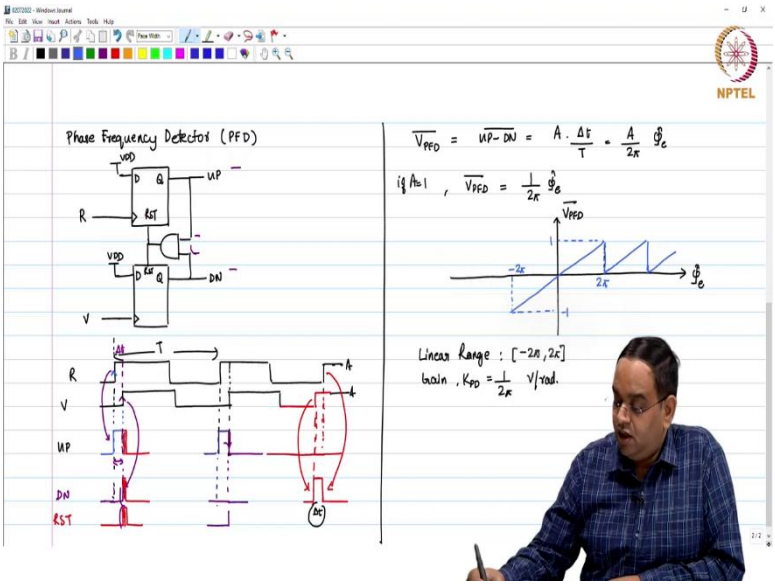

So, we have a block called as phase frequency detector. We will see what it does which the other blocks were not doing. It is abbreviated as PFD. It is typically made up of 2 D flip-flops. You can always design it using some other digital circuit also but you will see that it can simply be designed using 2 D flip-flops. The input D of both the flip-flops is connected to VDD, the supply voltage. The Q of both the flip-flops act as output for the PFD and one of these is clocked by R signal, and the other is clocked by V signal and the two Q signals are actually used to reset the two flip-flops using an AND gate.

So, you have a reset here, I will just write reset here and these two signals are called as UP and DN signals. You are a little bit familiar with UP and DN signals from the S-R based PD. So, let us look at the operation of this. So, I have my R signal like this, first look at the phase error detector operation. I have the R signal like this and the V signal slightly shifted from here just

to show you how it will detect the phase error and in this case right now, I am assuming that the frequencies are the same and the phase error is different.

We will look for the frequency error in a moment. So, do not worry about that part. So, this is R signal, this is V signal. Assume that before $t = 0$, all the outputs were actually 0. So, what happens when you get the rising edge on R? What happens is that the UP signal goes high, the DN remains low, there is no change in the DN signal. So, rising edge on R signal makes the UP signal go high, rising edge on V actually triggers a rising edge on DN signal. So, there will be a rising edge on DN signal.

Now, as you see, UP was already high and DN also goes high, so, both the inputs of the AND gate are high now. Because they both are high, the reset signal goes high. So, as soon as the UP and DN signals go high, the reset signal goes high, and if reset signal goes high, then you can say that both UP and DN will be brought to 0.

In real circuit, there is some time lag from DN signal going high to reset signal going high and then reset signal going high to UP and DN signals going low. So, right now, I am just putting all of that time duration as reset signal going low, so, within this time you can see that the DN signal will go low and the UP signal will also go low. Right now, this particular delay is very small, you can just neglect it. I deliberately did not make this as that DN remains low and UP also comes low.

So, one exaggeration for this can be, I will show you on the other edge that the UP signal goes high here, and as soon as I get the rising edge on the V signal, the DN signal remains low and UP signal also comes low. This is the exaggeration that as soon as you get the rising edge on V, the DN signal goes high and because the DN signal goes high and UP was already high, so, UP and DN will both make reset go high and reset signal will reset the outputs of the two D flip-flops. So, actually the UP signal will come down. So, this is like everything happens at the same instant. Here, I am showing that there is some kind of delay associated with it, and the actual phase error information is in this part only.

So, now you look at $UP - DN$. $UP - DN$ is high only during the time of the phase error. So, this is Δt. So, if I want to write the average of the PFD output, I will get,

$$\overline{V_{PFD}} = \overline{UP - DN}$$

If the amplitude which I am using for the voltage happens to be A, just an amplitude, then it is going to be,

$$\overline{V_{PFD}} = A.\frac{\Delta t}{T} = \frac{A}{2\pi}\varphi_e$$

$$\text{If } A = 1, \overline{V_{PFD}} = \frac{1}{2\pi}\varphi_e$$

What happens if the phase error is negative? Well, let us just make some change here. Let us say the V signal goes high, then in this particular case, the DN signal will go high first and the UP signal will already be low and that will remain low and DN signal will go low as soon as the R signal goes high.

So, this rising edge on V triggers the DN signal and rising edge on R triggers UP signal making it to go low. So here, on both the sides, if you are having this Δt, then for this particular error, you will get the average value as negative. So, if you look at the phase error detector characteristics, this is phase error and this happens to be $\overline{V_{PFD}}$. So, from -2π to 2π, it is a straight line, this is 2π, this is -2π.

The gain, K_{PD}, in our case with amplitude 1, is given by,

$$K_{PD} = \frac{1}{2\pi} \text{ V/rad}$$

So, this is the first phase error detector where you see it is linear across the zero phase error. So, as a phase error detector, the linear range is $[-2\pi, 2\pi]$ for phase error and the gain $K_{PD} = \frac{1}{2\pi}$ V/rad.

Now, what happens when the phase error is more than 2π with respect to your reference clock. If it happens to be that the phase error is greater than 2π, you will find that it will always go like this. How? Let us just look at it.

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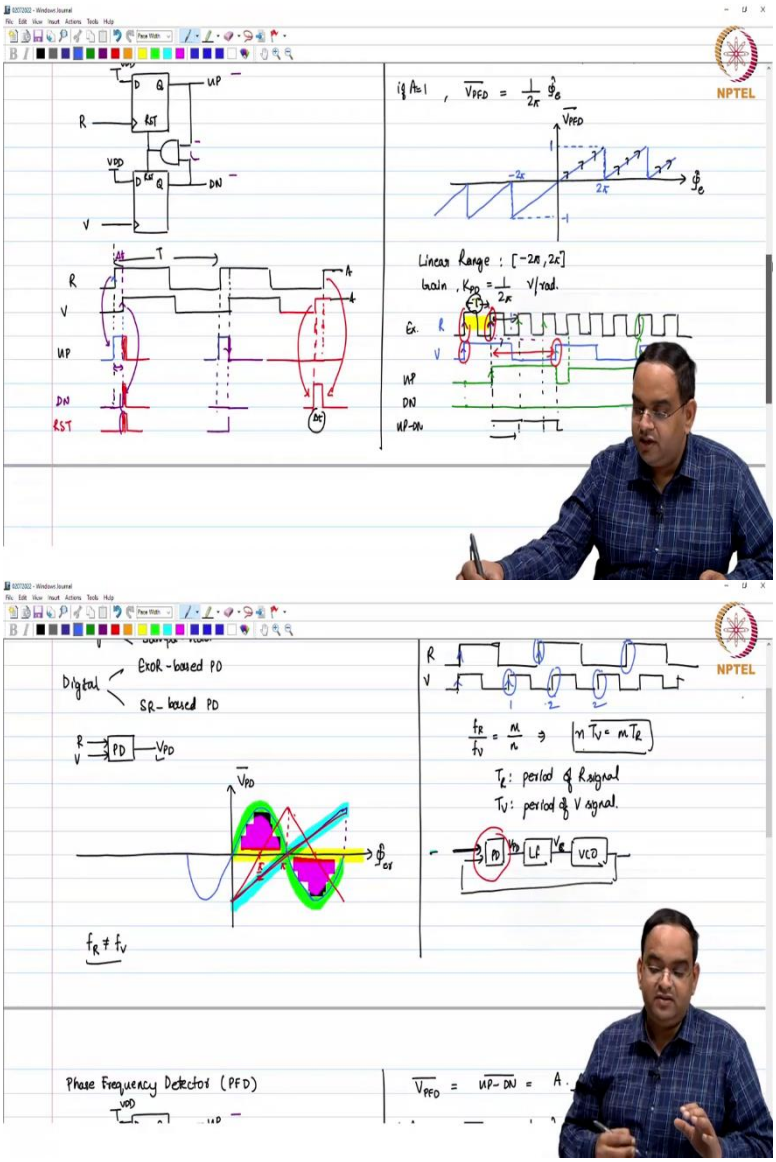

So, for an example, let us consider that your reference clock period is, you can choose either way, and this is my R signal and my V signal happens to be, let us say start with the same point, but this happens to be something like this. So, here I am taking this as 1.75, so, I should make it like this, let us do it this way. So, it is just an example which I am having.

So, in this case what you see is, initially you see both UP and DN, R and V both you get the rising edge at the same time. Then UP signal and DN signal, so, what is going to happen when you get your rising edge? So, first when you have rising edge on R and rising edge on V both, you can think ideally both the flip flops' output will go to 1 and then they will both go to 0, because the reset will get active, both are going to be like that.

Then as soon as you get a rising edge on R, this goes high, and you do not have a rising edge on V yet, so your UP will be maintained, DN will keep 0. Then you get another rising edge on R, well, even if you get another rising edge on R, it does not make any difference. UP still remains high, you get another rising edge, still remains high and then you get a rising edge on V. So, when you get the rising edge on V, what happens? The UP will go down and then at the very next rising edge on R, you again increase this and then at this particular point, it depends whether they both come at the same time or if the V signal is slightly before the rising edge on UP signal, then this will go down.

So here, if you think about it, the phase error which you are measuring at any given instant of time, for phase error, one thing is we are measuring the phase error with respect to the reference clock period. So, as I told you, you are always measuring the phase error with respect to the reference clock period. So, in first reference clock period, you see that the error is zero because they both are aligned. And then, if you look at the second rising edge on R, with respect to the second rising edge on R, in this whole period, you do not find a rising edge on V. So, the error between the two rising edges, if I look at it, between the two rising edges when you get this one and when you get here, this is like two and a half clock periods at T_V, this is the phase error.

So, $UP - DN$ signal, if you just think about it, $UP - DN$ signal, the average value here for this clock cycle, $UP - DN$, it remains 1, it still remains 1 during the next and then it goes to 1 and then after that it goes to 0. So, the phase error between these two signals where you actually see the frequency error, the phase error is actually larger than 2π, larger than 2π phase error here means larger than T_{period}, but the average value of $UP - DN$, $UP - DN$ is high for a longer time, but, if you look at the average value for each period, it is no more greater than the maximum value which you have from this PFD.

So, the frequency error is large, the phase error is as shown here, the average value of PFD output is still limited between -1 to 1 depending on whether you have a positive frequency error or a negative frequency error. So, in this particular case, $f_R > f_V$. So, you can say, the reference accumulates phase faster than the V signal.

So here, you will see that if you start from here, you will start changing the average value. If you are looking for the average value of V_{PFD} at every clock cycle, it will keep on increasing depending on what frequency error you have and then at one point it will reset and then again it will keep on increasing.

So, this happens to be in a periodic manner. The nice thing about this is that if the frequency error is positive, it will always remain positive, if the frequency error is negative, it will always remain negative. So, for a positive frequency error, when the phase error is increasing in one direction itself, the average value of the phase detector output is not equal to 0 unlike the previous case.

Here, the phase error will keep on increasing in one direction and then the average value of V_{PD}, average value of phase detector output will be equal to 0, that does not happen here. So, it is useful for us to employ this as a PFD and do not worry about it, whether the phase detector will detect the frequency error in the given time and correct and the PLL will lock. Well, those problems do not arise here.

So here, what you see is, you employ this PFD in your PLL loop, it will detect the frequency error and change the frequency in the correct direction always. So, that is about the phase frequency detector.

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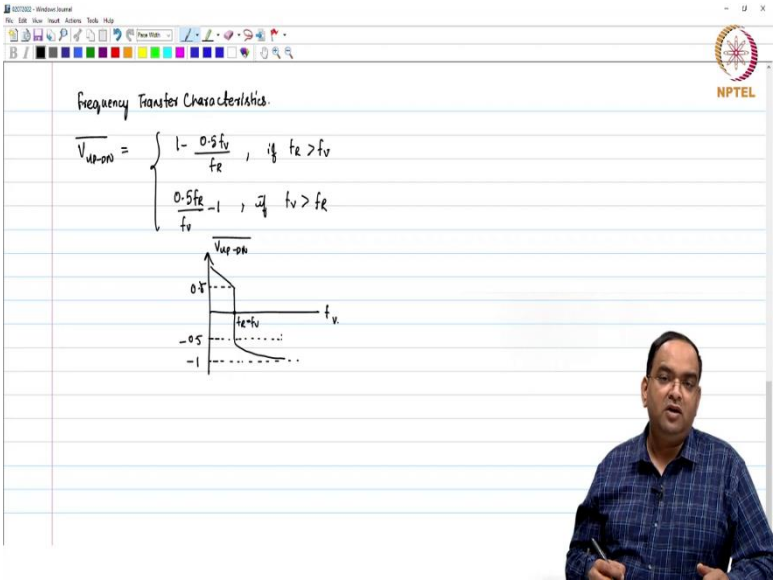

Now, you may ask me the transfer function as a frequency detector. So, what I have shown you as an average of the PFD output, now, if I just want to use it as a frequency detector, well, you can use it simply as a frequency detector and then it has frequency transfer characteristics, let me just write it. Well, it comes after some good amount of math. So, I will skip the math here, I will just show you what kind of frequency transfer characteristics the PFD has.

So, we have,

$$\overline{V_{UP-DN}} = \begin{cases} 1 - \dfrac{0.5 f_V}{f_R}, if\ f_R > f_V \\ \dfrac{0.5 f_R}{f_V} - 1, if\ f_V > f_R \end{cases}$$

One thing is you will see that it is not symmetric around the frequency error 0. Well, that is fine, at least it is detecting the correct sign of the frequency error, that is more important.

So, if I just plot this, what you will see is, when there is no frequency error, the value is actually 0.5. So, what I am plotting here is $\overline{V_{UP-DN}}$ with respect to the frequency f_V here. So, f_R is the reference which is fixed and this particular value asymptotically reaches to -1. At this node, you have $f_R = f_V$.

So, well, you may not use these transfer characteristics in your PLL. But the only thing which it is telling you is that if I use this PFD, I will detect the sign of the frequency error correctly, I will apply the correct change to the VCO's frequency all the time and I will acquire the frequency locking also.