

**Phase-Locked Loops**  
**Dr. Saurabh Saxena**  
**Department of Electrical Engineering**  
**Indian Institute of Technology, Madras**

**Lecture – 19**  
**Digital Phase Error Detectors: Part I**

(Refer Slide Time: 0:15)

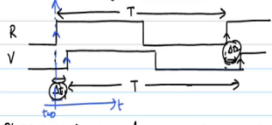
Phase Detectors (PD)

Analog PD

- Mixer based PD
- Sample & Hold PD

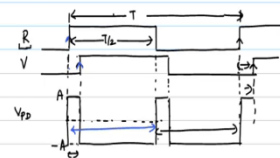
Digital PD

1. Exclusive-OR (EXOR) based PD



Phase error is measured with a reference clock. Here, the reference clock is R with time-period T.

$$f_{REF} = \frac{1}{T}$$

$$\phi_{ex} = 2\pi \frac{\Delta t}{T} \checkmark$$


$$V_{PD} = \frac{A \cdot \Delta t - A \left( \frac{T}{2} - \Delta t \right)}{T/2} = \frac{A \left( 2 \cdot \Delta t - \frac{T}{2} \right)}{T/2}$$

$$= A \left( 4 \frac{\Delta t}{T} - 1 \right)$$

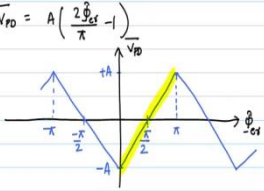
$$= A \left( 4 \frac{\phi_{ex}}{2\pi} - 1 \right)$$

Here, the reference clock is R with time-period T.

$$f_{REF} = \frac{1}{T}$$

$$\phi_{ex} = 2\pi \frac{\Delta t}{T} \checkmark$$

$$V_{PD} = A \left( 4 \frac{\phi_{ex}}{2\pi} - 1 \right)$$

$$= A \left( \frac{2\phi_{ex}}{\pi} - 1 \right)$$


Hello everyone. Welcome to this session on phase detectors. So, earlier we have looked at analog phase error detectors and out of those analog phase error detectors, we looked at two in particular. The first one was mixer or multiplier based PD and the other one was sample and hold based PD. So, one of the things which we found in these cases is that the mixer output was non-linear.

Now, we are going to look at digital phase error detectors and when I say digital phase error detectors, well, these phase error detectors are going to operate on digital signals or you can say CMOS signals which have two output levels, logic level zero and one.

So, the first one here is Exclusive-OR based PD which is also called as EXOR based phase detector. So, this is Exclusive-OR based PD. Now, let me first talk about what do we mean by phase error when we are having two square wave signals. This is something which we also saw in the last session. So, if you have two clock waveforms which are square waves and which look like this, so, this is R waveform and then let us say, I have V waveform, where both of them have the same output levels as shown to you here. The rising edges of the two clock waveforms differ by some value, let us call this as  $\Delta t_1$  and this one is  $\Delta t_2$ .

If the time period of both the clocks are same, then the timing error  $\Delta t_1$  and  $\Delta t_2$  are going to be the same. So, this is the time period, this is  $\Delta t_2$ . So here, we need to understand a couple of things. The first thing is that the phase error is always measured with respect to a reference clock, and in our case, that reference clock is here, the reference clock is R.

Why is it important to say that? Because phase is a dimensionless quantity and in order to define the phase, you need to know the time period. So, the time period which I am going to use is for the R clock. Here the reference clock is R with time period T. It may happen that the clock V may or may not have the same time period as R. So, for reference R, I can write,

$$f_{REF} = \frac{1}{T}$$

Now, the phase error here is defined as the timing error between the rising edges of the two clocks. So, let us say, you start with time instant  $t = 0$ . So, this is  $t = 0$  with respect to time. So, what you see here is that the error between these two rising edges is  $\Delta t$ . The phase error will be defined as,

$$\varphi_{er} = 2\pi \cdot \frac{\Delta t}{T}$$

If the two clocks have the same frequency, then this  $\Delta t$  will remain same at every rising edge of R. So, here also  $\Delta t$ , here also  $\Delta t$ , all these timing errors are going to be same.

So, when we are detecting the phase error for square wave signals using some circuit, at that particular time, we want the output of the phase error detector to be proportional to this  $\Delta t$ . So now, what is this Exclusive-OR gate? You have an EXOR gate, it is as simple as that and the output of the EXOR gate is the output of the phase error detector,  $V_{PD}$ . This is R and this is V.

Now you will remember how simple it is. So here, at both the rising edges, we are going to see  $V_{PD}$  like this. So, when you have one as logic high, and the other as logic low, the output logic will be high here. When both are logic high, the output will be low. Deliberately, I am showing you signal like this, like it has the EXOR gate. In this particular example, you can say the high value of the EXOR gate is A and the low value of the EXOR gate is -A. This is the  $V_{PD}$  output. You can very well have A and 0, just for this case, for this analysis, you will find it is quite easy with A and -A.

Then, you see that again there is a change of sign, change of output. So, this is A and then this is again going to be zero here and this will repeat if you are having the same frequency. So, interestingly what you see here is that if both R and V are having the same frequency, then this  $\Delta t$  is going to be the same for all the clock periods. The interesting part here is that this pulse actually repeats after every  $\frac{T}{2}$ . So, this time period is  $T$  and the other one is  $\frac{T}{2}$ . I can assume that this is  $\frac{T}{2}$  if I say that the duty cycle of the clock is 50%. Now, for this particular EXOR gate, you see that the  $V_{PD}$  output is having a pulse kind of waveform and it is changing at the rate of the reference.

So here, we define the average value of  $V_{PD}$  for the reasons which we discussed earlier. So, the average value of  $V_{PD}$  is given by,

$$\overline{V_{PD}} = \frac{A \cdot \Delta t - A \left( \frac{T}{2} - \Delta t \right)}{\frac{T}{2}}$$

This average value is taken over  $\frac{T}{2}$ . You want you can take it over  $T$  also, just that you will have to entertain this pulse also. Since it is periodic, whether I take an average over  $T$  or  $\frac{T}{2}$ , they both are going to be the same.

$$\overline{V_{PD}} = \frac{A \left( 2 \cdot \Delta t - \frac{T}{2} \right)}{\frac{T}{2}}$$

$$\overline{V_{PD}} = A \left( 4 \cdot \frac{\Delta t}{T} - 1 \right)$$

Now, in this case, I will just change from  $\Delta t$  to  $\varphi_{er}$  using the relationship  $\varphi_{er} = 2\pi \cdot \frac{\Delta t}{T}$ . So, this can be written as,

$$\overline{V_{PD}} = A \left( 4 \cdot \frac{\varphi_{er}}{2\pi} - 1 \right)$$

$$\overline{V_{PD}} = A \left( \frac{2 \varphi_{er}}{\pi} - 1 \right)$$

So, for the EXOR based phase error detector, what you see is that  $\overline{V_{PD}} = A \left( \frac{2 \varphi_{er}}{\pi} - 1 \right)$ . Let us just plot this.

So here, I am going to plot the average of the phase error detector output with respect to phase error. So, when phase error is equal to zero, you will have value of  $-A$  and when phase error is equal to  $\pi$ , you will have  $A$ , and then in between you will go from  $-A$  to  $A$ . This is  $\pi$  and this is  $\frac{\pi}{2}$ , and as the phase error increases more than  $\pi$ , you will see it will go like this.

On the opposite side or you can say for the negative phase error, what happens is that you are going to see like this, this is going to be  $-\frac{\pi}{2}$  and this will be  $-\pi$ . So now, if you look at this average of the phase error detector characteristic, it is showing you a linear response from phase error of zero to  $\pi$ .

If you talk about EXOR gate independently, the EXOR gate independently is non-linear. It has only two output levels. In terms of voltages, it is non-linear, but if you are using in the manner as I have shown here, then you see that the phase error detector behaves in a linear fashion in the range zero to  $\pi$ .

(Refer Slide Time: 12:54)

$$V_{PD} = A \left( \frac{2\phi_{err}}{\pi} - 1 \right)$$

Linear Range:  $\pm \pi/2$   
 Gain of PD,  $K_{PD} = \frac{2A}{\pi} = \frac{2}{\pi} A \text{ V/rad}$

**Phase Detectors (PD)**  
**Analog PD**  
 - Mixer based PD  
 - Sample & Hold PD  
**Digital PD**  
 1. Exclusive-OR (EXOR) based PD

Phase error is measured with a reference clock.  
 Here, the reference clock is R with time-period T.  
 $f_{ref} = \frac{1}{T}$   
 $\phi_{err} = \frac{2\pi \Delta t}{T}$

$$V_{PD} = \frac{A \cdot \Delta t - A \left( \frac{T}{2} - \Delta t \right)}{T/2} = A \left( \frac{4 \Delta t}{T} - 1 \right) = A \left( \frac{4 \phi_{err}}{2\pi} - 1 \right) = A \left( \frac{2 \phi_{err}}{\pi} - 1 \right)$$

If I am going to add this particular phase error detector in the PLL, just for an example. So, you take this phase error detector, you feed both the reference and the output signal, and then you have the loop filter and VCO. Then, in that particular case, you will see this is the  $V_{PD}$  output.

If the loop filter happens to be Type-II, you will lock to the average value of the phase error detector as zero. This is because for Type-II loop filter, you have an integrator, you have to have in the locked state, the average phase detector value as zero which means your locking point is going to be phase error of  $\frac{\pi}{2}$ . Locking to a phase error is not a problem in PLL. The only thing is that if the PLL is locked, the phase error should not change with respect to time, that is important.

So, what you see is that this particular phase error behaves linearly here. So, quite often we use a change in variable here where we just shift this plot and in place of having our axis at phase error of zero, I change the variable, and now I have this as  $\overline{V_{PD}}$  and this is the change in the variable. Now it is no more called as phase error, but it is  $\varphi_{er}^s$ , the shifted one.

What is the importance of this? Well, so what I have done here is that the phase error  $\frac{\pi}{2}$  will effectively become zero, so I need to change this. This is zero here, this is  $\frac{\pi}{2}$  and this one is  $-\frac{\pi}{2}$ . I am just changing the axis and this becomes  $-\pi$ , this is  $-\frac{3\pi}{2}$  and so on. So, the change in variable which you are looking here is that previously whatever was  $\frac{\pi}{2}$ , that has become zero now. So, the change in the variable which I am using is,

$$\varphi_{er}^s = \varphi_{er} - \frac{\pi}{2}$$

This is the change in the variable I applied and then I plotted  $\overline{V_{PD}}$  with respect to  $\varphi_{er}^s$ . So, what you see here is that  $\frac{\pi}{2}$  translates to zero and  $\pi$  translates to  $\frac{\pi}{2}$  and this one translates to this point. Well, other than the ease of looking at this phase error detector, there is nothing much which we did.

So, coming back to the phase error detector output, what we see here is that the EXOR based phase error detector is linear, it is not only monotonous. It is linear in range  $\pm \frac{\pi}{2}$ . In contrast to the mixer based PD and the sample and hold based PD, the range for the EXOR based PD is actually perfectly linear.

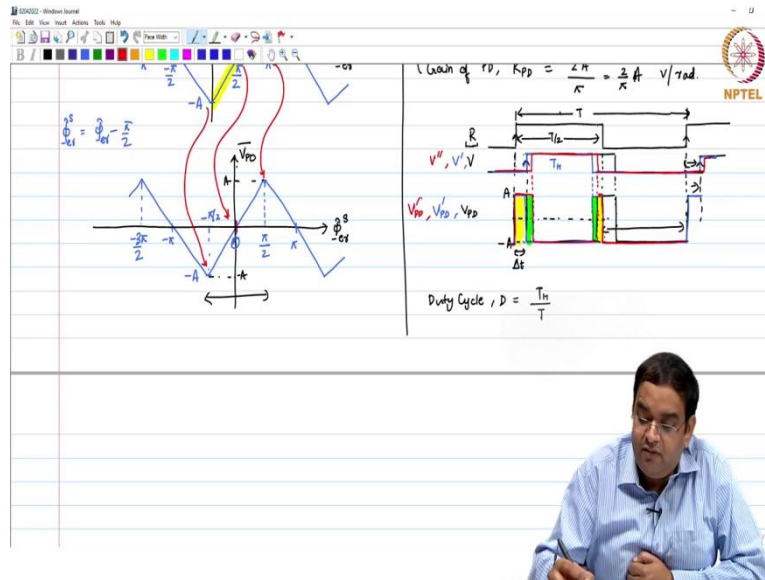
To find the gain of the phase error detector which is  $K_{PD}$ , now, this is just like finding the slope of a line which is not any different. So, it is given by,

$$K_{PD} = \frac{2A}{\pi} = \frac{2}{\pi} A \text{ V/rad}$$

So, the things which we look for are the linear range and the gain of the phase error detector. So, what you see here is that the gain is constant throughout this range. The gain is constant and you have a linear range. So, in contrast to the mixer based PD where you had gain as non-linear and there was no linear range, it was like a monotonous range which we had, this PD appears to be much better.

So, here we perform better on both the counts. Now, given this phase error detector and our analysis, actually when you go and implement, there is some inherent problem to this phase error detector. So, let us just look at it.

(Refer Slide Time: 18:31)



So, what happens if the clock has a duty cycle error? So, let us say the reference clock is pretty good and it has no issues, the problem is actually with the V clock which is generated by the oscillator. So, if that is the case, I will just show you one case where I have a duty cycle error. I am plotting a modified V and this modified V happens to be like this. So, in place of having a high time of  $\frac{T}{2}$ , it has a high time of  $T_H$ . I will just write this as  $V'$ . What happens if you have high time of  $T_H$ ? Well, the actual phase error is between these rising edges which still remains  $T$ .

But what are you going to see at the output of the phase error detector? This is fine and then depending on the duty cycle of the clock, so here you see this is high and this is low. So, you are going to get high for this region. So, I am plotting this for  $V'$ , this is  $V_{PD}'$ . When I am plotting on the same curve, it may be easier for you to recognize. So, this is the duty cycle error which you see. What is duty cycle? Duty cycle of the clock is defined as,

$$D = \frac{T_H}{T}$$

Now, for example, if the phase error changes by a small amount, let us say, and the duty cycle remains the same. So, you see that the output will be like this. Now it is going to be periodic

in  $T$  rather than  $\frac{T}{2}$ . So, I have shown you another waveform, let us call that  $V''$ . In response to  $V''$ , you are going to see  $V''_{PD}$  like this. So, the interesting part here is that even when the phase error changed from blue to the red one, you see that the total area for which the clock is high still remains the same. The total area which was earlier for the blue one was this, and to calculate the area when it changes to the red one, to yellow, you add this green here and on the other side, you deduct this green, what you will find here is that the total area for which the clock is high still remains the same. It very much depends on the phase error.

(Refer Slide Time: 22:44)

$\bar{V}_{PD} = -2DA$   
 For  $(\frac{T}{2} - DT) \leq \Delta t \leq \frac{T}{2}$   
 $\bar{V}_{PD} = -2A [1 - D - 2\frac{\Delta t}{T}]$   
 PLL will lock for  $\bar{V}_{PD} = 0$   
 $1 - D - 2\frac{\Delta t}{T} = 0 \Rightarrow \Delta t = \frac{T}{2}(1 - D)$   
 Corlier,  $D = \frac{1}{2} \Rightarrow \Delta t = \frac{T}{2}(1 - \frac{1}{2}) = \frac{T}{4} \frac{\Delta \phi}{\frac{\pi}{2}}$

$K_{PD} = \frac{2A}{\pi} \text{ rad/V} = \frac{2 \cdot A \cdot F}{2 \cdot \pi \cdot F}$

$\bar{V}_{PD} = A \left( \frac{2\phi_{err}}{\pi} - 1 \right)$

Linear Range:  $\pm \pi/2$   
 Gain of PD,  $K_{PD} = \frac{2A}{\pi} = \frac{2 \cdot A \cdot F}{\text{rad}}$

Duty Cycle,  $D = \frac{T_{in}}{T}$



In the presence of phase error.  $\phi_{er}' = 2\pi \frac{\Delta t_1}{T}$  and  $\phi_{er}'' = 2\pi \frac{\Delta t_2}{T}$ ,  $\bar{V}_{PD} = \bar{V}_{PD}''$

Linear Range:  $[-\pi(1-2D), \pi]$

For  $0 \leq \Delta t \leq (\frac{T}{2} - DT)$   
 $\bar{V}_{PD} = -2DA$

For  $(\frac{T}{2} - DT) \leq \Delta t \leq \frac{T}{2}$   
 $\bar{V}_{PD} = -2A [1 - D - 2\frac{\Delta t}{T}]$

PLL will lock for  $\bar{V}_{PD} = 0$

$K_{pp} = \frac{2A}{\kappa} \text{ rad/V} = \frac{A \cdot \pi}{2\kappa \pi}$

In the presence of phase error.  $\phi_{er}' = 2\pi \frac{\Delta t_1}{T}$  and  $\phi_{er}'' = 2\pi \frac{\Delta t_2}{T}$ ,  $\bar{V}_{PD} = \bar{V}_{PD}''$

Linear Range:  $\pm \pi/2$

Gain of PD,  $K_{pp} = \frac{2A}{\kappa} = \frac{2}{\kappa} A \text{ V/rad}$

Duty Cycle,  $D = \frac{T_n}{T}$

So, the point is the following. In the presence of phase error, we will calculate with equations later, but just first understand what is happening. So, here actually you have two phase errors. In the presence of the first phase error, we have,

$$\phi_{er}' = 2\pi \frac{\Delta t_1}{T}$$

In the presence of the second phase error, we have,

$$\phi_{er}'' = 2\pi \frac{\Delta t_2}{T}$$

Do not think this double dash is a derivative, I am just using this for different signs. Also, the average of  $V_{PD}'$  is same as the average of  $V_{PD}''$ .

$$\overline{V'_{PD}} = \overline{V''_{PD}}$$

You can easily relate to this by looking at the area under the curve when the output is high and when the output is low.

So, this is going to happen. It will change when the phase error exceeds such that the high time actually crosses this, that time it will change, till the time it remains within the  $\frac{T}{2}$  region it is going to be same. So, just another visualization for that. So, this is the high time for R clock. So, if you have something like this, this is  $T_H$ , this is, you can say,  $\frac{T}{2} - T_H$ .

Whether you have V as this or you just shift the clock and have some phase error like this or you have another one where you shift the clock, you have more phase error, it becomes like this. The area is going to be same for  $V_{PD}$ .

It is going to change only when, you can say, after a point where it becomes like this, if the phase error exceeds from this value. What is this value? Well, this value is nothing but  $\frac{T}{2} - T_H$ . If the phase error exceeds this value, then only you are going to see a change in  $V_{PD}$  output. So, based on this, we can actually plot the average of the phase error detector and the average of the phase error detector happens to be, so, let us say, this is -A and this happens to be A. This is phase error, this is  $\overline{V_{PD}}$ . So, this is going to be constant for some time and then it will change and it is again going to be constant on the other side for a while. This value is not going to cross zero at  $\frac{\pi}{2}$ . At  $\frac{\pi}{2}$ , it is going to be some other value, by the way, this is  $\pi$ .

As the phase error exceeds  $\pi$ , you will again see the constant part. This value happens to be -2DA and on the positive side, this is 2DA, and this offset point is actually  $\pi(1 - 2D)$ . So, what you see here is that in place of  $\overline{V_{PD}}$  reaching -A and A, it gets fixed at two different points, which are -2DA and 2DA.

Interestingly, the gain during this region still remains the same as what you had previously. What was the gain? The gain is given by,

$$K_{PD} = \frac{4DA}{2\pi D} = \frac{2A}{\pi} \text{ V/rad}$$

So, the gain remains the same while the linear range actually reduces. Now, the linear range is going from  $\pi(1 - 2D)$  to  $\pi$ , that is our range. You can again shift this plot back to this plot

wherever you find that the phase error is equal to zero. During this time, you have the phase error equation given by,

$$\text{For } 0 \leq \Delta t \leq \left(\frac{T}{2} - DT\right), \overline{V_{PD}} = -2DA$$

$$\text{For } \left(\frac{T}{2} - DT\right) \leq \Delta t \leq \frac{T}{2}, \overline{V_{PD}} = -2A \left[1 - D - 2\frac{\Delta t}{T}\right]$$

where, D is the duty cycle which is  $\frac{T_H}{T}$ .

You can substitute in this equation, and you can find the values accordingly. So, your PLL is not going to lock to  $\frac{\pi}{2}$ . If the frequencies are same, the PLL will lock for  $\overline{V_{PD}} = 0$ . This implies the following:

$$1 - D - 2\frac{\Delta t}{T} = 0$$

$$\Rightarrow \Delta t = \frac{T}{2}(1 - D)$$

If you want to do a sanity check, in the previous case, we had,

$$D = \frac{1}{2}$$

$$\Rightarrow \Delta t = \frac{T}{2}\left(1 - \frac{1}{2}\right) = \frac{T}{4} \xrightarrow{\varphi_{er}} \frac{\pi}{2}$$

This translates to a phase error of  $\frac{\pi}{2}$ . This was the locking point earlier, and now the locking point has just shifted but that is fine. So, because of the duty cycle, we have a problem that the phase error is not linear throughout the range zero to  $\pi$  or earlier like  $-\frac{\pi}{2}$  to  $\frac{\pi}{2}$ , that range has reduced. But what has happened is that though the range has reduced, the gain remains the same and the gain is constant in the reduced range.