

**Introduction to Semiconductor Devices**  
**Prof. Dr. Naresh Kumar Emani**  
**Indian Institute of Technology, Hyderabad**

**Lecture - 61**  
**MOSFET Device Metrics**

This document is intended to accompany the lecture videos of the course "Introduction to Semiconductor Devices" offered by Dr. Naresh Emani on the NPTEL platform. It has been our effort to remove ambiguities and make the document readable. However, there may be some inadvertent errors. The reader is advised to refer to the original lecture video if he/she needs any clarification.

Hello everyone. Welcome back to introduction to semiconductor devices. So, in the last couple of lectures we have understood how a MOSFET functions and we have also derived the current voltage characteristics for a MOSFET. So, we have seen that a MOSFET if you look at the vertical direction in the sense if you look at the gate oxide and the semiconductor it is essentially a mos capacitor.

So, we have studied the electrostatics and you know of mos capacitor in great depth. And then in the lateral direction from source to the drain it is essentially two p n diodes which are back to back. So, we have seen how there is a barrier formed across a channel and because of which current will not conduct and that barrier can be changed by applying a gate voltage. So, this is essential physics of the MOSFET. So, today we would like to understand what makes a good MOSFET.

**What is a 'good' MOSFET?**

The slide includes the following components:

- NMOS Diagram:** Shows a cross-section of an NMOS transistor with gate voltage  $V_{GS} (0 \rightarrow V_{DD})$  and drain-source voltage  $V_{DS} (0 \rightarrow V_{DD})$ . A handwritten note indicates  $V_{DS}$  is the supply voltage.
- PMOS Diagram:** Shows a cross-section of a PMOS transistor with gate voltage  $V_{GS} (0 \rightarrow V_{DD})$  and drain-source voltage  $V_{DS} (0 \rightarrow -V_{DD})$ . Handwritten notes specify  $V_{GS} = -V_{DD}$  and  $V_{DS} = 0$ .
- Output Characteristics Graph:** Plots drain current  $I_D$  versus drain-source voltage  $V_{DS}$  for various gate-source voltages  $V_{GS}$ . It shows a linear region and a saturation region. Handwritten notes include "Fix  $V_{GS}$ , sweep  $V_{DS}$ " and "linear  $V_{GS} = V_{DS}$ ".
- Transfer Characteristics Graph:** Plots drain current  $I_D$  versus gate-source voltage  $V_{GS}$ . It shows a subthreshold region, a linear region, and a saturation region. Handwritten notes include "Fix  $V_{DS}$ , sweeping  $V_{GS}$ ", "linear  $V_{GS} = 50 \text{ mV}$ ", and "saturation  $V_{GS} = V_{DS}$ ".
- NPTEL Logo:** Located in the top right corner.
- Speaker:** A small video inset of the professor in the bottom right corner.
- Footer:** "EE @ IIT Hyderabad" is written at the bottom.

So, MOSFETs are used in wide range of applications. And to understand what is a good MOSFET? We need to examine its current voltage characteristics in great detail. So, to start with; so what you are seeing here is basically a symbol you know circuit symbol for a MOSFET. This is one of the symbols so this is on the left it is an NMOS device on the right it is a PMOS device. These are one of the representations.

You know there are multiple representations if you look at different textbooks will have different notations. But you can refer and then compare that. So, when you have a MOSFET there are two types of  $i_v$  characteristics that we are interested in which is so we have already seen you know that there are four terminals in a MOSFET. And I am only showing you three terminals here but there is always a bulk.

So, if you look at this particular picture there is a drain, there is a source and there is a gate. So, usually for n MOSFET we will ground the source and we can apply varying voltages on the drain and the gate. So, in this case voltages a changed in the range 0 to  $V_{DD}$ .  $V_{DD}$  is a commonly used notation for supply voltage. So, each technology has a different supply, it can have a different supply voltage.

For example, in the old TTL logic we used to have supply voltages as 5 volts and then that came down to 3.3 and then 1.8 and rather than 2, 3.3, 2.51 0.8 and 1. So, now nowadays it is usually around one. So, now what we are considering is you could sweep the drain voltage from 0 to  $V_{DD}$  or you could also sweep the gate voltage from 0 to  $V_{DD}$ .

So, when we do this, we get two types of characteristics. The first type is output characteristics which is essentially a function of a plot of drain voltage versus drain current. Sometimes we also call this as  $I_d V_d$  characteristics, drain current and drain voltage characteristics. And we have seen this in detail you know we fix a particular gate voltage and then sweep the drain voltage from 0 to the maximum.

So, while we do that, we saw that when the drain voltage is small your MOSFET is biased in linear region. And then as you cross  $V_{D SAT}$  which we said is equal to  $V_{GS} - V_T$ . If your drain voltage

is greater than  $V_{D SAT}$ , we said the current saturates. So, I have shown here two particular graphs. You know one is basically when your gate voltage is less than  $V_D$ , we do not expect current. The transistor is off so no current.

But then if you choose  $V_{GS} = V_{DD}$  you get a saturating current characteristic which is shown here. So, it is important to note that on the left of  $V_{D SAT}$  it is the linear region on the right it is saturation region. This is one type of characteristic which we call as output characteristics. There is also one more type of characteristics which we call as transfer characteristics.

In this case we will keep the drain voltage fixed and then sweep the gate voltage. So, when we do that, we can choose the drain voltage to be a small number like 50 to 100 millivolts and if we do that that MOSFET will be biased in the linear region. So, you get a linear transfer characteristic which is shown in the bottom here. And then you could also choose the drain voltage to be at supply voltage  $V_{DD}$ .

If we choose that then definitely the  $V_{DS}$  is going to be greater than  $V_{DSAT}$  and that is why the MOSFET will be biased in saturation. So, you get a  $I_d$  vs  $V_G$  curve. So, in transfer characteristic we are fixing  $V_{DS}$  and then sweeping  $V_{GS}$  gate voltage. In output we are fixing  $V_{GS}$  and then sweep  $V_{DS}$ .

So, these characteristics you know you can actually do the measurements at multiple  $V_{GS}$ s or  $V_{DS}$ s. So, then you get a family of curves where there will be a quadratic relation like this. Drain current is going to increase as your gate voltage increases the drain current increases and there is a quadratic behaviour in the saturation.

So, this is for an NMOS device you could also do it for a PMOS device. And we said the PMOS device is essentially a complementary device to NMOS. One thing to kindly note is in CMOS technology especially we tend to connect the source to the highest supply voltage highest voltage which is usually the supply voltage. So, source is connected to  $V_{DD}$  and then gate is swept from 0 to  $V_{DD}$  and drain can be swept from 0 to  $V_{DD}$ .

Why do we do this? One of the reasons is that we are using an n-type substrate we want to make sure that the source and the channel junction is always reverse biased. Similarly, the drain channel or drain bulk junction that is also reverse biased. So, since it is a n-type substrate we have connected to  $V_{DD}$  so it gets reverse biased. We do not want to accidentally forward biased the source channel or the drain channel junction that is one reason.

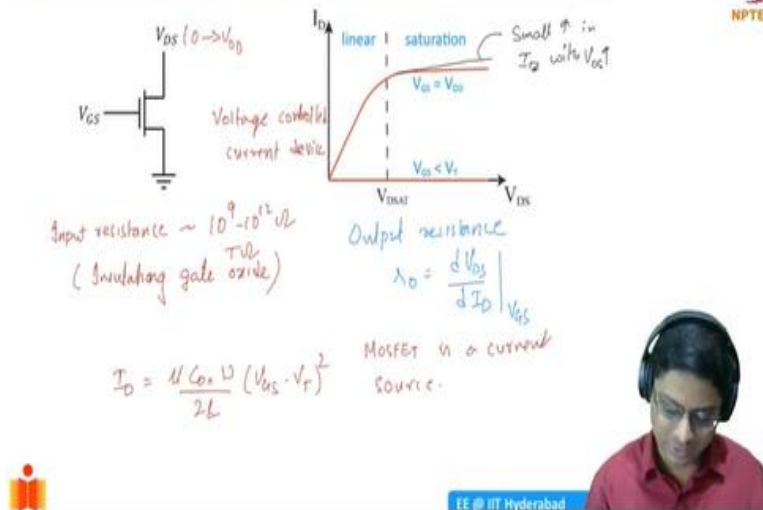
The other reason is it makes it very convenient. We said the gate voltages in the drain voltages for a PMOS device are exactly complementary. So, for NMOS device they were positive for a PMOS device they will be negative. If it is a well-designed PMOS and NMOS. So, this can be tuned by adjusting parameters like work function and doping and things like that. So, if you take a well-designed complementary PMOS device, what will be the  $V_{GS}$ ?

In the way that we have bias here.  $V_{GS}$  let us say is going to be if the gate voltage is 0 then it is going to be minus  $V_{DD}$ .

If we keep gate voltage as  $V_{DD}$  then  $V_{GS}$  is going to be 0. So, by tying the source to the  $V_{DD}$  we are essentially sweeping the gate voltage from 0 to  $-V_{DD}$ . Same thing happens to  $V_{DS}$  also. When  $V_{DD}$  is 0 then  $V_{DS}$  is  $-V_{DD}$  when  $V_D$  is  $V_{DD}$  then  $V_{DS}$  will be 0. So, we are essentially sweeping in the negative sense without actually having to create another voltage source.

Otherwise, you have to have one voltage source which is going from 0 to  $V_{DD}$  other one going from 0 to  $-V_{DD}$  and so on. So, we can avoid that. So, this is the way it is used in the CMOS devices. So, we can measure these characteristics for NMOS and PMOS devices. But what are the metrics that we need to look for when we think about a MOSFET?

## Input and Output Resistance



To understand that let us look at the drain characteristics. So, what we did here was we swept  $V_{DS}$  from 0 to  $V_{DD}$  and chose some  $V_{GS}$ . Initially  $V_{GS}$  is 0 and less than  $V_T$  and  $V_{GS}$  are  $V_{DD}$ . So, one of the important metrics in a mos device is the input resistance. How much will be the input resistance of the MOSFET?

So, MOSFET is a voltage controlled current device, because you are applying the gate voltage and you are controlling the current in the drain source nodes. So, what is the input resistance of a MOSFET? We said that the gate is actually having a metal and then there is an oxide which is separating and the oxide is an insulator. It is a very good insulator supposed to be a very good insulator.

So, usually the input resistance of a MOSFET will be typically  $10^9$  to  $10^{12}$  ohms or tera ohms range. It is a very good, it has a very high input resistance. So, usually it does not create a problem and this is because of an insulating gate oxide. So, it has a very high input resistance that means if you take another voltage source and apply voltage all of the voltage will fall across the MOSFET. You know another MOSFET could be driving it.

In that case as well most of the voltage will fall across the MOSFET in consideration. This is one of the parameters. The other important parameter is an output resistance. How do we define output resistance? Output resistance is defined as derivative of  $V_{DS}$  with respect to  $I_D$  that let us say

this could be at a particular  $V_{GS}$ . You fix a  $V_{GS}$  and then calculate the derivative and then you get the output resistance.

So, if you are in the linear region, drain voltage was low then you are in the linear region and there is a constant resistance. But usually, the MOSFETs are biased in saturation. In that case you see that the  $I_D$  is not changing very much for some change in  $V_{DS}$ . So, we can expect that the resistance is quite large.

It is actually high resistance because the current is changing by a very small amount for a large change in  $V_{DS}$ . So, it is like a current source, MOSFET behaves current source. What is the characteristic for current source? Irrespective of your load, it should supply the same amount of current and it does that when its output resistance is large.

So, you could also see that very small change in the drain current compared to large change in the  $V_{DS}$  that is why it is larger output resistance. But then what happens is this is for an ideal MOSFET in the square law theory. Once the MOSFET hits saturation it sort of remains constant current,  $I_D = \mu C_{ox} (W / 2L) (V_{gs} - V_T)^2$ .

We said the current remains at this value but it turns out that this is not quite true. There is some small change in the current, small increase in  $I_D$  with  $V_{DS}$  increase. So, this happens because of a short channel effect and is known as channel length modulation. And this channel length modulation becomes more and more significant in the short channel devices.

So, for now essentially what we are saying is there is this large output resistance and large input resistance, realistic devices have a finite output resistance. So, what are the applications that we can use MOSFETs?

## Drain and transconductance

$I_d(V_{gs} + v_{gs}, V_{ds} + v_{ds}) = I_d(V_{gs}, V_{ds}) + I_d$   
 $I_d(V_{gs}, V_{ds}) + \frac{\partial I_d}{\partial V_{gs}} \Big|_{V_{ds} \text{ const}} v_{gs} + \frac{\partial I_d}{\partial V_{ds}} \Big|_{V_{gs} \text{ const}} v_{ds}$

$I_d = \frac{\partial I_d}{\partial V_{gs}} \Big|_{V_{ds} \text{ const}} v_{gs} + \frac{\partial I_d}{\partial V_{ds}} \Big|_{V_{gs} \text{ const}} v_{ds}$

$I_d = \frac{\mu C_{ox} W}{2L} (V_{gs} - V_t)^2$   
 $g_{m, \text{sat}} = \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)$   
 $g_{o, \text{sat}} = \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)$

Linearly varies with  $V_{gs}$   
 Does not change with  $V_{ds}$

Linearly increases with  $V_{gs}$   
 Constant with  $V_{ds}$

EE @ IIT Hyderabad

So, we can use it in analog circuits and we can actually think of a small signal equivalent circuit in analog circuits. What we can do is let us say here there is this MOSFET and we applied a voltage  $V_{DS}$  and then gate voltage  $V_{GS}$ . So, you could have a drain current which is  $I_D$  which is essentially a function of  $V_{GS}$  and  $V_{DS}$ . So, you could fix this DC voltages and then you can get a DC current and then you can apply a very small signal on top of this DC.

For example,  $V_{DS}$  can be modulated by applying a small signal  $V_{ds}$ . Similarly, here I can apply a small AC signal of  $V_{ds}$ . So, we can say that

$$I_D(V_{DS} + V_{ds}, V_{GS} + V_{gs}) = I_D(V_{DS}, V_{GS}) + I_d(V_{ds}, V_{gs})$$

So, if this is a current, we can write this as essentially equal to  $I_D$  which is a DC operating condition operating current plus there is a small  $I_D$  which is AC drain current. We see drain current you have a DC operating point. So, essentially my AC is going to modulate my current, how much is this? This we can actually write out by Taylor series.

$$I_D(V_{GS}, V_{DS}) + \frac{\partial I_d}{\partial V_{gs}} \Big|_{V_{ds} \text{ const}} * V_{gs} + \frac{\partial I_d}{\partial V_{ds}} \Big|_{V_{gs} \text{ const}} * V_{ds}$$

$$\text{So, } I_d = \frac{\partial I_d}{\partial V_{gs}} \Big|_{V_{ds} \text{ const}} * V_{gs} + \frac{\partial I_d}{\partial V_{ds}} \Big|_{V_{gs} \text{ const}} * V_{ds}$$

So, this is a very interesting thing because whenever you have an AC voltage that is applied to either gate or drain the impact on the drain current can be calculated by knowing two parameters which are essentially derivatives of the IV characteristics these two parameters are very crucial. So, we it is called as trans conductance,  $g_m$  and the other term is output conductance,  $g_d$

We can find out how much is the output conductance. In small channel devices it is going to be some finite number. Trans conductance we can calculate by differentiating the current in linear region  $I_D$ .

$$I_D = \mu C_{ox} (W / 2L) (V_{gs} - V_T) V_{ds}$$
$$g_m = \mu C_{ox} (W / L) V_{ds}$$

So, here you see that the trans conductance is no function of you know this is linearly varies with  $V_{DS}$ , does not change with current. It does not change with  $V_{GD}$ . So, this is the linear trans conductance.

You could also have the saturation trans conductance.

$$I_D = \mu C_{ox} (W / 2L) (V_{gs} - V_T)^2$$
$$g_m = \mu C_{ox} (W / L) (V_{gs} - V_T)$$

So, here you see that this is linearly increases with  $V_{GS}$  and constant with respect to  $V_{DS}$ . MOSFETs, we use them for analog designs like OP AMPS you know and so on. But if you look at an OP-AMP inside an OP-AMP it is consisting of minimum there will be about nine transistors or it could have to go up to 27 transistors also.

You can actually have MOSFET circuits you design the OP-AMP like 741 that you use in your linear integrated circuits course would it can be designed using techniques.



# MOSFET in digital applications



Logic '0' - 0V  
Logic '1' -  $V_{DD}$

Switch Model

$V_{GS} > V_T$   $I_D = I_{ON} \left( \frac{V_{GS} - V_{GS}}{V_{GS} - V_{DD}} \right)^2$

$V_{GS} = 0$   $I_D = I_{OFF}$

$\frac{I_{ON}}{I_{OFF}}$  ratio  $\sim \frac{10^{-4} A}{10^{-10} A}$   
 $\sim 6$  orders

$I_D = J_s \left[ \exp\left(\frac{qV_G}{kT}\right) - 1 \right]$

IE @ IIT Hyderabad

MOSFETs are also used for digital applications. For example, your processors are it is a digital device digital processor because you have zeros and ones. You are not really concerned about how the voltage is changing continuously from 0 to  $V_{DD}$ . So, in digital circuits we refer to as logic 0 is basically 0 volts, logic 1 I can refer to as  $V_{DD}$ .

So, basically  $V_{DD}$  it could be in the modern technology it is about one volt or in the past it is 5 volts. So, if your voltage is 0 its logic 0 1 it is logic one. So, you can design digital circuits. So, because of the switching from 0 to 1 you are able to do this. A lot of processing all the digital circuits are essentially this, Boolean algebra we apply and then we design circuits like you know ANDs, NORs and so on. So, those are all digital circuits.

So, MOSFET is most predominantly used in digitalizers. And in that a MOSFET can easily be simplified and analysed using what is known as a switch model. So, we saw that when you apply a certain gate voltage above a threshold the MOSFET conducts and we will call it as on state. So, if I put my  $V_{GS}$  greater than  $V_T$  so  $I_D$  is basically some number you know it is going to be some  $I_{DS}$ .

Let us call it  $I_{D0}$  some number or we will call it  $I_{D ON}$ ,  $I_{ON}$  is a better number when the transistor is on. So, specifically what we will do is this is going to have  $V_{GS}$  of  $V_{DD}$  and  $V_{DS}$  of  $V_{DD}$ . If we put both my drain and the gate voltages at the supply voltage then whatever drain

current, we refer to it as  $I_{ON}$  that is when the switch is on. When your  $V_{GS} = 0$ , we will call this as  $I_{OFF}$ .

So, essentially in a processor like for example a code to do a processor in your computer would essentially keep switching from 0 and 1. So, current will switch from  $I_{ON}$  to  $I_{OFF}$ ,  $I_{OFF}$  to  $I_{ON}$  this is the switching. So, that is what is represented here by if you flip this switch, you have the current you know path which is formed. So, you have current flow from the drain terminal to the source into the ground or if it is open then there is no current flowing that is what we try to show by the switch model.

It is of course a simplified model; the realistic cases will be slightly more complicated. But anyway, for our practical purposes it is right now to consider this. So, how much is the current. To analyse we can see the transfer characteristics but with the  $I_d$  in a log scale. So, it is same  $I_d$  that we have seen in the past, that the current voltage was increasing the current is like this  $I_d$  versus voltage  $V_{GS}$ , this is  $V_T$ .

So, there is an exponential increase in the drain current with respect to  $V_{GS}$ . And it is not quite surprising if you think about it. So, what is the reason how the gate is actually controlling the drain current? We remember this physical picture wherein you have a fermi level which is constant and then you have the source and then the drain and in between you have the channel.

So, we saw that there was a barrier that is forming here. This is a potential barrier because you know the electric field here is going to be in this direction and the electric field is here in this direction. So, electrons cannot enter into the channel so there is no current flow. And this barrier is what dictates your current flow. So, when you increase your voltage, gate voltage for the positive direction you are lowering the barrier this is for a NMOS device and in the opposite case when you decrease it actually increases the barrier.

And we saw that whenever you have current flow across a barrier like for example a pn junction is a simplest case. You saw that the current  $J = J_0 \left( \exp\left(\frac{qV_{app}}{KT}\right) - 1 \right)$ . So, this is what the current was whenever you have a current flow across a barrier. So, it will depend on the barrier height.

So, now what you see is you know if you have such a phenomenon, it is very useful to draw the transfer characteristics in a log scale. So, what we are showing here is initially once above a  $V_T$  there is going to be some change and because it is a log scale it does not seem like it is a lot, but there is a significant increase in the current. But you know in the past whenever we showed the IV characteristics, we did not really emphasize this part we did not know.

What is off current here? How much is it that is important? So, to emphasize off current we show the IV characteristics in the log scale. When we do that when  $V_{GS}$  is 0 let us say there is going to be some current here which we call as off current and when  $V_{GS}$  is  $V_{DD}$ , we call it on current. These two numbers are very, very important for digital circuits. So, we have a you know what we call as a figure of merit you know you could take a ratio of  $I_{ON}$  to  $I_{OFF}$ .

If this ratio plays a very crucial role whenever there is a new technology that comes up, for example INTEL is introducing let us say seven nanometre or five nanometre technologies, they will talk about this. Because this ratio should be high if it is high then it is a good technology and what is a typical number.  $I_{ON}$  is going to depend on various you know geometrical parameters for example current is depend on width length and so on.

And there are also some you know how effective the channel is and actually controlling that. So, I will just take a typical number and I will say that let us say it is about  $10^{-4}$  amps just you know 0.1 milliamps, 100 micro amps divided by  $10^{-10}$ amps. This is a typical number you know this is 100 amps is not really a large current for a single MOSFET.

So, what is the voltage what is the ratio of the  $I_{ON}$  to  $I_{OFF}$ ? This is about in this case six orders of magnitude. So, this is a large change in the drain current and which is very useful for digital applications, we want this to be as high as possible. So, that whenever you turn on the MOSFET you want the current to flow. When you do not want the current when you switch it off you do not want any current to flow.

Why? Because the moment current flows you are consuming power. For example, if you are using a cell phone whenever you just put the cell phone on a table you are not using it. But if it is in the off state the processor has to be the off state, some of the circuits are in the off state. But if they still transmit large current, let us say microns of current then you are going to bleed your battery.

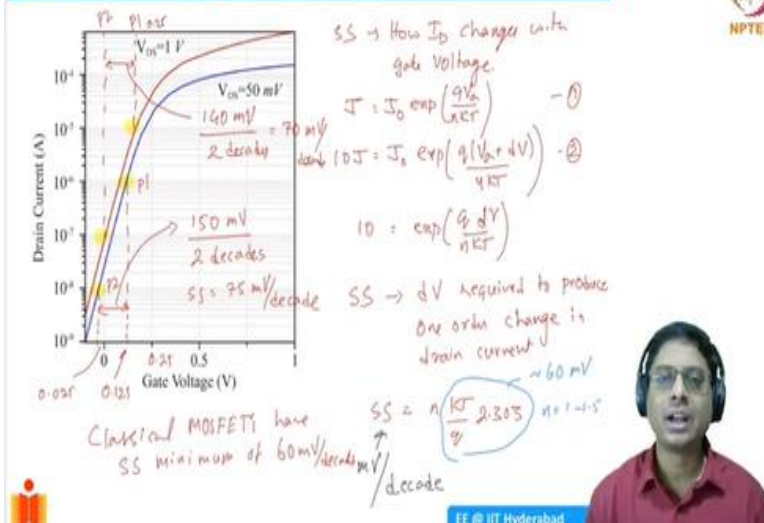
You are going to discharge your battery. So, that is why the cell phones get discharged even if you do not use it. Of course, you know some of the chips are always on and they are trying to communicate with the cell phone tower and all that that happens. But some of the chips are off and they should not discharge any current. But then in reality there is going to be very small current that keeps flowing.

It might be 100 pico amps per MOSFET but then there are one million MOSFETs in your cell phone then it becomes a substantial amount of current.

So, you can compute the power dissipation. The voltage multiplied with the current that will give you the power dissipation. So, it can be substantial amount of power that is getting dissipated. That is why when you are talking to somebody on a cell phone, the cell phone heats up because you are drawing current that is causing power dissipation. Voltage into current, 1.8 into 1 milliamp that is 1 milli watt of power that is getting dissipated.

It might seem like small but then remember there are one million transistors. So, it can be a substantial amount. So, we always worry about the power dissipation whenever we are talking about mobile circuits mobile chips. Anyway, so this is the application of a MOSFET in the digital domain.

## Subthreshold Swing



It is so important that we actually define a parameter which we call a sub threshold swing to capture how the drain current changes with gate voltage.

$$J = J_0 \exp\left(\frac{qV_{app}}{KT}\right)$$

So, this is the current some current is flowing at some applied voltage. Now we want to understand how much gate voltage change do we have to do to get one decade change in the current. Now for example I want to make my current to be 10 times J. If I want to get this how much should I apply how much extra dV should I apply to my gate.

$$10J = J_0 \exp\left(\frac{q(V_{app} + dV)}{KT}\right)$$

$$10 = \exp\left(\frac{qdV}{KT}\right)$$

So, this dV, the gate voltage change required to produce one order of change in the drain current is known as sub thresholds, SS.

$$SS = 2.303 * (KT/q) * n$$

So, this will be n KT by q into 2.3. So, this particular number we have seen it many times this is roughly 60 millivolts and n is basically going to be between 1 and 1.5 in most MOSFETs. So, the sub threshold swing is a very, very important quantity which we define as some number millivolts per decade

So, let us try to take an example and compute this. So, this has implications when we talk about MOSFET scaling that is why I want to emphasize this. Let us say I take my blue curve here, there are two curves. Now one of the  $V_{DS}$  of the gate transfer characteristics is measured at  $V_{DS}$  of 50 millivolts another one we are measuring it in one volt.

$$I_{d1} = 10^{-6} \text{ A}, I_{d2} = 10^{-8} \text{ A}, dV = 150 \text{ mV}$$

$$SS = \frac{150 \text{ mV}}{2} = 75 \text{ mV}$$

So, your sub threshold swing  $SS$  is going to be 75 millivolts per decade. Similarly, you know do one more problem wherein we take the red curve now.

$$I_{d1} = 10^{-5} \text{ A}, I_{d2} = 10^{-7} \text{ A}, dV = 140 \text{ mV}$$

$$SS = \frac{140 \text{ mV}}{2} = 70 \text{ mV}$$

So, there is two decades change here so this is again 70 millivolts per decade. So, this is a very important parameter that controls. Ideally if you have a MOSFET, ideal MOSFET you would like this to be 0. So, that just below  $V_T$  is off no current, should be completely 0.

But in reality, if you use this sort of a junction current flow across the junction sort of a configuration. You will get classical MOSFETs like what we have been discussing so far have  $SS$  minimum of 60 millivolts per decade. This is a minimum that you can get. Essentially what we are saying is we are not able to turn off the drain current, easily we have to change you know reasonably large you know 60 millivolts.

If high  $I_{ON}$  to  $I_{OFF}$  ratio, we have to make  $I_{ON}$  very, very small. Let us say we want to increase  $I_{OFF}$  by five orders or so when we switch it off. Let us say initially the  $I_{ON}$  was one milli ampere when we switch it off, we want it to be one microampere, we want three orders of change in the current. How much should we change my gate voltage? We should change it by three orders so three decades.

So, it will be three into sixty that is a minimum possible voltage, at least we have to apply 180 millivolts. But three decades is not enough nearly enough for us. We want it to be changing by six decades. So, we want to take my one milliamp to one nano amp. If we want to change that much

of current you know six orders of magnitude change in the current then we need to apply 360 millivolts.

Only if we apply  $V_T$  below 360 millivolts, we will go to 360 milli watts below  $V_T$  then we will have our MOSFET switched off completely. This is basically about a summary of various metrics that are important.

But of course,  $V_D$  is important,  $V_{D SAT}$  is important, the drain current at the saturation is very important. So, these are different metrics that we use when we want to compare different MOSFET technologies.

.