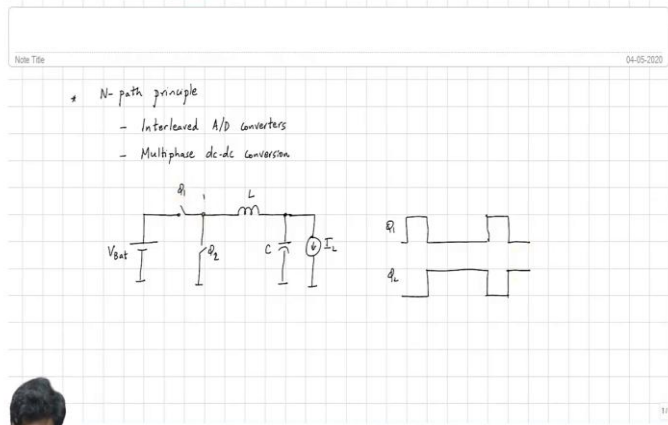



**Introduction to Time - Varying Electrical Networks**  
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**Lecture 48**  
**Dc-dc converter as an LPTV system**


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The slide content includes the following text and diagrams:

- N-path principle**
- Interleaved A/D converters
- Multiphase dc-dc conversion

The circuit diagram shows a DC source  $V_{bat}$  connected to a network of two switches,  $\phi_1$  and  $\phi_2$ . The output of this network is connected to an inductor  $L$ , a capacitor  $C$ , and a load  $I_L$ . To the right, two square wave waveforms are shown, labeled  $\phi_1$  and  $\phi_2$ , which are non-overlapping and complementary.



So, let us continue where we left off yesterday, we were discussing the N-path principle and we saw 1 practical case system which uses this N-path principle which is the area of time interleaved analog to digital converters and alternative another area which is, which also uses this is multi-phase dc-dc conversion and the basic principle behind that is what I am going to explain today.

So, as we were discussing a dc-dc converter as shown in this example is a way, this is let us assume that this is the battery voltage and this is of course, a very simplified picture of the whole thing and the dc-dc converter is supplying some load current say  $I_{sub 1}$ , this is an inductor and this is a capacitor. The principle with which this works is the following,  $\phi_1$  and  $\phi_2$  are non-overlapping clocks. So, this is  $\phi_1$ , this is  $\phi_2$  and therefore, at any one time only one of these switches is open and the other one is close.

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NPTEL

Buck converter

$V_{bat}$

$\phi_1$

$\phi_2$

$L$

$C$

$R_L$

$V_{out} = d V_{bat}$

$V_{bat} e^{j2\pi f t}$  where  $f=0$

$V_{bat}$

$dT_s$

$T_s$

$\phi_1$

$\phi_2$

LPTV network

$\overline{V_{out}} = d V_{bat} \Rightarrow H_0(s) = d$

$V_{out}(t) = \sum_k H_k(s) e^{j2\pi k f t}$

$\sqrt{LC} \gg T_s$

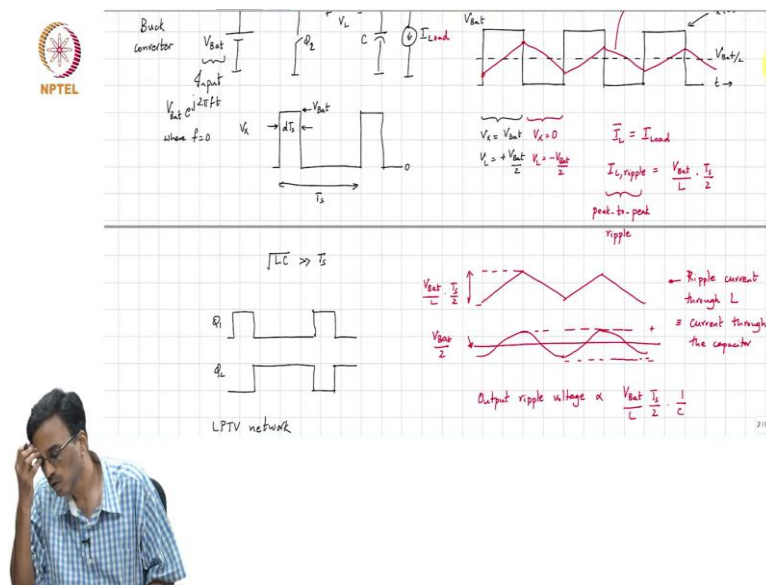
So,  $V_x$  there therefore is a wave form which basically takes on the value of  $V_{bat}$  for a fraction of the period of the clock namely, this is  $T_s$  and the duty cycle with which  $\phi_1$  is high is  $d$  then the width of this is  $d$  times  $T_s$ . So, this is the  $V_x$  waveform as a function of time and the peak value there is  $V_{bat}$  and when of course, when  $\phi_2$  is high, the value is 0. Now, the role of the low pass filter is to just select the DC value of this waveform and therefore, the idea is that if  $L$  and  $C$  have a sufficiently large time constant, then the average voltage, the voltage waveform  $V_{out}$  for all practical purposes should be  $d$  times  $V_{bat}$ .

Ideally if  $L$  and  $C$  are infinite then it should be exactly  $d$  times  $V_{bat}$ , but in practice of course, you cannot make them very big or inordinately big because they were that means it is more expensive and it occupies a lot of space. So, this is what is called a Buck converter for those of you have not seen this before and you know as I was explaining yesterday, this is a way of getting a voltage  $d$  times  $V_{bat}$  which is smaller evidently than  $V_{bat}$  without at least ideally with 100 percent efficiency because none of these elements here the two switches, the inductor or the capacitor, ideally are all lossless elements and therefore, if we are able to step down the voltage without any loss.

Now, where does this fit in? Well, this is a network as far as we are concerned this is a network that has periodically operated switches. So as far as we are concerned this is an LPTV network, the input is DC where in other words, it is  $V_{bat}$  times  $e^{j2\pi f t}$  where  $f$  is 0, and the output voltage is the DC component of the output voltage is  $d$  times  $V_{bat}$ , which implies that the  $H_0$  of 0 is  $d$ .

But unfortunately, because L and C are finite, it is not only DC that is present at the output, we should also expect to see, of t, yeah, so is simply must be sum over k of H sub k of 0, e to the j 2 pi f 0, so it must be k fs times t. And to get an idea of what the waveforms look like, let us assume that L times C, the square root of L times C, which is the time constant corresponding to the LC network is much, much larger than the switching period Ts. Under those circumstances, if we draw these waveforms, let me kind of make things more convenient for you to see.

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If we draw the waveforms, and let us say choose a particular value of d, I mean, this, you can be doing this for any duty cycle, but I am just going to choose an example a duty cycle d equal to half, that basically means that V out the average value of V out is going to be V bat by 2 so V x, if you look at V x, V x is doing this. So, this is V x and V x of t and the output voltage is going to be approximately the DC value of the output voltage is going to be V bat by 2.

So, if you look at the inductor, the voltage during this phase, so, during this period V x equals V bat and therefore, the voltage across the inductor V sub l is nothing but plus V bat by 2. So, if the voltage across the inductor is plus V bat by 2, what comment can we make about the current through the inductor?

Student: (( ))(8:20)

Professor: The voltage across, a constant voltage is applied across an inductor and therefore, what will happen to the current to the inductor?

Student: It will try to ramp up.

Professor: It will ramp up. So, the current through the inductor will basically do this in that phase. And what will, so and what will it do during this phase? What happens to the voltage across the inductor? Well,  $V_L$  one end of the inductor, that is  $V_L = 0$ , and therefore  $V_L$  is minus  $V_{bat}$  by 2 and this is only an approximation, because we are neglecting the small ripple across the. So, this is what the inductor current will look like and so this is  $I_L$  and what must be the average value of  $I_L$ ?

Student: ( ) (9:33)

Professor: No, if there is no average current flowing through the inductor, then who is supplying the load?

Student: The average current has to be ( ) (9:41)

Professor: Exactly. So, the average current passing through the capacitor must be 0 in steady state, and therefore, the average current through the inductor must be, oh, I am sorry, I chose the same  $L$  for the load. I will call this load,  $I_{load}$ . So, the average current through the inductor must be the same as the load current. And what comment can you make about the ripple across the inductor.

Well, the voltage across the inductor during any one phase is  $V_{bat}$ . So,  $V_{bat}$  by  $L$  is the rate at which the inductor ramps up and the time you have for ramping up is  $T_s$  over 2 and therefore, the peak to peak, this is the peak to peak ripple, intuitively these things make sense because, you know if the inductor is very large there is a lot of inertia, it takes a long time to ramp up.

If the voltage is very large for a given inductor, you will, it will ramp up quicker and the ripple will be higher if you wait for a longer time because the ramp will be there for a long period. Now, so the current to the inductor can be thought of as a DC value of  $I_{load}$  plus some ripple riding over it and therefore, the voltage and this current, the inductor current flows through the capacitor and the ripple voltage across the capacitor will cause, I mean the ripple current of the inductor will go through the capacitor and cause a voltage ripple.

So, this waveform if you look at the ripple waveform of the current through the inductor, this is the ripple current and that is  $V_{bat}$  by  $L$  times  $T_s$  by 2 and so, this is the current which flows through the, is the AC current flowing through the capacitor and which is the total

current flowing through the, the ripple current going flowing through L is the actual current flowing through the capacitor because the capacitor cannot have any average DC current flowing through, is the same as the current through the capacitor.

So, if a current like this flows through capacitor what comment can we make about the voltage across the capacitor? Well, it will do something like, it will do something like this. So, this is the ripple voltage, so the capacitor voltage will have a constant value, the average value of the capacitor voltage is nothing but  $V_{bat}$  by 2, on top of it there will be a ripple.

And the amplitude of the ripple will be inversely proportional to, output ripple voltage is obviously proportional to the amplitude of the triangular current through the capacitor. So, is  $V_{bat}$  by  $L$  times  $T_s$  by 2. And it is also proportional to, inversely proportional to the capacitor the capacitor is very large the voltage developed across it will be very small.

So, it is very clear that if you want the output voltage ripple to be small  $L$  and  $C$  must be very large. Now, what this is saying is that well, you need to have a better filter. Yeah. So, if you have a better LC, low pass filter, then you have lesser amount of ripple at the output. There is nothing you know fantastic about this and it is pretty common sense. Very good.

Now, this is the principle behind the basic operation of a dc-dc converter, it turns out that, in practice, it is not desirable to have a large ripple on the output voltage. So, how do you get rid of ripple? Well, there are several ways as you can see from this picture. One is you make the  $L$  and  $C$  very large, it has the disadvantage that the components become bigger in size, and the amount of space they occupy on a board becomes larger. And, you know, they are of more expensive.

Another way is to say, I will have the same components and I am going to reduce the switching, I mean, reduce the switching period. So I am going to reduce  $T_s$  by a large factor. Unfortunately, it turns out that, well, that obviously also reduces the, that reduces the ripple, obviously.

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- Multiphase dc-dc conversion

Back converter

$V_{bat}$

$V_c$

$V_{out} = dV_{bat}$

$d = 1/2$

$I_L$

$V_c(t)$

$V_{bat}$

$V_c = V_{bat}$   $V_c = 0$   $\bar{I}_L = I_{load}$

$V_c = +\frac{V_{bat}}{2}$   $V_c = -\frac{V_{bat}}{2}$

$I_{L,ripple} = \frac{V_{bat} \cdot I_L}{L}$

peak-to-peak

Ripple

$\sqrt{LC} \gg T_s$

$V_{bat}$

$V_{bat}$

← Ripple current through L

= Current through the capacitor

- Multiphase dc-dc conversion

Back converter

$V_{bat}$

$V_c$

$V_{out} = dV_{bat}$

$d = 1/2$

$I_L$

$V_c(t)$

$V_{bat}$

$V_c = V_{bat}$   $V_c = 0$   $\bar{I}_L = I_{load}$

$V_c = +\frac{V_{bat}}{2}$   $V_c = -\frac{V_{bat}}{2}$

$I_{L,ripple} = \frac{V_{bat} \cdot I_L}{L}$

peak-to-peak

Ripple

$\sqrt{LC} \gg T_s$

$V_{bat}$

$V_{bat}$

← Ripple current through L

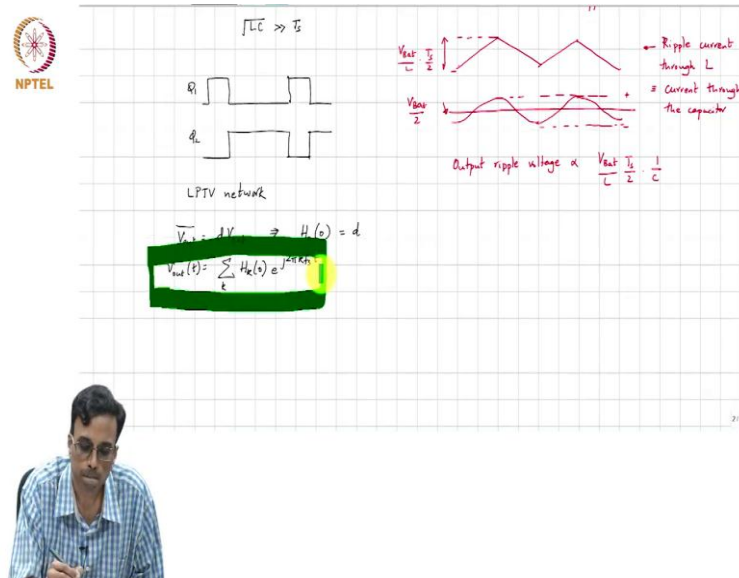
= Current through the capacitor

But the difficulty with that is that now these switches need to be driven at a much higher rate. And it turns out that in practice, there is always going to be a big parasitic capacitance here, which has to be charged and discharged every clock cycle, and therefore, that represents a loss of power. Further, the amount of power needed to drive these switches also is directly proportional to the switching frequency and finally, what do you call, so as a result of all this, you know, running at higher switching frequency will reduce ripple at the cost of reduced efficiency because the switching losses go on increasing.

So, the question is, you know, is it possible to reduce the ripple without increasing the switching frequency, and without increasing the size of the components. And one way of doing that is to use multi phasing, which is basically the N-path principle. Remember, when

we discussed this yesterday, over the last couple of classes, what does the N-path principle do?

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It is that the output voltage as we have seen here is, the output voltage as we have seen here is some  $H_{sub k}$  of 0 times  $e$  to the  $j 2 \pi k s$  times  $t$ , and it is the non-zero components of this expression, namely, the harmonic transfer functions for  $k$  not equal to 0, that are actually responsible for the ripple at the output of the dc-dc converter.