Analog Electronic Circuits
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Lecture – 85
Usage of Current Mirror (Part-C)

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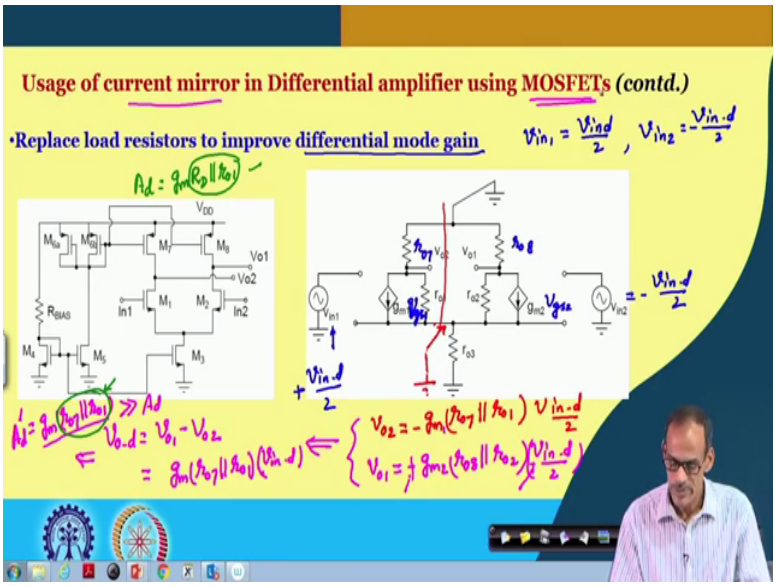

Welcome back after the break. So, we are talking about the differential amplifier particularly constructed by MOSFET. Now we are going to see the differential amplifier using BJT, where we will be deploying the current mirror, corresponding current mirror using BJT and will see the similar kind of situation there.

So, I may not repeat, but just for completeness we shall visit to those circuits which let me go to the next slide to start with replacement of the tail resister.

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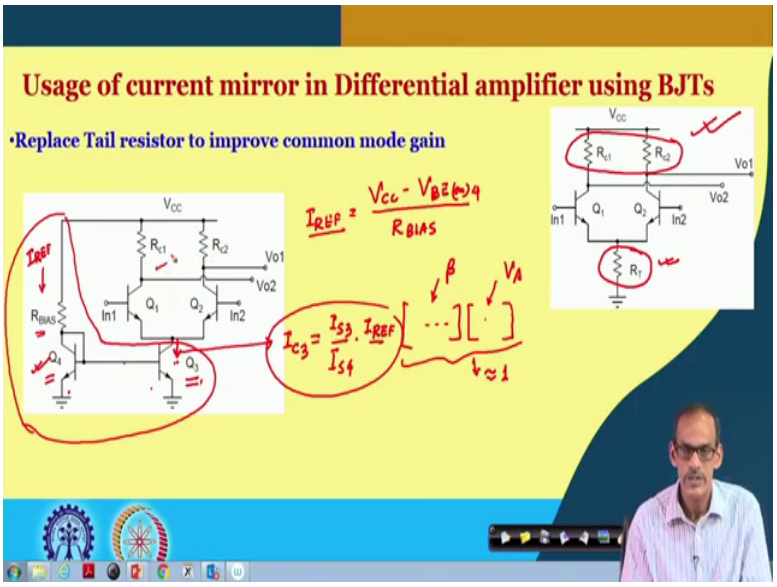

So, here we do have yeah. So, here we do have the differential amplifier which is having till resister is passive element and also the load part it is passive. Now, here instead of R T, what we are using is transistor 3 which is getting a bias from transistor 4 and the R BIAS circuit.

In fact, similar to the previous case, you can see that this is the current mirror circuit which is helping us to set the tail current here. Now in this case the reference current I reference, it is coming from V c c. So, V c c minus V b e on of transistor 4 divided by R BIAS.

And this reference current based on the reverse saturation current ratio or transistor 3 and transistor 4, we do get current here which is I c of transistor 3 it is equal to I s 3 divided by I s 4 multiplied by I reference of course, multiplied by two nonideality factor; one is due to early voltage and another one is due to beta loss or brisk bias loss.

So, we may draw off this nonideality factor considering this is approximately equal to 1. Then we do get the current here said by this I reference current. And once you get the ka reference current here or the tail current here said by the reference current, then we can analyse this circuit by considering it is small signal model.

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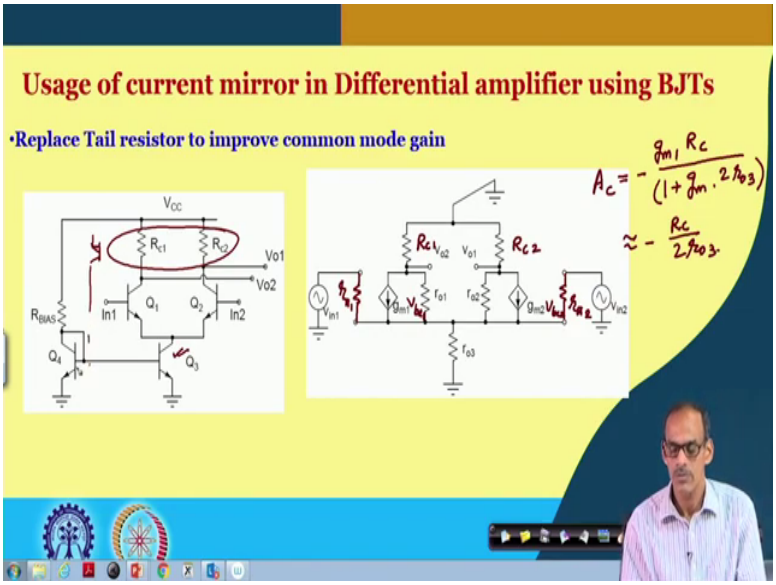

So, as we have done for moss circuit. So, here also we can draw this small signal equivalent circuit compared to the moss circuit the difference here of course, we do have r pi. So, here also we do have r pi and the voltage here it is V b e, V b e 2 here and we do have R c 1 and R c 2.

Now again similar to the previous case here if you analyse we can find the common mode gain. It is g m into R c divided by 1 plus g m into 2 times of r o 3 and that can be well approximated by R c divided by 2 times of r o 3.

Now similar to the previous case, this this part can also be replaced by active load and that load current of course, should be consistent with whatever the current we do have flowing through transistor 3 and to make it consistent the mirroring circuit should also get current from here as we have seen for MOSFET version. The corresponding circuit is given in the next slide yeah.

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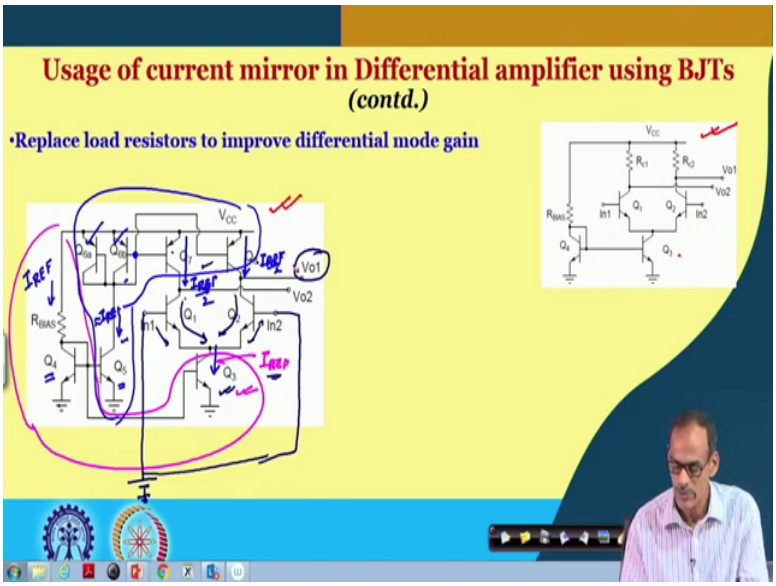

So, here we do have that modified circuit. So, the modified circuit is given here and this was the previous circuit where load it was passive, but till tail element it was bias by current

mirror. Here we do have both the tail part it is coming from this current mirror and the load part.

So, this load part it is having these current mirror and it is reference current of course, this reference current it is also getting from the same common reference current. And as a as a result we can maintain the good balance of this current and this current together with whatever the current is flowing through transistor 3. Namely, if I say that similar to the previous case if I say this is I REF, assuming transistor 4 and transistor 5 they are identical.

So, this current it is also approximately equal to I reference and then we do have two transistors identical transistor to transistor 7 and 8 which is mirroring and since we do have two transistors diode connected I have connected, this is connected. So, the current here it is I reference by 2 same thing here also it is I reference by 2. And here on the other side at the tail we do have this current it is I reference.

So, whenever we are applying a common DC voltage and if transistor 1 and transistor 2, they are identical then you can see half of these two currents together they are converging to I reference without any problem maintaining their corresponding V b equal. So, that is how the load part it is getting replaced by active device, but as I said that this proper matching of the active load current with the tail current it is essential otherwise the DC voltage it may having some issue.

Now here, similar to the common mode gain for differential mode gain we can we can draw the small signal equivalent circuit and then we can analyse the circuit to get the differential mode gain.

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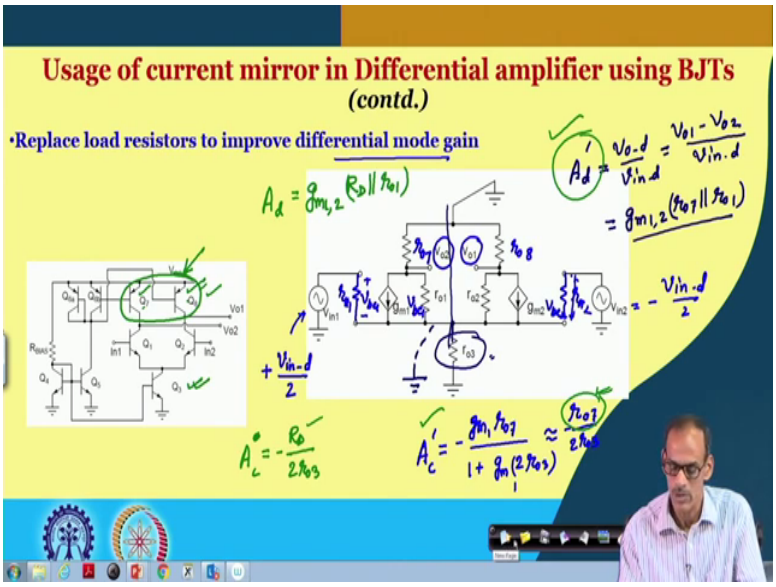

So, in the next slide we do have the corresponding small signal equivalent circuit, it is in fact, we do have r pi here and r pi here and this register it is r o 7 and this is r o 8 g m 2 into v b e 2, g m 1 into v b e 1 and v b e 1 it is given here. So, likewise here also we can get the v b e 2.

And, then we do have the corresponding output and for differential mode of operation; we can say this is half of the differential input is coming as v in 1 with maybe positive polarity and here it is remaining half namely v in d by 2, but with a minus sign. And since left and right parts they are identical. So, again we can split this register, in fact, it is not necessary to split for differential amplifier rather this node it becomes AC ground or a virtual ground.

That makes this part, left part and right part we can consider independently without considering this r o 3 and by analysing this circuit we can find the corresponding differential mode gain say A d dash which is defined by v o d divided by v in d and v o d it is v o 1 minus

v o 2 divided by this v in d and. As you have discussed earlier in other examples it will be easy to find that this is equal to g m 1 or 2 multiplied by r o 7 in parallel with r o 1.

In comparison with this modified gain, if you recall the previous circuit; differential mode gain it was g m 1 or 2 transistor multiplied by R D in parallel with r o 1. So, definitely this is having much higher gain. In fact, this circuit since the active load the here you are using active load with respect to passive load. The common mode gain of course, got increased, but since differential mode gain also got increased it is not an issue.

So, just for completeness modified common mode gain it becomes r g m into r o 7 divided by 1 plus g m into 2 times r o 3 with a minus sign and approximately this is approximately equal to r o 7 divided by 2 r o 3. So, this is in comparison with the previous circuit gain, common mode gain, it was minus R D divided by 2 times r o 3.

So, here of course, the common mode gain it got increased with respect to R D, here we do have r o 7 which is much higher, but if I consider the ratio differential mode gain divided by common mode gain that is remaining unchanged. In fact, the ratio is important which is referred as common mode rejection ratio. So, to summarize we have replaced both the active load part and the tail part it is getting in fact, current mirror. So, that makes the differential mode gain and common mode gain getting improvised.

Now instead of having say this kind of load which is not having any signal propagating we may have some better arrangement particularly, because if you see this transistor current and this transistor current DC current wise they are same. So, we may be having some attempt to or tendency to use current mirror here.

So, in the next slide what we will see that there will be an there will be one modification of replacing this active load by active current mirror load.

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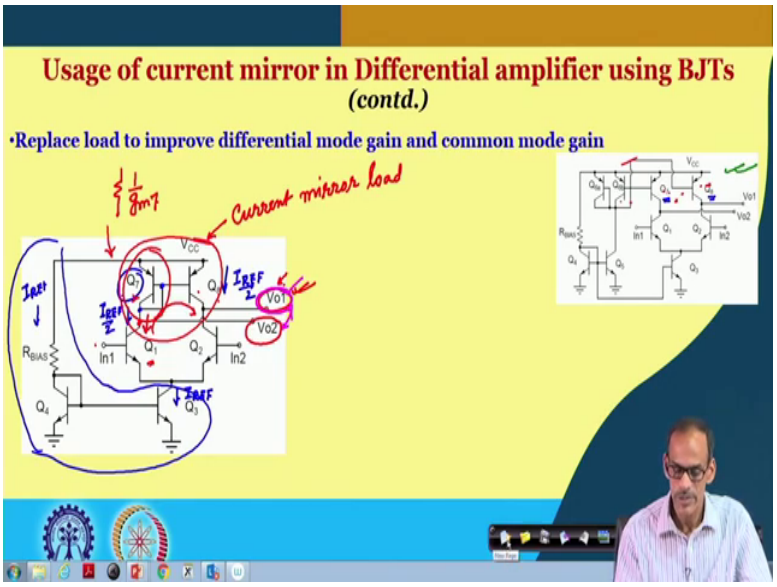

So, here we do have the active load circuit sorry, here we do have the active load circuit. On the other hand, if you see the transistor 7 and transistor 8, both are having equal DC current. So, why not making this transistor like a diode connected transistor if it is having say half of the current flowing here then that half current or I REF by 2, that can be that can be mirrored into transistor 8.

So, if this is I REF by 2 so, these two currents together it is giving I REF and that makes definitely the circuit simpler. So, what we are looking for here it is we do have simple only this portion it is having a current mirror bias and in addition to that we also have a current mirror load. So, this kind of load it is referred as current mirror load. Note that, here also we do have a current mirror, but we do not consider this as current mirror load. Namely because

this current mirror though we do have current mirror circuit, but it is just getting only DC bias.

In contrast to that in this case whenever we will be applying a signal, transistor 1, it is having say current signal and that signal it is also getting mirrored into transistor 8. And there will be it is direct impact or consequence on the differential mode gain on and current mode gain or to be specific the signal here it is a function of this one.

Also since this transistor 7 it is diode connected. It is expected that a signal at this node it will be getting affected because the impedance of transistor 7 which is diode connected. So, that impedance it will be much smaller in fact, this will be approximately 1 by g m 7.

So, as a result at this node the signal it will be less. But, but we have to keep in mind that because of the signal it is getting mirrored from transistor 7 to 8. The signal on the other side namely at V o 1, it is getting enhanced and the signal here it is getting doubled. So, if I take difference of this two and if I say that is the differential output signal, then we will not be seeing any change on differential signal.

So, that is how it is done. In fact, that it makes the circuit much simpler as you can see. In fact, it is not just only for simplicity this circuit is popular, in addition it is also used to make the circuit differential to single ended.

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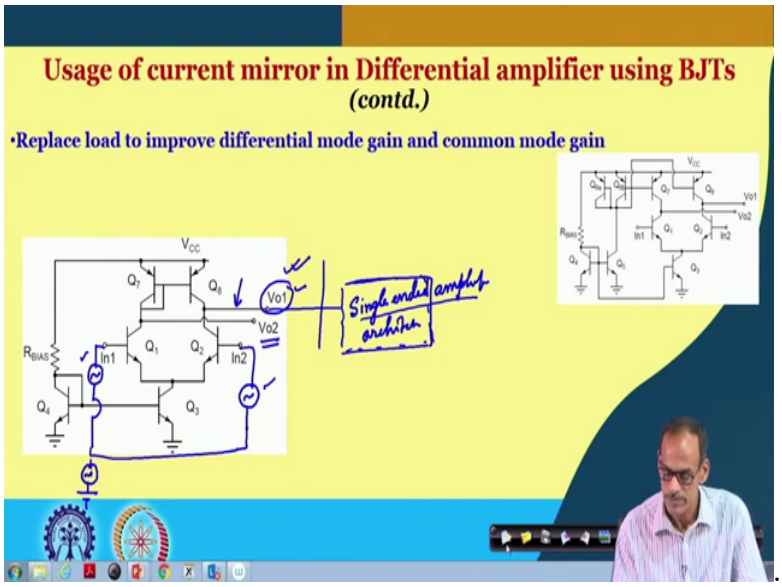

So, here we do have most of the signal whereas, at this node we do have hardly any signal. So, while we are stimulating this circuit by say external whatever the signal coming here which is signal it may be coming in the form of differential and common mode component. But, then the differential part it is getting combined and it is coming in the form of single ended and whatever the circuit you will be connecting here in case if the common mode part it is nicely rejected by this circuit at this point then rest of this circuit, rest of the circuit we can use in the form of single ended architecture, single ended amplifier architecture.

So, from this point onwards it will be single ended amplified. So, similar to this BJT we also have the MOSFET version where we can replace the active load by active current mirror load.

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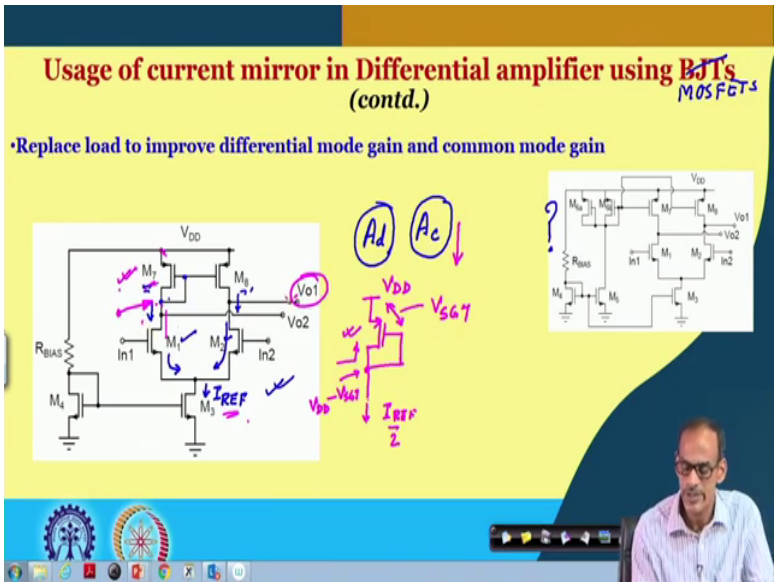

So, in the next slide we are having that circuit. So, as you can see here transistor 7 and transistor 8, they are forming a current mirror and again similar to the previous BJT version. So, sorry this should be MOSFET. So, here the not only of course, from DC point of view, the current here it is getting mirrored here and we know for DC operating point current flow through transistor one and transistor two they should be equal.

So, whatever the reference current we do have, we do expect half of this reference current it will be coming from transistor 1 and that half of the reference current it is getting nicely mirrored here which is eventually coming back to transistor 2. So, that makes the entire circuit well balanced.

So, and as I said that it is not only making this circuit much simpler compare to compare to this circuit it also improves or modifies the differential mode gain and common mode gain. In

fact, if we see the differential mode gain it hardly gets change, but the in common mode gain it is getting drastically dropped. So, in the next slide we will be talking about the common mode gain and differential mode gain by drawing it is small signal equivalent circuit.

So, DC point of view also we have to keep one thing one important thing here that since this transistor yeah since transistor 7 it is diode connected voltage here it is pretty well defined. In fact, whatever the half of this reference current is flowing here along with the V gs of this transistor it defines the corresponding voltage here. So, if I draw the left part, we do have transistor 7 diode connected.

At the source we do have V DD and the current flow here it is I reference by 2. So, by considering it is dimension and the K factor, we can find and of course, the threshold voltage we can find what is the corresponding V SG of this transistor. So, the voltage here it is DC voltage here it is V DD minus this V SG. So, this node since it is diode connected you may say that DC wise it is very well defined and small signal wise you may say that impedance of this circuit, small signal impedance it is much smaller namely 1 by g m.

So, based on the reference current you can find the corresponding DC voltage here and this DC voltage eventually if this 7 and 8, they are well matched. It can be shown that DC voltage on the left side it is also equal to DC voltage on the right side. So, let me try to explain why the DC voltage here and DC voltage on the right side they are equal.

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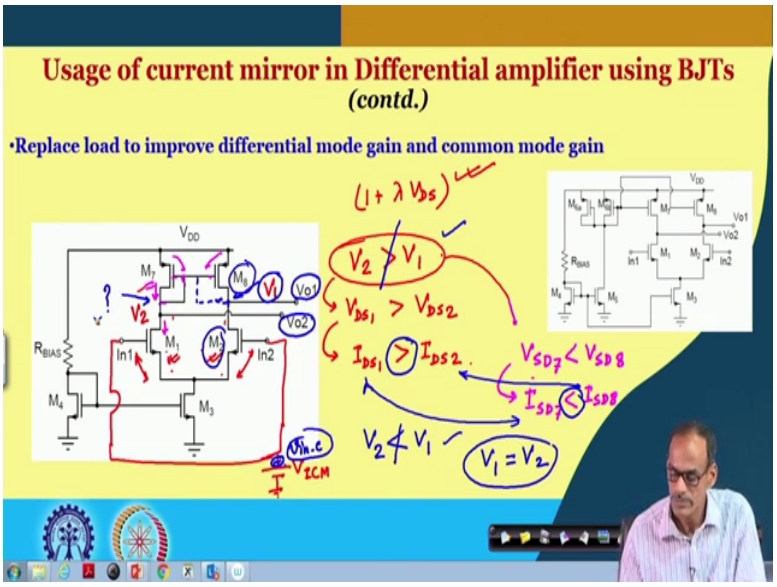

Suppose, if I consider 1 plus lambda V DS part also for all the transistors particularly all the 4 transistors. And then if I say that DC at this point it is say V 2 and DC here at this side it is V 1. So, if I consider V 2 it is a higher than V 1 and let we assume that we do have same DC voltage connected at the both the inputs and assuming transistor 1 and transistor 2, they are identical.

So, since we do have same common mode voltage, it is coming to the input. So, we may say that we are expecting that these two currents should be same because the V GS here and the V GS here they are equal and transistors are identical.

But if I consider lambda V DS part then definitely the they may be slightly different. So, if I consider V 2 it is higher than V 1, which means that V DS of transistor 1 it is higher than V DS of transistor 2 and that gives us I DS of transistor 1, it is higher than I DS of transistor 2.

And this this difference is primarily by considering 1 plus lambda V DS and then if I consider this condition on the upper side and if I consider transistor 7 and 8 they are identical.

So, that makes v s d or transistor 7 it is less then V SD of transistor 8. In fact, that gives us though these two transistors are identical and then they are V SD, they are identical, but because of one plus lambda V DS you may say that I SD of transistor 7 it is less than I SD of transistor 8. But then since it is DC connection in the there is no current flow here it is capacitive connection the I SD of transistor 7 and I DS of transistor 1, they are equal.

So, if these two are equal and also this two are equal, but then their relative value it is having opposite condition. So, that makes this condition not possible. So, similarly, it can be shown that V 2 cannot be less than strictly cannot be less than V 1. So, by considering this we may say that V 1 should be equal to V 2. So, DC wise you may say that this node and this node they are identical.

So, you may say that they are virtually getting short and not only this is for DC, even if you have say is some small signal here even for the small signal whatever the signal you will be getting here, the same signal it will be coming here. So, if I know what will be the voltage coming here for common mode input v in c whatever the voltage we are getting here we can directly say that the corresponding voltage it is coming to the other input. So, to get the common mode gain of this circuit, we can simply consider left up and then you can what will be the corresponding right of voltage.

Even though this is not directly connected and we are expecting that M 8 and M 2, they are in saturation region and hence the output impedance should be very high, but because by the virtue of this current mirror particularly for common mode operation, the left of left side output and right side output they are identical. So, to get the small signal common mode gain, what we can do probably we can draw the small signal equivalent circuit and then there we can analyse the circuit to get the common mode gain. So, in the next slide we will be having that analysis yeah.

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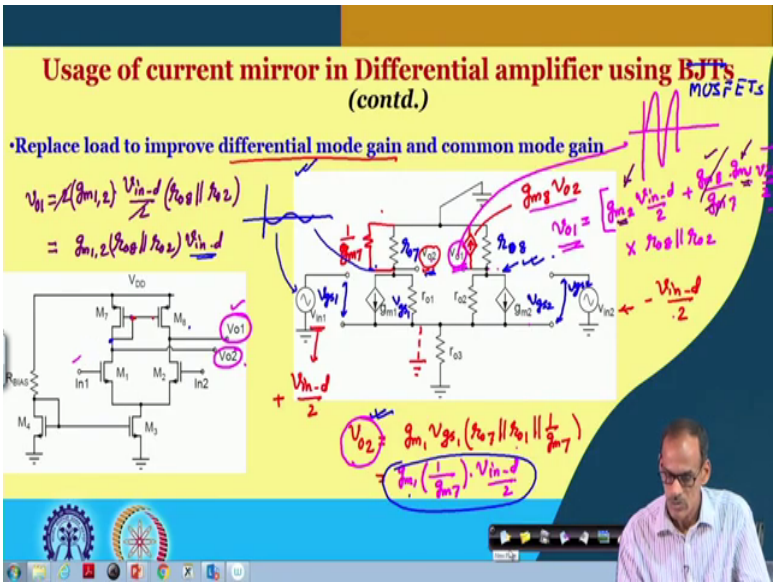

So, we do have the small signal equivalent circuit most of it only thing I have to add here it is g m into v g s. So, an v g s 1, it is here this is MOSFET. So, likewise here we do have v g s 2 and this is v g s 2. Here we do have transistor 8 and here we do have. So, this is r o 8 and also we do have r o 7. In addition to that we do have this transistor diode connected.

So, what we are expecting? Either we draw the voltage dependent current source or simply you can since it is diode connected you may say that it is having 1 by g m 7 is the equivalent resistance. Also this node it is going to the gate of transistor 8. So, in case if we have a signal here at say V o 2, that signal it will also provide a current here and this current it is g m 8 multiplied by v o 2 right.

So, now if you see two cases particularly for common mode operation and differential mode operation. Let me to start with let me consider v in 1 equals to v in d by 2 with a plus sign

here and this is equal to minus v in d by 2. Even though this circuit and left circuit and right circuit they are not perfectly well balanced, but still approximately you can consider that this is AC ground.

So, this is for differential mode of operation you may consider this is AC ground. And the voltage coming here at v o 2 it can be written as g m 1 into v g s which is v g s 1. In fact, this is multiplied by r o 7 in parallel with r o 1 in parallel with 1 by g m 7. Now v g s 1 equals to v g s. So, this is g m 1 into v g s 1 it is essentially v in d by 2 and this part it is approximately equal to 1 by g m 7. So, this is v in d by 2. So, that gives us the output voltage here.

Now, if I consider on the other hand if I consider the voltage here V o 1. So, the v o 1, it is this is equal to the current here we do have g m 2 into v g s 2 which is equal to minus v in d by 2. So, this minus and that minus is getting cancelled. So, you can say simply v in d by 2 multiplied by the resistance here, but also we do have this current which is equal to g m 8 into this voltage and this voltage it is g m 1 divided by g m 7 into v in d by 2 and this multiplied by this multiplied by the resistance here. So, the resistance of course, here it is r o 8 in parallel with r o 2.

So, if let me use the other space to write this v o 1 equals two if I considered g m 8 and g m 7 they are equal. So, I can cross it and then we do have g m 1 here and g m, g m 2 and g m 1 they are same both are getting multiplied by v in d. So, we can see that this is g m 1 or 2 multiplied by v in d by 2 multiplied by r o 8 in parallel with r o 2. So, this is having two times; one is coming from say g m 2 part another is coming from the current mirror part. So, this 2 and this 2, they are getting cancelled and that gives us g m 1, 2 multiplied by r o 8 in parallel with r o 2 into v in d.

So, this is very interesting that signal here, signal here compared to the previous case got doubled. Earlier we obtained the signal here and signal here they are having equal amplitude, but of course, in opposite phase on the other hand now the signal here is this is much smaller. If you see the gain here it is approximately equal to say maybe 1, if say g m 1 and g m 7 they are equal. But the signal on the other hand here it is much higher or it is getting doubled.

So, I should say if I observe the signal here and signal here at this side we may have very small signal almost in the same order of this one. So, the signal here and signal here they are having similar amplitude of course, they are in opposite phase. On the other hand, if you see at V o 1, at this point the signal here it is having much bigger amplitude.

So, we may simply consider this node as the primary output and then we may say that this circuit it is having from this point onwards this is carrying the quote and unquote entire signal. And this port or this node it is having hardly any signal or rather this signal it is amplitude it is in the same order of magnitude of the primary input.

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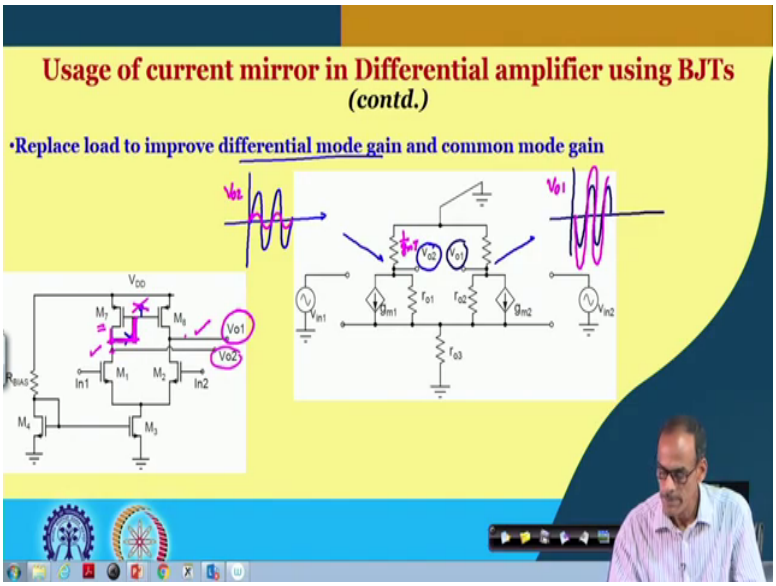

So, to summarize what I like to say here it is. If I consider say this is not connected rather if this node it is coming from independent bias then the voltage here and voltage here under differential mode of operation they were having equal magnitude something like this.

So, here it was signal it was having equal amplitude, but opposite phase right. And now if I make this diode connection, if I make this diode connection instead of giving independent bias now if I give the bias getting generated from here. So, that makes this signal is getting much weaker because of this diode connected transistor it is registrants it becomes 1 by approximately 1 by g m 7.

On the other hand, this signal got amplified, it got doubled. So, this is v o 1 and this is v o 2. So, for diode connected transistor 7, we can say this is the main output and this is I should say secondary output also you have to keep in mind that voltage DC voltage here and DC voltage here they do have the same level. As I said that voltage here and voltage here cannot be different for common mode operation. So, now we can talk about the common mode gain.

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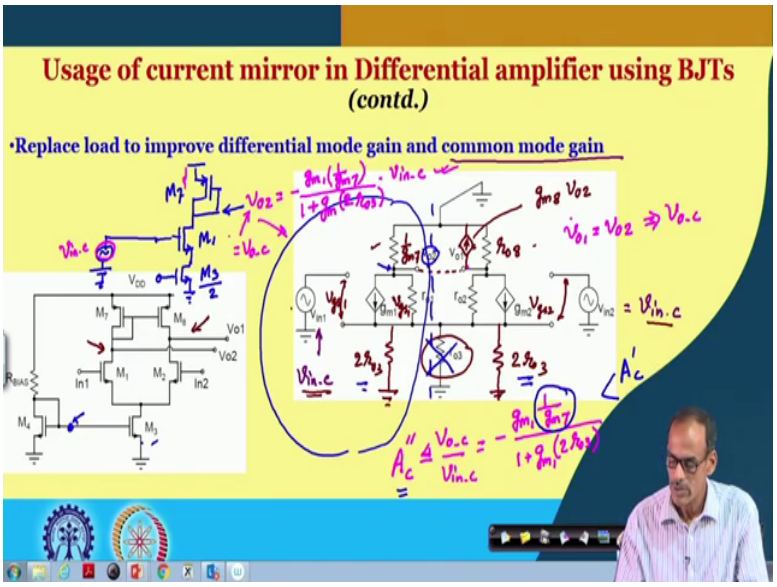

So, let we talk about the common mode gain. For common mode operation this is v in c this is also v in c and; however, this resistance this is 1 by g m 7 approximately this is r o 8, but it is also having voltage dependent current source which is equal to g m 8 multiplied by v gs which is same as v o 2. Now this is g m into v g s 1 and this is into v g s 2 and this is the corresponding v g s 2 and this is the corresponding v g s 1.

Now, under this common mode operation we are applying same signal here as well as here and as a result we may say that we can probably since left and right half they are having similar kind of situation. We can split this resister into two identical parts; this is r o 3 2 times and this is also 2 times of r o 3. Now as I said that this voltage and this voltage under strictly common mode operation whether for DC voltage or even for common mode condition, since these two voltage is they are equal.

So, we may say that this node and this node they are virtually short. In fact, if you short it then this voltage dependent current source can be replaced by one register which is same as 1 by g m 8. So, that makes the left and right part they are identical and hence you can split the circuit without any effect. So, you can replace this one, this resister by these two identical resisters. And then to find the voltage at this node V o 2, we can simply analyse this part and if we analyse this circuit it becomes like a common source amplifier, where the load it is diode connected.

So, the circuit becomes like this. We do have g m 1, we do have g m 7 connected to V DD and then this transistor half of the transistor we may call say M 3 by 2. It is just a just a matter of representation and at this point we are giving the small signal along with the DC. Of course, this node it is getting the bias similar to this point and we like to know what will be the corresponding output here due to the small signal and this small signal it is v in c.

Now, if you analyse this circuit or if you draw the small signal equivalent circuit, you can find that the voltage here v o 2, it is equal to minus g m 1 multiplied by whatever the impedance we do have which is 1 by g m 7 divided by 1 plus g m 1 multiplied by 2 times of this r o 3. So, this into whatever input signal we are applying v in c. In fact, as I said the voltage here also it will be same.

So, we may say that v v o 1 under common mode operation is also equal to v o 2 and that gives us v o c equals to same as whatever we have obtained here. So, this is equal to v o common mode. And hence the corresponding common mode gain if I say AC double dash which is defined by v o c divided by v in c. So, that is equal to minus g m 1 multiplied by 1 by g m 7 divided by 1 plus g m 1 multiplied by 2 times of r o 3.

Now, again you can see here because the resistance now it is getting changed to 1 by g m 7. So, this AC it is much smaller than the previous common mode gain. So, to summarize what we can see the advantage of having this current mirror in the load part.

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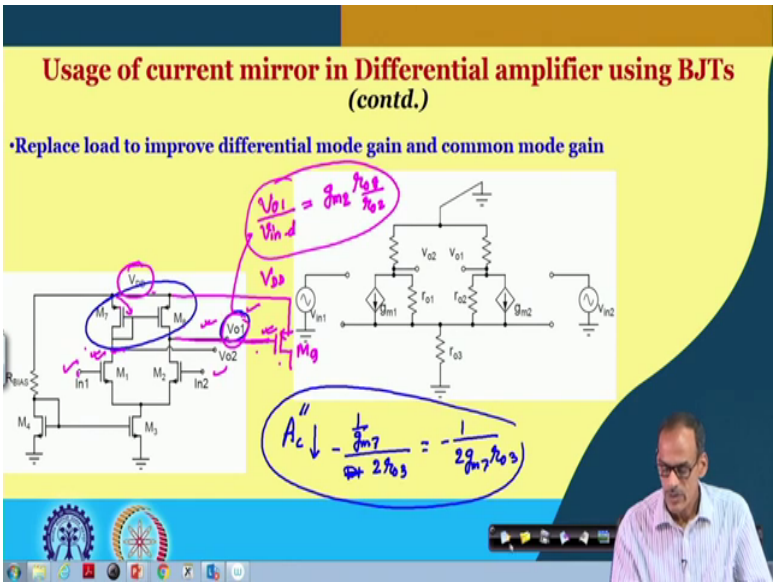

What do we obtain it is the common mode gain got drastically decreased and it is equal to minus 1 by g m 7 divided by 1 plus sorry, one part we can remove so, into 2 times of r o 3. So, that is equal to minus 1 by 2 g m 7 r o 3.

So, this is one consequence of having this active current mirror load and the gain at this point, gain at this point if I say that v o 1 divided by v in d. So, that is becoming g m 1 into r o 8 divided by r o 2. In fact, you may say g m 1 or g m 2 both are same. So, we can say that differential input to single ended output gain it is same as whatever the gain earlier you obtained.

So, that is why this circuit it is very popular to convert differential signal in the form of common mode signal in addition to that since the DC voltage here it is same for the two nodes the DC voltage here it can be directly obtained from this node and since this DC

voltage it is with respect to V DD or to be more precise it is V DD minus V SG of transistor 7. So, we can say that DC voltage here it is V DD minus V SG of transistors 7 and hence this voltage can directly be used to bias PMOS transistor in the subsequent stage.

So, we can have this is V DD and let you call this is transistor 9 and this 9 transistor 9, it is having a very meaningful DC voltage received from on the previous drain node of transistor 8 and of course, it is also receiving the signal which is coming through this V o 1. I think most of the things I have covered.

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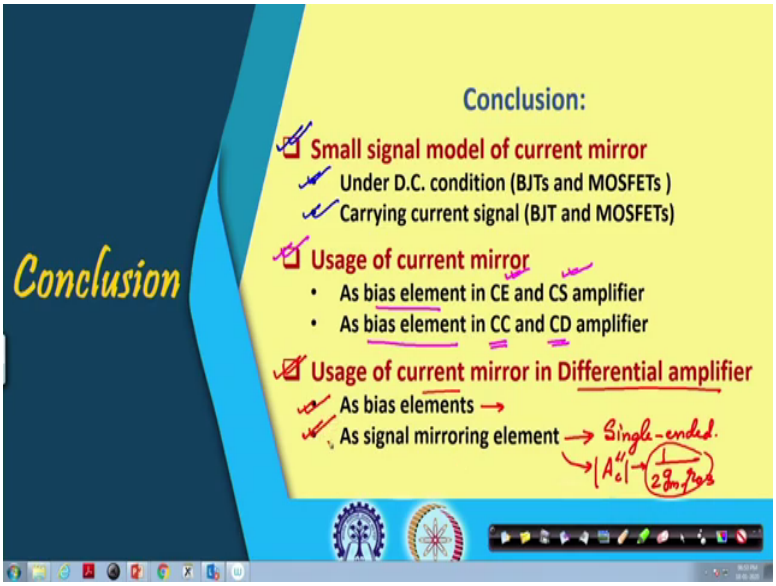

Let me summarize the presentation in these 3 parts of this lecture what we have done it is we have started with a small signal small signal model of current mirror particularly, under DC condition as well as whenever it is carrying the signal current for both BJT and MOSFET versions.

And then after that we have talked about usage of current mirror particularly as bias elements for common emitter amplifier and common source amplifier particularly for the load part and we have seen that it enhance the gain of the both the amplifiers. And then also we have discussed about the usage of current mirror as a biasing element for common collector and common drain amplifier. And then finally, we have talked about usage of current mirror in differential amplifier.

And it is having two kinds of application, one is for biasing element and we have seen that it improves the common mode gain and differential mode gain. In addition to that finally, we have talked about the usage of the current mirror as active mirror load. This helps to convert the output port in the form of single ended and in addition it also decrease the common mode gain what we said is A c double dash very low it is in fact, it is magnitude it is 1 by 2 times g m 7 into r o 3, this is very very small.

So, this helps to improve the common mode rejection drastically. I think that is all to cover. In the next class we will be talking about numerical examples.

Thank you for listening.