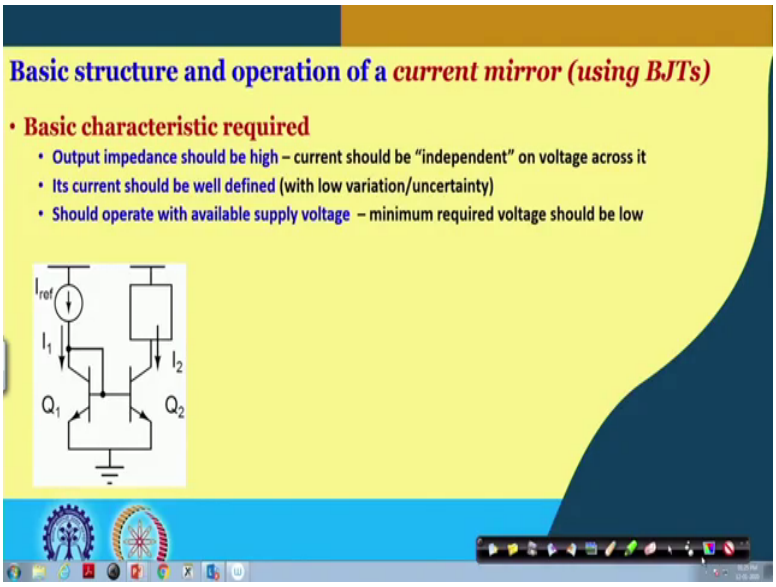
Analog Electronic Circuits
Prof. Pradip Mandal
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

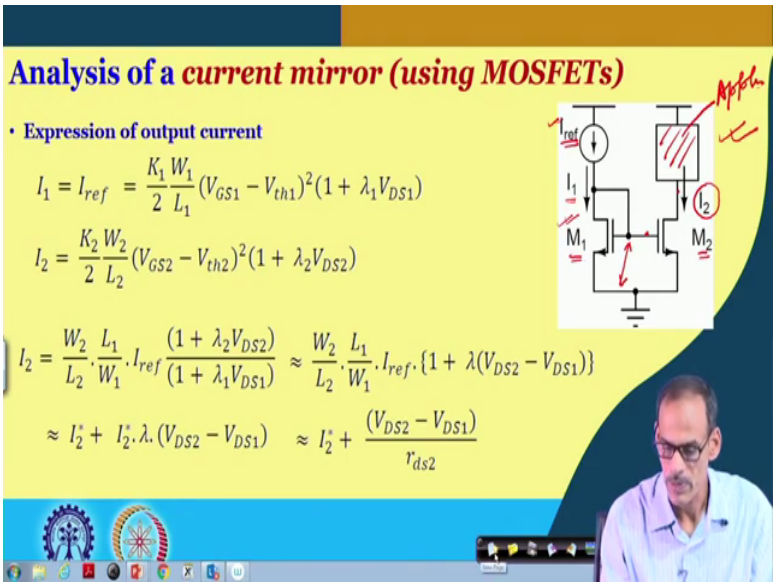
Lecture – 82
Current Mirror Circuits (Part-B)

(Refer Slide Time: 00:32)



So dear students, so welcome back after the break. So, we are talking about the basic structure of current mirror both BJT and MOSFET versions. And now we are going to discuss more detail about the expression of the output current and output resistance of those current mirror.

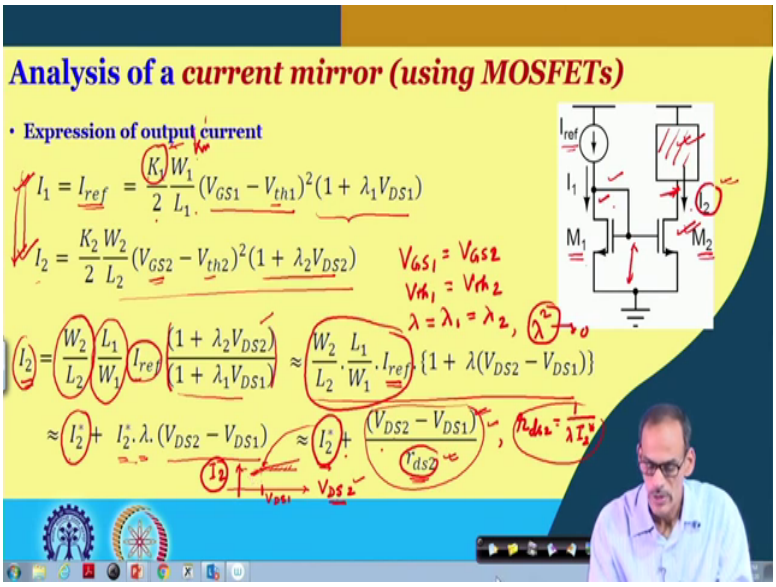
(Refer Slide Time: 00:47)



So, to start with the analysis of current mirror we do have here, the circuit which is, as I said that it is having a reference current, I ref and then we do have transistor-1 here which is diode connected and it develops a voltage V GS which is supplied to the get to source or transistor-2.

And then transistor-2, it is connected to the application here. So, this is the application circuit and we like to get the expression of the current I 2. In terms of the reference current, or you can say this I 1 and then the size ratio of M 1 and M 2. Now to start with, we do have the expression of the current I 1.

(Refer Slide Time: 02:00)



So expression of this current I 1 which is given here. Incidentally, that is also equals to I ref and expression of this current assuming transistor it is in saturation. In fact, this transistor it is in saturation because its drain and gate they are connected together.

And its expression is given here, K divided by 2 W by L of the transistor and typically, in text book it is referred as k n dash; so, that is the eternals conductance parameter. And then that multiplied by V GS minus V th of the transistor square and then we do have 1 plus lambda into V DS of the transistor.

So likewise, we also have the expression of current for the transistor-2. So we do have current here, it is also having very similar expression and because of the connection here, we do have both the V GS's, they are equal namely V GS1 and V GS2, they are equal.

And also, we do have the threshold voltage here and here if we consider they are equal namely, V th1 equals to V th 2. Then, by taking ratio of these 2 currents what we are getting is the expression of the current I 2 in terms of the reference current and then W by L of transistor-2 divided by W by L of transistor-1.

So that is the ratio of aspect ratio of the 2 transistors. And then we also have 1 plus lambda V DS of transistor-2 divided by 1 plus lambda V DS of transistor-1.

Now, we can approximate this part; this part in terms of 1 plus lambda into V DS difference assuming, lambda 1 equals to lambda 2. And also, we are ignoring the term associated with lambda square. So, if you consider lambda 1 equals to lambda 2 equals to lambda, and if we ignore the second-order term associated with this lambda. So if we drop this term, then we do get this approximation rather approximated expression of current flowing through transistor-2.

Incidentally, that is also defining the current through the application circuit. Now, this part it is defined by the aspect ratio of the 2 transistors and also the reference current. And let me denote that by I 2 star, just to indicate that is the main part or nominal part of this I 2 current. And then we also have the additional term I 2 star multiplied by lambda into V DS difference.

So, we can write this expression in this form, I 2 star plus V DS difference divided by r ds 2. Where r ds this r ds2, it is defined as 1 by lambda into I 2 star. In fact, that is the I ds of this transistor. Sorry, this is the; this is the r ds of this transistor.

So, we can say that if the voltage here and voltage here namely, the drain voltage of the two transistors they are equal. So, that makes this part equal to 0 and hence, the I 2 it is nothing but I 2 square I 2 star.

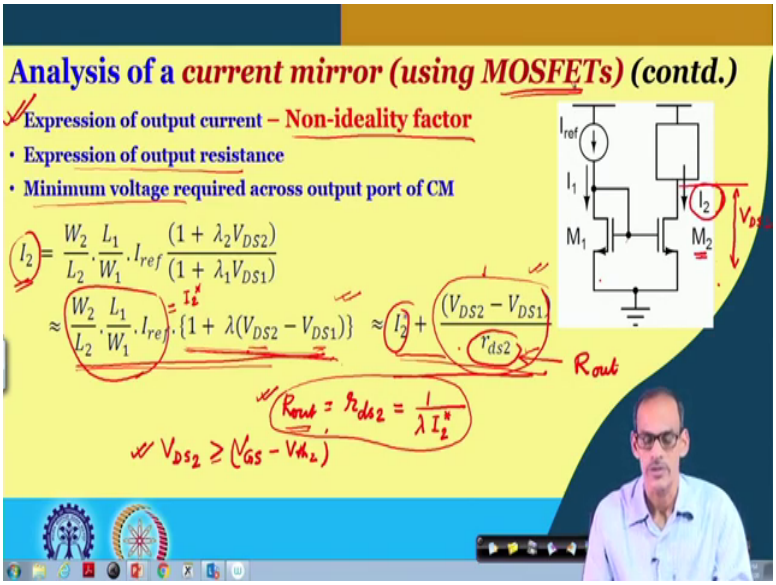
So, we can say that I 2 star is it is the current of transistor-2 when the 2 drain voltages they are equal. Now in case, as I said that the voltage here it will be defined by the application.

And in case, if this voltage or drain voltage of transistor-2 it is different from drain voltage of transistor-1, then we will be getting this additional part of this current.

In fact, if you plot the I DS of 2 or you can say I 2 versus V DS 2 and if V DS equals to V DS 1; V DS 2 is equal to V DS 1, at this point whatever the current we are getting that is I 2 star. And then if V DS 2, it is different from V DS 1, say this is higher, so based on the resistance, the current it will be having additional component.

So, we can say that finite dependency of the I 2 current on V DS 2 is getting captured by the second term. In fact, that is well characterized by this r ds. So this additional part whatever the additional current we do have, that is getting represented by the second term. In fact, this V DS 2 it can be even lower than V DS 1 by almost threshold amount. So, we will discuss that in the next slide.

(Refer Slide Time: 08:21)



So, in summary what you are saying is that the expression of the expression of the application circuit current or I 2 it is given by its nominal value multiplied by a plus plus the additional component which is defined by the r ds. In fact, if you see this expression this part is the I 2 star. So, this is equal to I 2 star which is getting multiplied by 1 plus lambda into V DS 2 minus V DS 1.

So the expression of this current, based on our situation either we may consider this expression this expression whole expression or it may be in this form. So in this form, if you see here, in this form we do have nominal current plus the additional current. Whereas, in this form we do have the nominal current multiplied by a factor which is referred as non-ideality factor.

So whenever, we will be talking about non-ideality factor is essentially that is 1 plus this additional component. Of course, this V DS 2 if it is higher than V DS 1 then this will be positive; otherwise, it will be negative. So that is the expression of the output current. If I say that this is the output of the current mirror.

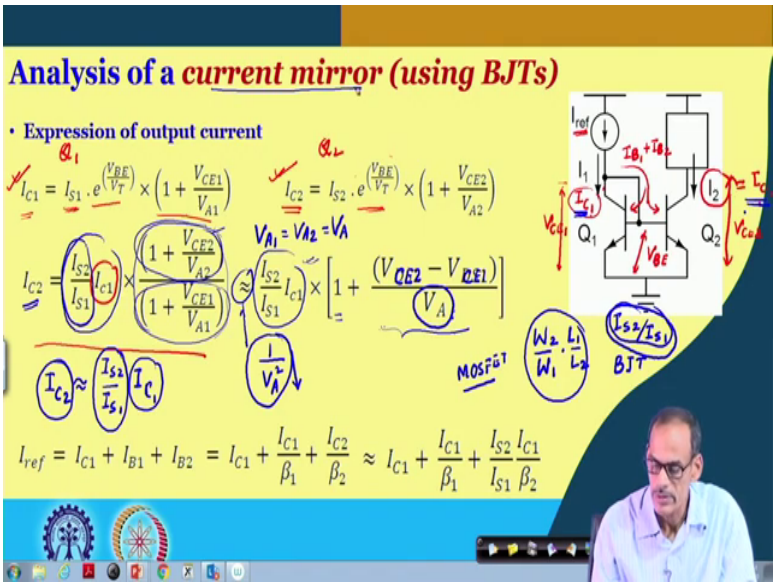
And of course, it depends on the condition of this transistor. Particularly, the V DS of this transistor. If this V DS it is sufficiently high, keeping this t-2 it is in saturation, then only we can get this non-ideality factor it will be small. So, it can be and as long as it is in saturation, its dependency as I said that it can be characterized by this r ds which is also referred as output resistance R out.

So the expression of R out, expression of R out of this current mirror is which is same as in this case incidentally, this is same as r ds 2 and that is equal to 1 by lambda of the transistor multiplied by I 2 nominal, I 2 star. So, we get this resistance it is high only when as I said that transistor it is in saturation and to do so, we require the V DS to be sufficiently high. Namely, it should be higher than its V GS V GS of 2 and V GS of 1 both are same minus V th.

So as long as we do satisfy this condition, then we are getting this output resistance. So, we need to maintain this minimum voltage across this element to get this advantage namely, this

resistance it is high and if this resistance it is high, this part it will be small or you can say that non-ideality factor it will be small. So, similar to this current mirror, similar to the current mirror using MOSFET, let me consider the current mirror using BJT transistor.

(Refer Slide Time: 12:20)



So there also, so, here is the circuit. So there also we can first we can derive the expression of the output current namely, this current, I 2 current. In fact, I 2 it is the collector current of transistor-2 I C2. And also, here we do have collector current I C1. And then this I C1 and I reference they do have a dependent relationship. But, we need to say that this I C1 it is not exactly equal to I ref because we do have some base current is flowing for transistor-2 as well as transistor-1.

So, we do have I B1 and I B2. But before that if you write the expression of the collector current of transistor-1 and transistor-2 in terms of V BE the common V BE voltage and the corresponding V CE, V CE1 here and then here we do have V CE2.

Assuming that both the devices are in active region of operation we do get similar kind of expression for I C1 which is saturation current or reverse saturation current multiplied by e power V BE by V T multiplied 1 plus V CE divided by early voltage of the transistor.

So same thing, we do have the expression of collector current for transistor-2. Now as I said that if I consider this both the V BE's are same and non-ideality factors are equal to 1 or maybe even equal, then we can take the ratio of this current and this current where this V BE part or e to the power V BE part is getting cancelled. And that gives us the expression of I C2 in terms of I C1 and also in terms of the reverse saturation current of the 2 transistor I S2 divided by I S1.

And in addition to that, depending on the V CE voltage, we do have this factor in the numerator and also in the denominator. Similar to the previous current mirror, here this factor it can be approximated assuming that of course, V A1 equals to V A2. And if we consider, if we denote that as V A then we can write in this form, assuming then here also this approximation involves that 1 plus V A square term we have dropped.

So, if I consider, if we ignore the second order terms of 1 by V A then, we do get this approximation. And in this approximation what we have it is this factor, the main factor multiplied by 1 plus sorry this should be V CE. V CE2 minus V CE1. So, in case if this V CE of the 2 transistors they are equal, again this part it will be equal to 0.

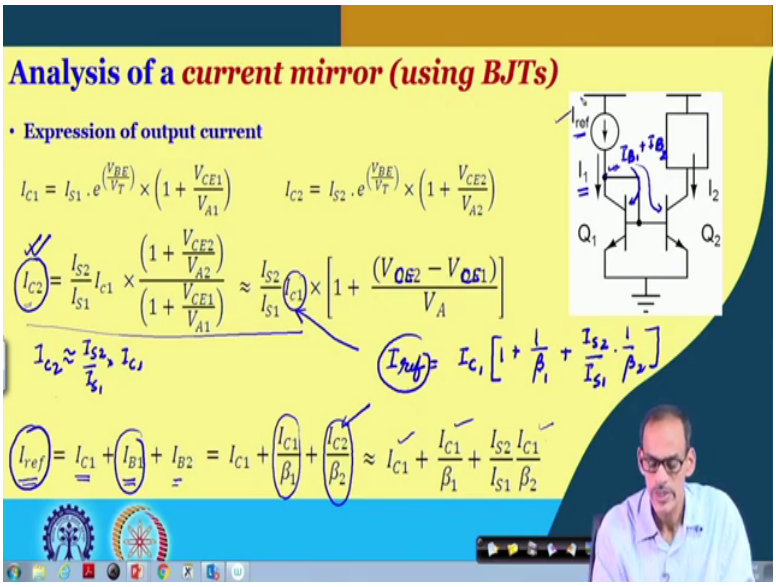
But if they are different then we will get a value and this additional component of course, it depends on the value of this early voltage. Typically, this early voltage it is very high and we may assume that the I C2, it is approximately equal to this one.

So, dropping this part dropping even 1 by V A part. So, we can say that I C2 it is approximately equal to I S2 divided by is I S1 into I C1. Now, if you see here, the expression of this current it is primarily depends on whatever the collector current we do have here multiplied by the ratio of their reverse saturation current.

So we can say that whatever the current we do have, it seems that is getting reflected here or getting mirrored there by the mirror ratio of I S2 divided by I S1. In fact, in the previous current mirror the mirroring ratio it was W 2 divided by W 1 into L 1 divided by L 2.

So, that was the mirroring ratio for MOSFET current mirror. Whereas, for this case the ratio mirroring ratio of the BJT was version it is defined by the reverse saturation current. In fact, geometrically if we see the or dependency of this I S on the geometry of the transistor, this ratio it is I should say emitter to base junction area ratio. Anyway, since this current it is getting mirrored here, that is why the name suggests that it is mirroring the current based on their aspect ratio or emitter area in ratio.

(Refer Slide Time: 19:07)



Now this in this circuit, as I say that the I C1 it is not equal to I ref because we do have we do have the 2 base currents I B1 and I B2. So, let us try to write the expression of I C1 in terms of I ref. This is V CE2 and this is V CE1, as I said.

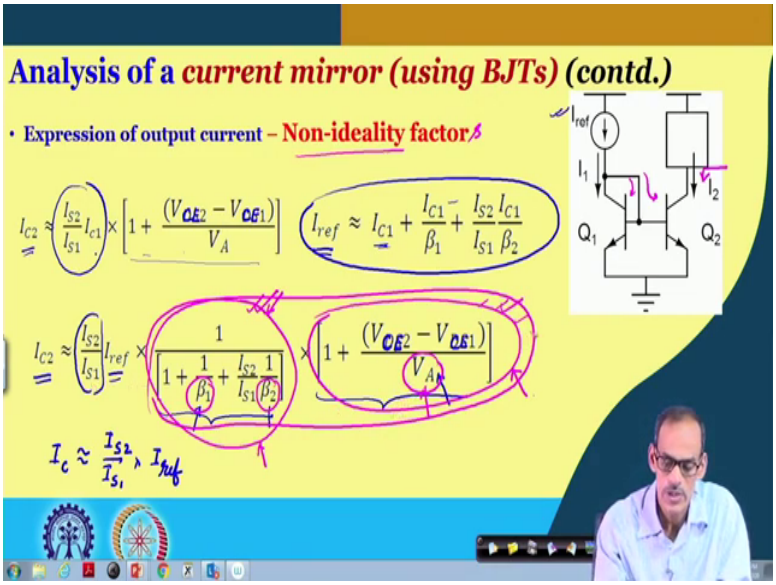
So, now if I at this node if I see the if I consider the K CL, we do have I ref equals to the collector current or transistor-1 plus the 2 base currents. So now, these 2 base currents again, it can we say this current it can be expressed in terms of its collector current namely, I C1 divided by beta of the transistor. So, same thing for the second transistor I C2 divided by beta of the transistor.

And then if I consider this relationship, I C2 can be well approximated by this I S2 divided by I S1 multiplied by I C1. So, from that if we replace this I C2 in terms of I C1, then we do get

relationship between I ref and then I C's. So, we can say that I reference equals to I C1 multiplied by 1 plus 1 by beta 1 plus I S2 divided by I S1 into 1 by beta 2.

So now, we do have the so far we do have I 2 I C2 expression in terms of I C1 and then I C1 can be; expression of I C1 can be placed here namely, I ref divided by this factor to get the current final current in terms of the reference current. So, in the next slide we will be doing that.

(Refer Slide Time: 21:36)



So here, what we said is that the expression of I C2, it is primarily we do have this factor and then we do have whatever, non-ideality factor and then I reference and I C1 is having this relationship. So, by plugging in the expression of I C1 into this equation what you are getting is, the final expression of I C2 which is the ratio of the reverse saturation current multiplied

by this reference current multiplied by 1 divided by this factor, and also we do have this factor.

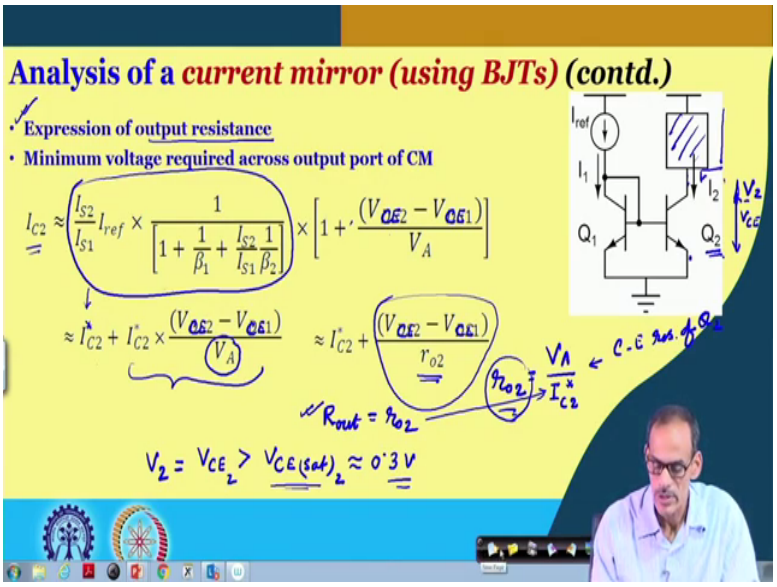
Again, I have repeated this mistake sorry for that. This should be I C2 sorry, V CE2 minus V CE1. So same thing here also this is V CE2 minus V CE1. So now, if the situation it is ideal namely, if the beta is very high say this beta and this beta if they are very high and also, if this early voltage it is very high then we can say that I C2, it is well approximated by I S2 divided by I S1 multiplied by I reference current.

So, the rest of the part of the expression this part we can say, it is non-ideality factors. It is having 2 factor, one is due to the early voltage, another one is due to the finite value of the beta or whatever you say the current loss here due to the base bias. Now this similar to the previous current meter, we can also write this dependency part as in terms of output resistance and this part we can say that loss due to beta.

So in the next slide, we can say that in case, if we get higher output resistance or higher value of this early voltage then this factor it will be getting improvised or this factor it will be going towards 1. On the other hand, but then this factor it will be still it whatever its value it is there it is in fact, less than 1 whereas, this factor it is mostly it is more than 1.

Now, this factor can be taken care differently. So, we may have 2 possible options to improve this circuit. One is to increase the output resistance or increasing this factor: non-ideality factor, other one it is improving this factor. Now, coming to this factor or the effect due to the output resistance, this output resistance can be expressed. In fact, we can rewrite this equation in terms of output resistance.

(Refer Slide Time: 25:33)



Probably, in the next slide I do have that, let me see. So here we can rewrite the expression, we can rewrite the expression of I 2 I C2. So, we can say that this part let me consider this part it is I C 2 squared or sorry I C2 star.

So, if I say that this is I C star then, we do have here I C2 star multiplied by this factor. Again, I have repeated this mistake, sorry for that; V CE2 minus V CE1. Now this part can be expressed in terms of this V CE difference divided by r o2 where this r o2 it is equals to V A divided by I C2 star. In fact, that is the collector to emitter resistance of the transistor-2. So, I should say this is collector to emitter resistance of Q 2.

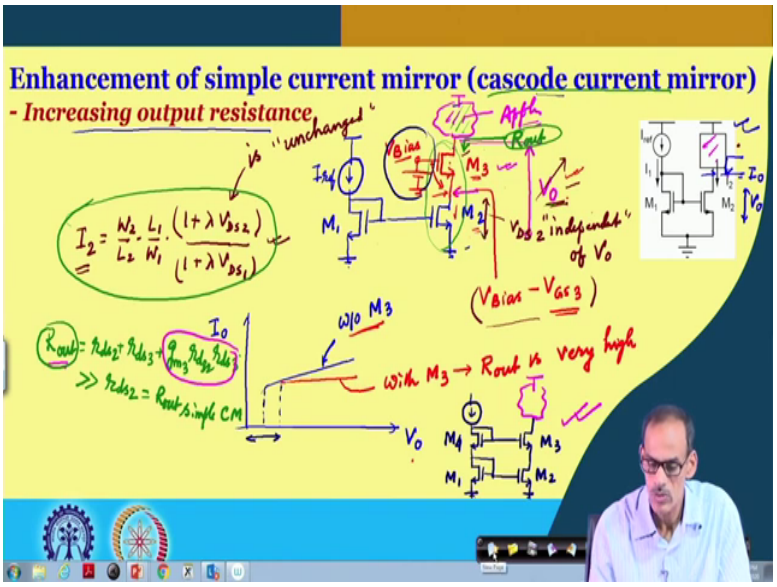
So if this output resistance it is higher, maybe that can be obtained by a higher value of this early voltage, then you can say that this non-ideal part, it will be smaller. So, we may wish to keep the transistor in active region so that we can get the output resistance high. And as I said

that this output resistance it is essentially r o2. So, we can say this R o R out equals to this r o2 which is having this expression.

Now, we can get high value of this output resistance which we are looking for only if we assume that the transistor it is in active region of operation. And to get that, we require minimum voltage across this transistor. So, that is the V CE. So, we can say that the V CE minimum we require it should be higher than V CE sat. And that is the voltage here, voltage across this element we call it is maybe V 2.

So, this is the voltage here. So, we can see the voltage across this current mirror, it should be at least this V CE sat. Typically, its value it is 0.3 volt. So, that may not be a difficult one. So, the application circuit after deducting this minimum V CE Sat, application circuit it will be having a very good possible range for its own operation. So, that way you can say that this circuit is good.

(Refer Slide Time: 29:16)



Now for both the current mirrors as I said that there are non-ideality factors and let us try to see how those factors can be reduced or how we can enhance the circuit performance. So if I consider say, a simple current mirror as it is given here and we like to enhance the circuit performance; when I say enhance, we like to increase the circuit by increasing its output resistance.

So, to increase the output resistance what you can do we can place one transistor at this point, to get the modified circuit like this. So, M 1 and its connection remaining the same, we do have I reference here, connected to supply voltage and then we can have M 2. And then we do have the application circuit here, but in between we like to place one transistor.

Keeping of course, both the transistors if I call say transistor-3, and this is M 2 and we like to keep a meaningful DC voltage here so that this transistor; when I say meaningful, DC voltage

it is such that this transistor this voltage it is sufficiently high, keeping transistor-2 in saturation. And of course, on top of this, we do have the application circuit. So whatever the application circuit we do have, we do have the circuit.

Now, by adding this transistor what we can say intuitively, even if say, this voltage in this case it is changing, if I call now say V O even if I change this voltage, maybe that is done by this application circuit, this voltage hardly it varies. Of course, I am assuming that all the devices are in saturation region.

So, based on the gate bias, V Bias and the current flow here and the size here the V GS of this transistor-3 it is set there. So, the voltage coming here, it is essentially V Bias minus V GS of transistor-3. And this V GS of Transistor-3, it hardly depends on the output voltage.

As a result, even if say this voltage it is changing, even if this voltage it is changing, as long as transistor-3, it is in saturation this voltage it is not changing. So, we can say it is remaining almost constant. As a result, we can say that V DS of this transistor, it is independent of I should say quote and unquote of the output voltage.

So, that makes the expression whatever, I 2 which is W by L of the transistor and divided by W by L or transistor-1 into 1 plus lambda into V DS2 divided by 1 plus lambda into V DS1. Now, this expression of course, remaining same, but then by adding this transistor compared to the simple current mirror. What we are doing is, even if you vary this output voltage the V DS2 it is quote and unquote unchanged.

Or you can say that this current it is it hardly depends on this voltage here. So pictorially, if I compare the 2 cases, the simple current mirror based on probably finite lambda, we do have this output current and the voltage dependency it is having a slope. So, let you call this is output current. So, this is the output current and the voltage drop across this one is say V O output voltage.

Now, if I consider on the other hand, on the this circuit where we do have transistor-3, it is protecting this source voltage from the variation from the output voltage and for that, we do

have the corresponding current it is almost remaining flat. So, this is with transistor-3. And on the other hand, this is simple one without M 3.

So in fact, if you see the waveform, you can see that this is giving us higher output resistance or less dependency of the current on output voltage. So, indicating that R out is very high. And at least compared to this one it is very high. So, let us try to see why we call it is very high?.

In fact, if you see the output resistance looking into the output port here, the output resistance it is basically it is a cascode structure and we have derived the output resistance of the cascode structure which is giving us say R out equals to r ds of transistor-2 plus r ds of transistor-3, plus g m of transistor-3 and r ds of transistor-2 multiplied by r ds of t ransistor-3.

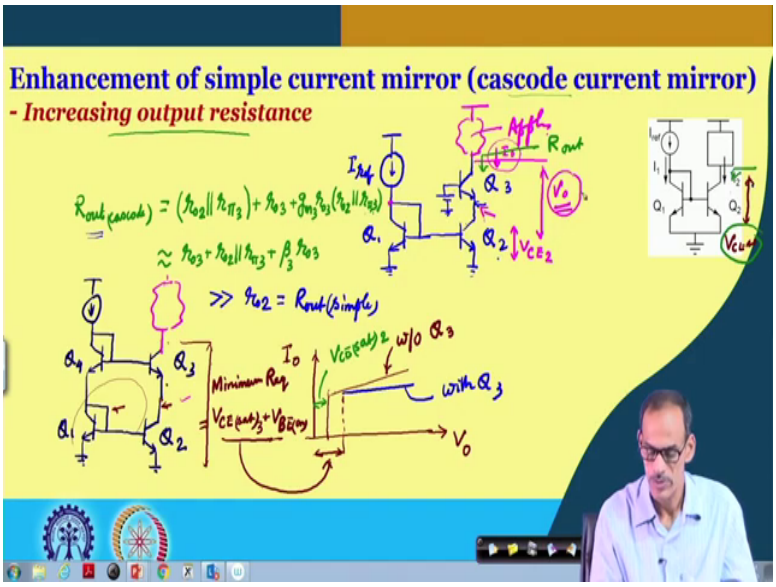
So, because of this additional this factor, this output resistance it is much higher than this case where this case the output resistance it is it was. So, this is much much higher than r ds2, which is R out of the simple one, simple current mirror. And this is the output resistance of the modified one. Since you are placing this transistor in the form of cascode, this circuit is referred as cascode current mirror.

And as I said that main advantage here it is that we are getting output resistance it is very high. As a result, the output current it hardly depends on the output voltage here or whatever the application circuit current it can be well defined by this ratio. Basically, from this one we can get the current which is independent of this output voltage.

The practical circuit, it is having slight modification instead of having independent bias here, we prefer to have that bias free so we can place one more transistor in diode connected form in the left branch to create a bias for transistor-3. So, we can have the left branch like this. So, this is M 1 which is biasing M 2 here and then we do have M 3 here, M 3 it is getting biased from this fourth transistor which is also diode connected. And of course, on top of this one we do have the application circuit.

So, this is rather very common circuit. Only advantage only disadvantage of this circuit over the simple current mirror is apart from requiring more transistor, the minimum required voltage over which we can maintain this constant current it will be higher for the for the cascade cascode current mirror, compared to minimum required voltage for the simple current mirror.

(Refer Slide Time: 39:52)



So, in the same way if you consider the BJT version, so there also we do have the possibility of improving the output impedance by the means of cascode structure; and here again, the purpose to a have cascode it is to improve the output resistance and as you can guess, that we do add one extra transistor on top of this Q 2. So, let you call this is Q 3.

We may have a meaningful voltage here, when I say meaningful voltage, it is basically what you are saying is that the voltage here it should be such that transistor-2 it is in active region

of operation. We do have I ref then, this is connected to V dd and then we do have the application circuit here.

So, this is the application circuit and this is the output voltage, this is the current flowing through this circuit. So, for this circuit again, if you analyze it can be said that this output voltage it is having hardly any influence on this voltage or it is having hardly any influence on the V CE2 voltage.

As a result, the current flow through this transistor or the final current, it hardly depends on this output voltage or you can say that the output resistance it is in this case, output resistance looking into the collector, it is much higher than the output resistance of this circuit. In fact, if I consider this structure which is referred as the cascode current mirror, as you can guess this output resistance of the cascode circuit, it is equal to r o of transistor-2 in parallel with r pi.

So, this is of course, we have to consider r pi 3. And then we do have r o of transistor-3, then plus g m3 r o3 then r o2 in parallel with r pi3. In fact, this can be well approximated by this r pi3 here. And so, we can say this is r o3 plus r o2 in parallel with r pi3.

And this part g m and this one we can see it is Beta 3 into r o3. Which is definitely much higher than this is much much higher than r o2, which is the output resistance of the simple current mirror. So compared to simple current mirror, the corresponding output resistance it is much higher.

And if you observe the variation or dependency of the output current for the 2 cases namely, a simple current mirror and cascode current mirror, on the output voltage V O. For simple current mirror, based on the early voltage, it may be having significant dependency, whereas, for this case for this case the dependency it will be much smaller.

So, this is with Q 3 and this is without Q 3. And the practical circuit practical circuit for this cascode current mirror similar to BJT, here we use one more transistor in the left branch to create a bias for transistor-3. And then of course, we do have the below transistor and then we

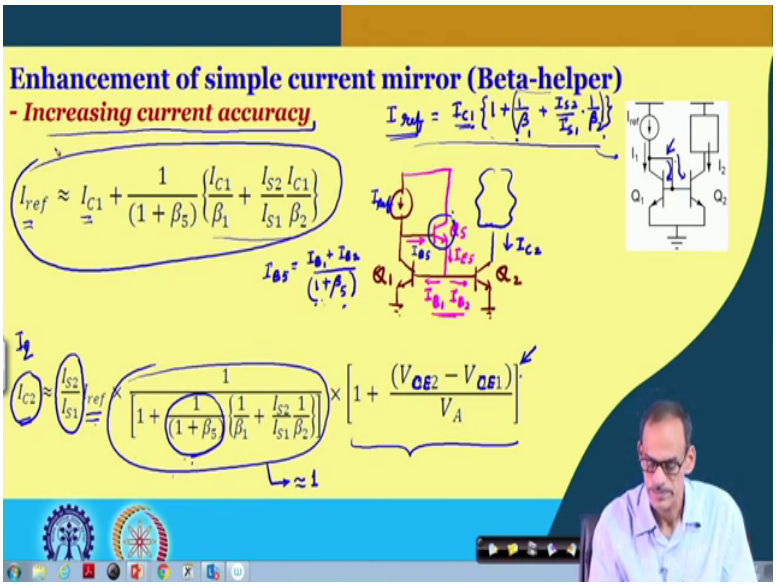
do have the Q 2. This is Q 1, this is Q 3, this is Q 4 and then we do have the reference current here. And of course, we do have the application circuit, it is here.

Now, this is the this is I should say more practical circuit. Now if I compare the 2 circuits, definitely I am getting higher resistance in this case. But the only drawback here it is the minimum required voltage to get this benefit it is higher namely, for this case we require one V CE or rather V CE sat.

So, minimum required voltage that is equal to V CE sat here or Transistor-3 plus this voltage. And in fact, that voltage if I go through this loop, it can be shown that this voltage and this voltage they are equal. So, that is 1 V BE on. Whereas for this simple current mirror, the minimum required voltage here it was only V CE sat. So, that is the only you know limitation. So, we do have a requirement here it is V CE sat plus V BE on.

Whereas, for the other circuit for this circuit we require only V CE sat, V CE sat of transistor-2. So, that is how we can increase the output resistance and we can get the less dependency of the output current on the output voltage.

(Refer Slide Time: 47:30)



So the other factor, other non-ideality factor, namely, dependency on beta you may recall that in the expression of the final current, particularly, for the BJT based circuit there are some loss of the reference current because, it is supplying the I B here and I B here and the relationship of I reference with I C1, it was I reference equal to I C1 multiplied by 1 plus 1 by beta 1 plus I S2 divided by I S1 into 1 by beta 2. This is the case for the simple current mirror.

Now, to avoid this loss or to reduce this loss, what we can do? We can place one transistor here, we can place one transistor here, which may work as current amplifier which is referred as Beta-helper circuit. So, the circuit is like this. We do have the reference current then we do have lower one, the Q 1 and also the Q 2.

Similar to the previous case Q 1 and Q 2, but in addition to that, we do have one extra transistor which is increasing this current here. So, if the base current here it is say, I B1 and this is I B2 which is emitter current of this transistor. So, let me call this is Transistor-5 and I E of transistor-5, it is summation of this 2 current.

So, the current at the base of this transistor it is ah, I can say this is I B5. And I B5 equals to I B1 plus I B2 divided by 1 plus beta of the transistor. So, we can say that by adding this extra transistor, the loss of this current loss of this reference current; if I say that is the loss, then that is getting reduced by this factor. As a result, the relationship between I ref and I C1, instead of this equation, in this part, you will get a factor which is 1 plus beta 5.

So, this is the corresponding relationship. I ref equals to I C1 multiplied by this factor and then this part. So, what is its consequence? The final expression of this I 2 or I C 2, if I say this is the I C2 and then we do have the application circuit here. And so, it is having I S2 divided by I S1 multiplied by I ref and then this factor, we can see it is getting improvised by adding this 1 plus beta of transistor-5. And this part however, it is remaining as is once again, sorry, this would be V CE2 minus V CE1.

So this part, we already have discussed to improve this one we can put the cascode structure. In addition, we can put this transistor to make this non-ideality factor very very close to 1. So, this is referred as beta-helper circuit by the beta of this transistor we are making this factor more towards the ideal one. So, that is why it is referred as beta-helper circuit.

So, that is the expression of the final current, whatever you see, I O or I 2. I think these are the 2 possible way of improving the circuit and by doing this, as I said that non-ideality factor it is going close to 1. In other words, beta-helper circuit it increases the accuracy of the current.

(Refer Slide Time: 53:01)

Now to summarize, what are the things we have discussed in the this lecture, we have started with motivation of going for current mirror namely, the to implement current biasing element in amplifier, we require the current mirror. And we also have discussed about basic characteristic namely, output impedance of the current bias element or current biasing element should be as high as possible.

And in addition to that, the current mirror also works as signal mirroring circuit. Later, we will be talking about how it is really doing that. But just to give a hint, that it also have good application in current mode amplifier to mirrored signal; not only mirroring signal, it also helps to amplify current mode signal.

Then we have talked about the basic structure of current mirror and to get the basic structure, we have discussed about various versions of current biasing elements, namely simply

registered and then leading to active device, and then we are we have discussed about the final version which is current mirror.

And the structurally, current mirror it is having a current reference followed by a mirror pair transistor. And then after the break, we have discussed more detail about the expression of the output current. So, we have gone through detailed circuit analysis and we have derived the expression of output current of a current mirror in terms of reference current, and then aspect ratio or the reverse saturation current ratio.

Then we also have talked about the output resistance and then finally, we have talked about advancement of current mirror namely, cascode current mirror and also, so, this is for both BJT and MOS and then also we have talked about beta-helper. So, beta-helper, it it improves the non-ideality factor. Second non-ideality factor of BJT current mirror due to the whatever the loss it was having in the base bias.

So, I think that is all we have discussed, we yet to discuss 1 more item small-signal model of current mirror. That it will be discussed in the next lecture along with other topic.

Thank you for listening.