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**Lecture – 69**  
**Multi-Transistor Amplifiers: Amplifier with Active Load (Contd.) – Numerical Examples (Part B)**

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**Performance comparison with CE amplifier with Passive load**

•  $V_{CC} = 12V$ ;  $\beta = 100$ ;  $V_{BE(on)} \approx 0.6V$ ;  $R_B = 570k\Omega$ ;  $R_C = 3k\Omega$ ;  $C_\pi = 10\text{ pF}$ ;  $C_\mu = 5\text{ pF}$

$V_A \approx 100V$

Ckt load	$A_v$	$R_{in}$	$R_o$	$C_{in}$	B.W. (3-dB)
Active	1923	1.3 k $\Omega$	25 k $\Omega$	9.63 nF	63.63 kHz
Passive	218	1.3 k $\Omega$	2.8 k $\Omega$	1.16 nF	56.2 kHz

$r_o = 50k\Omega$ ,  $R_o = 3k\Omega \parallel 50k\Omega = 2.8k\Omega$   
 $A_v = g_m \times R_o = \frac{1}{f_3} \times 2.8 \times 10^3 = 218$

So, welcome back after the break. So, we are talking about the CE amplifier with active load and passive load and we have discussed about their performance and we have compared their performance. Now, before we go into common source amplifier, we must make a note of the common emitter amplifier and the circuit we have discussed particularly its stability issue of its operating point.

So, in the next slide, what we will be talking about on that issue first, then we will be explaining its solution.

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**CE amplifier with active load having stable bias**

- $\beta_1 = 100$ ;  $\beta_2 = 200$ ;  $V_{BE(ON)1} \approx V_{BE(ON)2} \approx 0.6V$ ;
- $V_{A1} = 100V$ ;  $V_{A2} = 100V$ ;  $C_{\pi 1} = C_{\pi 2} = 10 \text{ pF}$ ;  $C_{\mu 1} = C_{\mu 2} = 5 \text{ pF}$
- $V_{CC} = 12V$ ;  $R_{B1} = 570k\Omega$ ;  $R_{B2} = 1.14M\Omega$ ;  $C_L = 100pF$

> Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$   
 > Find the Upper Cutoff frequency

$$I_{C1} = I_{C2}$$

$$\left(1 + \frac{V_{CE1}}{V_{A1}}\right) = \left(1 + \frac{V_{EC2}}{V_{A2}}\right)$$

$$\frac{V_{CE1}}{V_{CE2}} = \frac{V_{A1}}{V_{A2}} = \frac{1}{2} \Rightarrow V_{CE2} = 2 V_{CE1}$$

6V → 4V

So, to start with suppose, we do have see this circuit what we have discussed before. And in case say the early voltage of the two transistors they are not consistent with whatever we have planned and or in case if there is any variation of one of these two bias resistors or maybe beta of the 2 transistors if they are changing either with time or whatever it is may be due to temperature or due to aging effect that it will directly affect the operating point here.

You may recall whenever we have picked up the value of this  $R_{B2}$ , it is picked up based on the mismatch of this two beta, but of course, we are assuming the early voltage of the two transistors they are equal. So, the  $R_{B1}$  and  $R_{B2}$  difference if you see it is just to compensate the beta difference of the truth of transistor. Now let you imagine a case that is

suppose all the things are same, but then suppose this early voltage it got changed from say it 100 to maybe 200.

Then this voltage if this is getting changed to 200. Then  $1 + V_{CE1}$  divided by  $V_{A1}$  is equal to  $1 + V_{CE2}$  of transistor 2 divided by its early voltage ok. So, then so, here we have assumed that beta difference it is getting compensated by appropriate selection of the  $R_{B1}$  and  $R_{B2}$ . So, then by equating the current here and current here, what do you obtain it is that  $I_{C1}$  equals to  $I_{C2}$ .

So, that gives us this relationship between  $V_{CE1}$  and  $V_{CE2}$ . So, from this we can see that  $V_{CE1}$  divided by  $V_{CE2}$  equals to  $V_{A1}$  divided by  $V_{A2}$ . And here we said that it got changed from on this particularly, early voltage of transistor 2 got changed from 100 to 200 and hence it is 1 by 2. So, that gives us  $V_{CE2}$  equals to 2 times of  $V_{CE1}$ .

On the other hand; the summation of the two  $V_{CE}$  and  $V_{CE}$  together it is equal to 12 volt. So, from that you can say that maybe this is then it will be converging to a meaningful value, say this is 8 volt and this is 4 volt satisfying this condition and also summation of this one, it is equal to 12 volt.

So, in case if the early voltage it is getting changed to 200, the voltage DC voltage at the output node it is getting changed from 6 volt to 4 volt. Still both the devices are in active region of operation, but off course the DC voltage got changed and as a result the swing, negative side swing it is getting affected compared to the positive side. So, but of course, you may still say that both the devices are in active region of operation and the gain may be very good and so and so. The problem it will be even more severe particularly, if I consider if the beta is getting changed and rest of the things are remaining same.

Say for example, we anticipated that the beta it will be 200 and if this 200 it is getting changed to say maybe 180, then what happens? Let me clear the space and then let me explain that situation.

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**CE amplifier with active load having stable bias**

- $\beta_1 = 100$ ;  $\beta_2 = 200$ ;  $V_{BE(on)1} \approx V_{BE(on)2} \approx 0.6V$ ;
- $V_{A1} = 100V$ ;  $V_{A2} = 100V$ ;  $C_{\pi 1} = C_{\pi 2} = 10 \text{ pF}$ ;  $C_{\mu 1} = C_{\mu 2} = 5 \text{ pF}$
- $V_{CC} = 12V$ ;  $R_{B1} = 570k\Omega$ ;  $R_{B2} = 1.14M\Omega$ ;  $C_L = 100pF$

> Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$   
 > Find the Upper Cutoff frequency

$I_{B2} = 10\mu A$   
 $I_{B1} = 20\mu A$   
 $V_{CE1} + V_{EC2} = V_{CC} = 12V$

$2.4 - 0.38 V_{EC2} = -2 \rightarrow I_{B1} = 20\mu A$   
 $V_{EC2} = \frac{4.8}{0.38} = 12.6$   
 $100 \times 20\mu A \left(1 + \frac{V_{CE1}}{V_{A1}}\right) = 180 \times 10\mu A \left(1 + \frac{V_{EC2}}{V_{A2}}\right)$  KCL  
 $20 \left(1 + \frac{V_{CE1}}{V_{A1}}\right) = 18 \left(1 + \frac{V_{EC2}}{V_{A2}}\right)$   
 $2 + 0.2 V_{CE1} = 0.18 V_{EC2}$   
 $0.2 \{12 - V_{EC2}\} - 0.18 V_{EC2} = -2$

So, suppose this beta it is getting changed to 180 and let you assume that rest of the things are same, namely;  $V_{BE2}$  and  $V_{BE1}$  are remaining same as whatever you have planned and this is giving us  $I_{B2}$  equals to 10 micro ampere and this is giving us  $I_{B1}$  equals to 20 micro ampere.

So, what we have then beta 1 which is 100 multiplied by this 20 micro ampere multiplied by 1 plus  $V_{CE1}$  divided by  $V_{A1}$  should be equal to 180 multiplied by 10 micro ampere multiplied by 1 plus  $V_{EC2}$  divided by  $V_{A2}$ . And also we know that  $V_{CE1}$  equals to sorry, we can say that summation of these two  $V_{EC2}$  is equal to  $V_{CC}$ . In fact, this is KVL and on the other hand this is KCL at this node.

Now, because of this change, all of a sudden what we have here it is if I consider this two left and right side and what you are getting here it is 20 into 1 plus  $V_{CE}$  divided by  $V_{A}$  equals



to 18 multiplied by  $1 + V_{CE2} / V_{A2}$ . So, of course, these two are equal. So, we can say they are 100 and so this gives us  $2 + 20$ . So that is  $0.2 V_{CE1}$  equals to  $0.18 V_{CE2}$ . And then also we do have this equation and this is equal to 12 volt.

So, now by putting the expression of  $V_{CE1}$  into  $V_{CE2}$  or vice versa. You can get the value of the  $V_{CE1}$ . So, let me take this here, so this is equal to 0.2,  $V_{CE1}$  equals to 12 volt minus  $V_{CE2}$ , then this is equal to minus 0.18  $V_{CE2}$  equals to minus 2 all right. And then what we are getting here it is further simplifying we do have point. So, this is 0.38  $V_{CE2}$  and then here we do have 0.2. So, that is 2.4.

So, from here what we are getting it is 2.4 minus 3 point sorry, 0.38  $V_{CE2}$  equals to minus 2 or we can say that  $V_{CE2}$  equals to 4.8 divided by 0.38 well right. I think I am correct. So, if you calculate this 4.8 divided by; 4.8 divided by 0.38. So, that gives us 12.6, it is impractical.

Because if we have this voltage which is more than 12 volt; that means, that the corresponding transistor here is not having any headroom here. So, this is not possible. So, practically what happens is that, this voltage goes down, down and then pushing this transistor 1 into saturation region and then its current corresponding current here it gets reduced till it is matching with the current here. So, this kind of small change; say 10 percent reduction of the beta of transistor 2, it creates the situation where one of this transistor it is entering into saturation region.

There is no surprise because, the circuit gain it is we have increased as a result we are making the output node very sensitive to variation it is not only sensitive to signal voltage, but also to parameters. And whenever one of this parameter particularly say, beta or maybe likewise you can consider this resistance it is varying then the output voltage DC voltage it is getting changed. So, we can say that this original circuit even though it is having advantage of getting high gain its output node voltage it is very unstable and it is very sensitive rather is very sensitive to beta of the 2 transistors.

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### CE amplifier with active load having **stable bias**

- $\beta_1 = 100$ ;  $\beta_2 = 200$ ;  $V_{BE(on)1} \approx V_{BE(on)2} \approx 0.6V$ ;
- $V_{A1} = 100V$ ;  $V_{A2} = 100V$ ;  $C_{\pi 1} = C_{\pi 2} = 10 \text{ pF}$ ;  $C_{\mu 1} = C_{\mu 2} = 5 \text{ pF}$
- $V_{cc} = 12V$ ;  $R_{B1} = 570k\Omega$ ;  $R_{B2} = 1.14M\Omega$ ;  $C_L = 100pF$ 
  - Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$
  - Find the Upper Cutoff frequency  $\approx 570 \text{ k}\Omega$

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So, what may be the remedy for that? So, here we do have the solution, it is given here. We do have the solution given here. What we have done is that? This  $R_{B2}$  instead of connecting to ground, we are connecting into the output node. And whenever in case a this beta it is getting reduced and then what we are expecting is that this voltage may be getting going towards the ground as you have seen and that makes the corresponding base current  $I_B$  current instead of a constant current, that is getting increased and then, that is making the corresponding collector current  $I_C$  it is getting increased.

So, I should say this arrangement it is having some feedback mechanism which is helping us to maintain this voltage remaining towards its middle point. But of course, at the beginning we have to make some sensible calculation and sensible you know selection of the value of the resistances.

So, of course, if you put say 1.14 mega ohm then also it will be, but I suggest that if we do have a target at this node of say 6 volt and unlike the previous case where this was connected to ground and for which we obtained the value of this resistance it was 1.14 mega ohm.

Now, instead of ground we do have a 6 volt target and the R B it is connected to this expected to be connected to 6 volt in normal circumstances. So, the selection of this R B 2 should be appropriate namely, instead of 1.14 mega ohm, this should be reduced to maybe close to half ok. Probably, close to say 570 kilo ohm.

So, with 570 kilo ohm, it may produce this current close to whatever 10 micro ampere and then with the beta of 200 the collector current it will be to the main target it was 2 milli ampere. Because the current here it is still 2 milli ampere. Now, then how do you calculate the corresponding operating point?

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**CE amplifier with active load having stable bias**

- $\beta_1 = 100$ ,  $\beta_2 = 200$ ;  $V_{BE(on)1} \approx V_{BE(on)2} \approx 0.6V$ ;
- $V_{A1} = 100V$ ;  $V_{A2} = 100V$ ;  $C_{\pi 1} = C_{\pi 2} = 10 \text{ pF}$ ;  $C_{\mu 1} = C_{\mu 2} = 5 \text{ pF}$
- $V_{CC} = 12V$ ;  $R_{B1} = 570k\Omega$ ;  $R_{B2} = 1.14M\Omega$ ;  $C_L = 100pF$

> Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$   
 > Find the Upper Cutoff frequency

$$I_{B2} = \frac{V_{CC} - V_{OUT} - V_{EB(on)2}}{R_{B2}}$$

$$2 \text{ mA} = I_{C1} = \beta_2 \times \frac{V_{CC} - V_{OUT} - V_{EB(on)2}}{R_{B2}}$$

$$R_{B2} = \frac{\beta_2 \{ V_{CC} - V_{OUT} - V_{EB(on)2} \}}{I_{C1}}$$

$$= \frac{200 \{ 12 - 6 - 0.6 \}}{2 \text{ mA}} = 540 \text{ k}\Omega$$

$\left\{ 1 + \frac{V_{CE}}{V_A} \right\} \approx 1$

Let us see that. Suppose, instead of taking this value of this resistance half of it. Suppose, this is 1 mega ohm, so that means; instead of taking 570 kilo ohm. In case if it is changing to this value and then what will be the consequence at the output voltage or maybe in case if it is say 1 mega ohm and in addition to that suppose this is getting changed then, what happens?

So, in such situation, if you consider the consider the K C L K V L equation for this loop and then if you keep this current  $I_{C1}$  which is directly obtained from its own bias and then beta then we can find a compact equation. Suppose, this output voltage is  $V_{OUT}$  then  $I_{B2}$  equals to  $V_{CC}$  minus  $V_{OUT}$  minus  $V_{EB(on)}$  of transistor 2 divided by divided by  $R_{B2}$  and so, this is the  $I_{B2}$ . So, this is  $I_{B2}$  after multiplying with beta of the transistor, we can get the corresponding collector current.

So, we can see  $I_{C1}$ , this collector current should be equal to  $\beta$  of the transistor 2 into  $I_{B2}$  which is  $V_{CC} - V_{OUT} - V_{EB}$  on divided by  $R_{B2}$  ok. Before we go into 1 mega ohm, let us try to see what may be a suitable value here. So, that this voltage it is settling to 6 volt. So, since our target here it is 6 volt. Let me put the 6 volt here and whatever the  $\beta$  we do have this current of course, it is 2 milli ampere. So, we do have 2 milli ampere of  $I_{C1}$ . So, then what we are getting it is  $R_{B2}$  equals to  $\beta$ ,  $V_{CC} - V_{OUT}$ , the target voltage minus  $V_{EB}$  on divided by whatever  $I_{C1}$ .

Note that in this calculation we are assuming that  $1 + V_{CE} / V_{EC}$  by  $V_A$ ; this part it is approximately 1. So, that is the assumption. So, if you follow this assumption, then the calculation becomes more you know handy and also practical. So, with this equation what we are getting it is  $\beta$  is equal to 200,  $V_{CC}$  is 12, this is target is 6, so that is  $6 - 0.6$  divided by 2 milli ampere.

So, that gives us 200 is getting cancelled here, we do have mega here and then we do have 5.4 into 10 to the power 5. So, that is equal to 540 kilo ohm. That is what I was anticipating that this resistance it will be coming close to its half value. So, the if we target this is a 6 volt then we can take this value equals to say 540 kilo ohms. Now if I said this value of say 540 kilo ohm and then if I say that this  $\beta$  it is getting changed to the similar quantity maybe, say 1 eighty instead of 200, then what happens?

So, now we are setting this bias registered 540 kilo ohm expecting the output voltage it will be 6 volt. But in our calculation; we have considered  $\beta$  is equal to 200, but say unfortunately, this  $\beta$  got changed to 180. Then what happens?.

So, again we can probably use this equation and instead of using this is 6, we should use we should use rather we should rather find this value for this is given as 240 k. So, what is the, how do you find the corresponding output voltage in case this  $\beta$  is changing from 200 to 180?

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**CE amplifier with active load having stable bias**

- $\beta_1 = 100$ ;  $\beta_2 = 200$ ;  $V_{BE(ON)1} \approx V_{BE(ON)2} \approx 0.6V$ ;
- $V_{A1} = 100V$ ;  $V_{A2} = 100V$ ;  $C_{\pi 1} = C_{\pi 2} = 10 \text{ pF}$ ;  $C_{\mu 1} = C_{\mu 2} = 5 \text{ pF}$
- $V_{CC} = 12V$ ;  $R_{B1} = 570k\Omega$ ;  $R_{B2} = 1.14M\Omega$ ;  $C_L = 100pF$

> Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$  →  $540 \rightarrow V_{OUT} = 6V$   
 > Find the Upper Cutoff frequency

$2 \text{ mA} = \beta_2 \left\{ \frac{V_{CC} - V_{OUT} - V_{BE(ON)2}}{R_{B2}} \right\}$   
 $V_{CC} - V_{OUT} - V_{BE(ON)2} = \frac{2 \times 10^{-3} \times 570 \times 10^3}{200} = 6$   
 $V_{OUT} = 12 - 0.6 - 6 = 5.4V$

Let we do this calculation. So, what I said is 2 milli ampere current 2 milli ampere of current equals to beta 2 multiplied by V C C minus, whatever the V OUT. We like to calculate that and then we do have V E C, not V E C, V B E, V E B, V E B on 2 divided by R B 2. Now from this we need to calculate this V OUT. So, we do have V C C minus V OUT minus V E B on. So, that is equal to 2 milli ampere, 2 to the power, 2 into 10 to the power minus 3 multiplied by 540 k, 540 into 10 to the power 3 divided by beta, beta is now 180.

So, this part what we have it is, this is getting cancelled when this 0, 1 this 0 it is getting cancelled this is 9 and then, so it becomes 6. So, this is becoming 6, then that gives us V OUT equals to V C C minus V E B 2. So, that is 12 volt minus 0.6 and then you have 6. So, we do have 6 minus 0.6, so that is equal to 5.4 volt find forward. So, what is the conclusion here it is

that we started with this  $R_B$  equals to 540 expecting that beta it will be 200 and the corresponding  $V_{OUT}$  expected  $V_{OUT}$  it was 6 volt.

Now, the beta got changed, this beta got changed to 180. So, that is what we have taken here it is 180 and due to that the corresponding  $V_{OUT}$  got changed only to 5.4. So, this is a demonstration that since this resistance it is connected to the output node it is creating some feedback mechanism. So, that this output voltage remain insensitive to this bit of variation right. Now if we put this register here connected to the output node, off course it will be having a consequence on the voltage gain.

So, to take care of that we can put a capacitor here. So, that for signal this node base node should not be having any signal. The signal should be getting bypassed by this capacitor only. However, this register since it is connected here that will maintain the operating point stability ok. Probably, I do have the corresponding calculation for that let me try to see in the next slide.

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**CE amplifier with active load having stable bias**

- $\beta_1 = 100$ ;  $\beta_2 = 200$ ;  $V_{BE(on)1} \approx V_{BE(on)2} \approx 0.6V$ ;
- $V_{A1} = 100V$ ;  $V_{A2} = 100V$ ;  $C_{\pi 1} = C_{\pi 2} = 10 \text{ pF}$ ;  $C_{\mu 1} = C_{\mu 2} = 5 \text{ pF}$
- $V_{cc} = 12V$ ;  $R_{B1} = 570k\Omega$ ;  $R_{B2} = 1.14M\Omega$ ;  $C_L = 100pF$

> Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$   
 > Find the Upper Cutoff frequency  $\approx 70 \text{ kHz}$

$$|A_v| = g_{m1} (r_{o1} \parallel r_{o2} \parallel R_{B2})$$

$$= \frac{1}{13} \left\{ \frac{25k\Omega \parallel 540k\Omega}{23.89 \times 10^3} \right\}$$

$$\approx \frac{23.89 \times 10^3}{13} \approx 1838$$

$R_{out} = 25k \parallel 540k = 23.89k\Omega$

So, here we do have the circuit where we do have this feedback arrangement namely  $R_B$  got connected to the output node and also we do have this capacitor to fill make the base node not affected by signal coming through this resistor.

So, here we do have the small signal equivalent circuit. It to it was it is actually very similar to the previous case except this  $R_{B2}$ , it is connected to the output node. And also this node it is connected to supply voltage. We may say that this is AC ground or simply you can say this is getting shorted. So, that makes this  $V_{B2}$  equals to 0, that makes this signal is 0. Leaving behind whatever the circuit we do have before it is this circuit is also becoming identical to that except off course this  $R_{B2}$  it is coming in parallel with  $r_{o2}$  and  $r_{o1}$ .

And what is this consequence? The voltage gain  $A_V$  it becomes  $g_{m1}$ ,  $r_{o1}$  in parallel with  $r_{o2}$  in parallel with  $R_{B2}$ . And we have calculated the value of this  $g_m$  and  $r_{o1}$  and  $r_{o2}$ .



So, here we can put those values here. So, this is getting multiplied by this is 50 k, this is 50 k, so together it is 25 k in parallel with 540 k.

Of course, there will be some consequence here, but since this register it is getting dominated. I should say that will be having hardly any difference. In fact, let me do the calculation for you. In fact, we can directly calculate the corresponding  $V$  out which is 25 k in parallel with 540 k. So, how much is it? So, we do have 540 k divided by 565 into 25.

So, that is equal to 23.89 kilo ohm. So, we can say that this whole portion it is becoming 23.89 into 10 to the power 3 divided by 23 sorry 13. So, that is equal to 1838. So, unlike the previous case where it was 19, something it was there. It got slightly decreased because you do have this resistance coming in to coming in to the picture and that degrades the gain slightly.

But rest of the things it is remaining almost same of course, since this gain got changed slightly it will be having impact on this input capacitance upper cut off frequency also it will be having slight change because the output resistance it is getting changed, but still it will be in the range of say 60 close to say, maybe 70 kilo Hertz. So, the upper cut off frequency it will be in this range.

So, I think you yourself can calculate that and now going to the similar kind of exercise for common source amplifier.

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### Numerical example: CS amplifier with active load

- $(K_n \cdot W_1/L_1) = 1 \text{ mA/V}^2$ ,  $(K_p \cdot W_2/L_2) = 4 \text{ mA/V}^2$ ;  $V_{th1} = 1 \text{ V}$ ,  $V_{th2} = -1.5 \text{ V}$ ,  $\lambda_1 = \lambda_2 = 0.01 \text{ V}^{-1}$ ,
- $C_{gs1} = C_{gs2} = 10 \text{ pF}$ ;  $C_{gd1} = C_{gd2} = 5 \text{ pF}$
- $V_{DD} = 12 \text{ V}$ ,  $R_{11} = 9 \text{ k}\Omega$ ,  $R_{12} = 3 \text{ k}\Omega$ ,  $R_{21} = 95 \text{ k}\Omega$ ,  $R_{22} = 25 \text{ k}\Omega$ ,  $C_L = 100 \text{ pF}$

> Find operating points and values of small signal parameters of transistors  
 > Find Output swing (distortion free output signal)

$(1 + \lambda_1 V_{DS1}) = (1 + \lambda_2 V_{DS2})$   
 $M_1: V_{GS} - V_{th1} = 3 - 1 = 2 \text{ V}$   
 $M_2: V_{GS} - |V_{th2}| = 2.5 - 1.5 = 1 \text{ V}$   
 $I_{DS1} = \frac{K_n}{2} (V_{GS} - V_{th1})^2 = 2 \text{ mA}$   
 $I_{DS2} = 2 \text{ mA}$   
 $g_{m1} = 2 \text{ mA/V}$   
 $g_{m2} = 4 \text{ mA/V}$   
 $r_{ds1} = r_{ds2} = \frac{1}{\lambda I_D} = 50 \text{ k}\Omega$

So, we do have here the common source amplifier circuit and we do have the corresponding bias resistors and all. So, if you see this circuit; we do have let me use blue colour, no black colour is fine. So, we do have this register it is 9 k, this resistance it is 3 k. So, that gives us this volt is equal to 3 volt. On the other hand we do have 25 k here and we do have 95 k here.

In fact, intentionally, I have taken different value of this transconductance factor for transistor 1 and transistor 2. For transistor 1; we do have 1 milli ampere per volt square whereas, for this transistor; we do have 4 milli ampere per volt square. Now again for this case it is I D S current of the 2 transistors should be equal. So, to compensate this difference we require different value of V G S minus V t h for the 2 transistors. Also I have taken threshold voltage of the 2 transistors different. One is 1 volt here for transistor 1 and then for transistor 2 it is minus 1.5.

So, to compensate this trans conductance factor difference, here we like to have different  $V_{GS} - V_{th}$ . So, you might have noticed that for transistor 1  $V_{GS} - V_{th}$  equals to 3 minus 1, that is equal to 2 volt. On the other hand for transistor 2;  $V_{GS} - V_{th}$ , I have taken so this is 2.5 minus 1.5. So, that is equal to 1 volt. So, to calculate the current which is  $k_n W/L$  and by 2 multiplied by  $V_{GS} - V_{th}$  square.

Since this part, this part it is different for the 2 transistors; they are getting compensated by this one. And here the difference ratio it is 4. So, the  $V_{GS} - V_{th}$  ratio since it is square, it is 2. So, that is how it has been picked up the values of these resistors. I am sharing this information so, that is in case if you have to design this circuit namely in case if you have to find the value of the resistors from this information, then you will be getting a hint how to calculate the or how to get the DC voltage here and then how to get the value of the resistors.

Note that the value of  $R_{22}$  and  $R_{21}$  it is quite different from  $R_{11}$  and  $R_{12}$ , that is again it is just intentional, but since its gate leakage it is ignorable namely, gate to source resistance it is you can consider infinite then the value of these resistances are absolute value of the resistances are not really important, the ratio is important ok.

So, anyway what we obtain in the fate it is  $I_{DS1}$  equals to say 1 milli ampere divided by 2 into  $V_{GS} - V_{th}$  which is 2 volt square. So, 1 milli per volt square, this is 2 volt square. So, that gives us 2 milli ampere. In fact, you can also find that  $I_{SD}$  of transistor 2 it is also 2 milli ampere right.

And from that you can calculate the small signal parameter, but before that the output voltage to get the DC output voltage since these 2 parts of the 2 transistors they are equal. And to get the DC output voltage, I need to consider  $1 + \lambda_{V_{DS}}$  of the 2 transistors and if I equate them namely  $1 + \lambda_{V_{DS1}}$  and to  $V_{DS}$  and  $\lambda_{V_{DS2}}$  into  $V_{SD2}$ .

So, that gives us since the both the  $\lambda$ s are equal. So, that gives us  $V_{SD2}$  equals to  $V_{DS1}$ . However, summation of these 2 quantity it is equal to  $V_{DD}$  which is 12 volt. So, that gives us both of them are equal to 6 volt. So, that gives us this voltage it is 6 volt and hence

we obtain the corresponding operating point. Now from that we can say if this is 6 volt, we do have the voltage at this node it is we do have 12 volt and this drop it is 2.5 volt. So, the voltage here it is 9.5 volt.

So, positive side swing wise, positive side you can say that the signal can go from this 6 volt DC till 1 this transistor 2 entering into the saturation region, rather going out of the saturation region. So, what will be the limit the gate voltage it is 9.5 plus its magnitude of this threshold voltage. So, that is becoming 11 volt. So, the upper limit of the output voltage it is 11 volt that we obtained by considering its gate voltage plus magnitude of this 1.5.

On the other hand; lower side we do have 3 volt here DC and then minus  $V_{th}$  of transistor 1 which is 1 volt. So, this voltage it can go as low as 2 volt. So, the swing wise; if I say that positive side we do have output swing positive side it is 5 volt 11 minus 6. So, that is equal to 5 volt and then negative side, we do have 6 volt minus 2 volt. So, that is equal to 4 volt ok.

So, this is what the basic difference compared to the BJT version and this MOS version and then we can go for the small signal parameter calculation. In fact, we have done before. So, if I consider this  $I_{D,S}$ , then what you obtain it is  $g_{m1}$ ; it is 2 milli ampere per volt. On the other hand  $g_{m2}$  is equal to 4 milli ampere per volt and then  $r_{o1}$  equal to  $r_{o2}$  both of them are equal to 50 k.

Why 50 k? If I consider this  $\lambda$  and the corresponding  $I_{D,S}$ . So, both of them this resistors are  $1/\lambda$  into the corresponding  $I_{D,S}$ . So, that gives us 50 kilo ohm. So, from that we can find gain. In the next slide we do have the gain calculation sorry.

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### Numerical example: CS amplifier with active load (contd.)

- $(K_n \cdot W_1/L_1) = 1 \text{ mA/V}^2$ ,  $(K_p \cdot W_2/L_2) = 4 \text{ mA/V}^2$ ;  $V_{th1} = 1 \text{ V}$ ,  $V_{th2} = -1.5 \text{ V}$ ,  $\lambda_1 = \lambda_2 = 0.01/\text{V}$ ,
- $C_{gs1} = C_{gs2} = 10 \text{ pF}$ ;  $C_{gd1} = C_{gd2} = 5 \text{ pF}$
- $V_{DD} = 12 \text{ V}$ ,  $R_{11} = 9 \text{ k}\Omega$ ,  $R_{12} = 3 \text{ k}\Omega$ ,  $R_{21} = 95 \text{ k}\Omega$ ,  $R_{22} = 25 \text{ k}\Omega$ ,  $C_L = 100 \text{ pF}$

> Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$   
 > Find the Upper Cutoff frequency

$$|A_v| = (g_{m1} \parallel r_{ds1} \parallel r_{ds2})$$

$$= 2 \text{ mA/V} \times 25 \text{ k}\Omega$$

$$= 50$$

$$C_{in} = 10 + 5 \times (50 \text{ pF}) = 265 \text{ pF}$$

$$R_{in} = 3 \text{ k}\Omega \parallel 9 \text{ k}\Omega = 2.25 \text{ k}\Omega, \quad f_U = \frac{1}{2\pi(R_{in} \parallel r_{ds1} \parallel r_{ds2})C_L} = 63.63 \text{ kHz}$$

So, we do have the small signal equivalent circuit given here. It is very similar to on the B J T version except of course, we do not have any  $R_{pi}$ . So, the calculation here it is I should say simpler and since this node it is connected to A C ground. So, the voltage here it is 0. So, that makes this current equal to 0, leaving behind the circuit is having only  $r_{ds1}$  and  $r_{ds2}$  in parallel and then this current incident incidentally  $V_{gs1}$  equals to this  $V_{in}$ .

So, the output voltage it is  $g_{m1}$  multiplied by  $r_{ds1}$  in parallel with  $r_{ds2}$  with a minus sign and then of course, that is  $V_{gs1}$  which is  $V_{in}$ . So, that gives us the voltage gain equals to  $g_{m1}$  multiplied by  $r_{ds1}$  in parallel with  $r_{ds2}$  which is equal to 2 milli ampere per volt multiplied by this is 25 kilo ohm, so that is equal to 50. Of course, this gain it is not so high. Mainly because its corresponding  $g_{m1}$  it is quite low, but at least we can say that the gain got increased.

So, likewise you can calculate the input capacitance. So, C in you can calculate. In my calculation; it is coming that is 10 plus 5 into 50 plus 1. So, that is equal to 5, 60 sorry, 265 pico Farad and ok. So, input resistance of course, it is just parallel connection of this R 1 1 and R 1 2. So, that is very simple that is coming 3 k in parallel with 9 k and I guess it will be 2.25 k ok.

And the upper cut off frequency f u, which is 1 by 2 pi this r d is 1 in parallel with r d s 2 which is r o multiplied by C L, C L it is connected here and the C L it is again 10 100 pico Farad and this is earlier we have done this calculation. This upper cut off frequency it is 63.63 kilo Hertz. Now, if you compare these performances with the standard one namely circuit with passive load.

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### Comparison with CS amplifier having passive load

•  $(K_n W/L) = 1 \text{ mA/V}^2$ ;  $V_{th} = 1 \text{ V}$ ,  $V_{dd} = 12 \text{ V}$ ,  $R_1 = 9 \text{ k}\Omega$ ,  $R_2 = 3 \text{ k}\Omega$ ,  $R_D = 3 \text{ k}\Omega$ ;  $C_L = 100 \text{ pF}$

Ckt load	$A_v$	$R_{in}$	$R_o$	$C_{in}$	B.W.
Active	50	2.25 k	25 k	265 pF	63.63 kHz
Passive	5.66	2.25 k	2.83 k	43.3 pF	562 kHz

$g_m = 2 \text{ mA/V}$ ,  $R_o = R_D \parallel r_{ds} = 2.83 \text{ k}$   
 $A_v = 5.66$

So, in the next slide we do have the circuit to compare with. So, what we said for common source amplifier with active load. The gain it was 50,  $R_{in}$ ; it was 2.25, I guess it is readable. Let me use the different colour then. So, we do have 50 here,  $R_{in}$ ; it is 2.25 k,  $R_o$ ; it was 25 k,  $C_{in}$ ; it was 265 pico Farad and then bandwidth it was 63.63 kilo Hertz. If you compare the common source amplifier having passive load and if its bias condition it is equivalent namely here we have taken 9 k and here it is 3 k and the resistance here it is 3 k.

So, that gives us this  $I_{DS}$  current of 2 milli ampere and hence the corresponding  $g_m$  it is also 2 milli ampere per volt. Output resistance; it is  $R_D$  in parallel with the  $r_{ds1}$  or  $r_{ds}$  which is 50 k. So, that is coming 3 k in parallel with 50 k. So, that is equal to 2.83 k. So, that gives us the voltage gain equals to 5.66. So,  $g_m$  into this one. So, the voltage gain here it is 5.66 input resistance it is parallel connection of this bias resistors. So, that is remaining 2.25 k.

Output resistance as we have calculated here it is 2.83 k.  $C_{in}$ , on the other hand it is we do have 10 here and then 5 multiplied by 6.66, 1 plus  $A/V$ . So, that is equal to around 40, 43 to be more precise, 43.3 pico Farad.

And the bandwidth if you consider the output resistance of 2.83 and this 100 pico Farad, it is coming 562 kilo Hertz. Earlier we have calculated, but you also can check it. So, what we have seen here it is that gain got increased by this active load. However, the 3 dB bandwidth got decreased right and then input capacitance of course, it got increased ok. And this increase and this decrease, they are having the same factor mainly due to the change of this output resistance.

So, if I am having say circuit with passive load the gain it is very low and then also it is having some bandwidth and then with active load the gain got increased, but then bandwidth got decreased and their gain bandwidth product; however, remaining same. So, this is the comparison of the common source amplifier having active load versus passive load.

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**Numerical example:**  
**CS amplifier with active load having stable bias**

- $(K_n \cdot W_1/L_1) = 1 \text{ mA/V}^2$ ,  $(K_p \cdot W_2/L_2) = 4 \text{ mA/V}^2$ ;  $V_{th1} = 1 \text{ V}$ ,  $V_{th2} = -1.5 \text{ V}$ ,  $\lambda_1 = \lambda_2 = 0.01/\text{V}$ ,
- $C_{gs1} = C_{gs2} = 10 \text{ pF}$ ;  $C_{gd1} = C_{gd2} = 5 \text{ pF}$
- $V_{DD} = 12 \text{ V}$ ,  $R_{11} = 9 \text{ k}\Omega$ ,  $R_{12} = 3 \text{ k}\Omega$ ,  $R_{21} = 35 \text{ k}\Omega$ ,  $R_{22} = 25 \text{ k}\Omega$ ,  $C_L = 100 \text{ pF}$

➤ Find operating points and values of small signal parameters of transistors  
➤ Find Output swing (Distortion free output signal)

$$A_v = g_{m1} (r_{ds1} \parallel r_{ds2} \parallel R_{21})$$

$$R_o = r_{ds1} \parallel r_{ds2} \parallel R_{21}$$

$$= 2.5 \text{ k}\Omega \parallel 35 \text{ k}\Omega$$

$$= ?$$

So, here also similar to the BJT circuit, here also the stability issue is there that can be handled by the same approach namely connecting this register instead of connecting to ground we can connect these to output resistance. But then you have to suitably modify this resistance earlier it was 95 k, now we have changed this register to 35 k.

So, that this voltage with whatever the parameters are given here namely 1 milliampere per volt square for transistor 1 and then for transistor 2, this is transconductance factor it is 4 milli ampere per volt square and also threshold voltage it is we are keeping same with that this resistance need to be changed from 95 k to 35 k and with that we do get this output voltage 6 volt. This is 2.5 volt sorry, this voltage difference is 2.5 volts. So, this voltage it is rather 9.5 volt, this is a 3 volt.



So, rest of the things of the 2 circuits are remaining same except of course, this resistance coming in the expression of the  $A_V$ . So, the  $A_V$  equals to  $g_{m1} r_{ds1}$  in parallel with  $r_{ds2}$  in parallel with  $R_{21}$ . So, there will be slight decrease of the gain. So, that probably we can calculate this part it is 25 k and this part it is 35 k ok. Likewise, the output resistance also is getting changed due to this  $R_B$ ,  $R_{B21}$  and the expression of  $R_o$  it is  $r_{ds1}$ ,  $r$  in parallel with  $r_{ds2}$  in parallel with  $R_{B21}$ .

So, you can find this 25 k in parallel with 35 k right. So, you can find this value. So, I will not be going in detail of that. So, the small signal equivalent circuit you can draw.

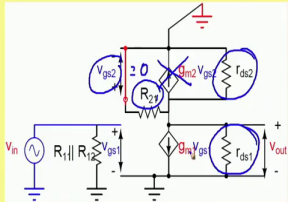
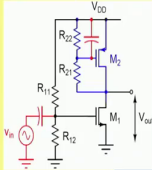
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### Numerical example: CS amplifier with active load having **stable bias (contd.)**

- $(K_n \cdot W_1/L_1) = 1 \text{ mA/V}^2$ ,  $(K_p \cdot W_2/L_2) = 4 \text{ mA/V}^2$ ;  $V_{th1} = 1 \text{ V}$ ,  $V_{th2} = -1.5 \text{ V}$ ,  $\lambda_1 = \lambda_2 = 0.01/\text{V}$ ,
- $C_{gs1} = C_{gs2} = 10 \text{ pF}$ ;  $C_{gd1} = C_{gd2} = 5 \text{ pF}$
- $V_{DD} = 12 \text{ V}$ ,  $R_{11} = 9 \text{ k}\Omega$ ,  $R_{12} = 3 \text{ k}\Omega$ ,  $R_{21} = 35 \text{ k}\Omega$ ,  $R_{22} = 25 \text{ k}\Omega$ ,  $C_L = 100 \text{ pF}$

> Find voltage gain,  $R_{in}$ ,  $R_o$  and  $C_{in}$   
 > Find the Upper Cutoff frequency



So, it is very similar, this  $V_{gs}$  it is getting changed. So, the  $V_{gs}$  it is getting changed 20 and that makes this portion equals to 0, but then this  $R_{21}$ , it is coming in parallel with  $r_{ds1}$  and  $r_{ds2}$  ok.

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**Conclusion:**

- Motivation of using active load
- Basic operation and analysis of
  - CS amplifier with active load
  - CE amplifier with active load
- Practical amplifier circuits with active load:
  - CS
  - CE
- **Numerical examples and Design guidelines**
  - CE amplifier with active load and comparison with passive load
  - CE amplifier with active load having stable bias
  - ✓ CS amplifier with active load and comparison with passive load
  - ✓ CE amplifier with active load having stable bias

So, in summary or in conclusion, what we have done here it is; primarily, numerical examples we have discussed and numeric today we have extensively discussed about numerical examples that also gives you a slight inside of the design guidelines and what we have discussed here it is common emitter amplifier with active load and its performance it has been compared with common emitter amplifier having passive load.

So, we have done the comparative performance comparison to motivate why we go for active load. You also have discussed about the common name, how do you take care of the stability issue that may be arising due to the active load making the output voltage a very sensitive. So,

similarly, for similar to the BJT for MOS transistor also we have seen common source amplifier with active load and its performance it has been compared with common source amplifier with passive load. And also here we have discussed about the stability issue and how to resolve that issue. I think that is all I do have to share.

Thank you for listening.