Analog Electronic Circuits
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Lecture – 67
Multi-Transistor Amplifiers: Amplifier with Active Load (Part B)

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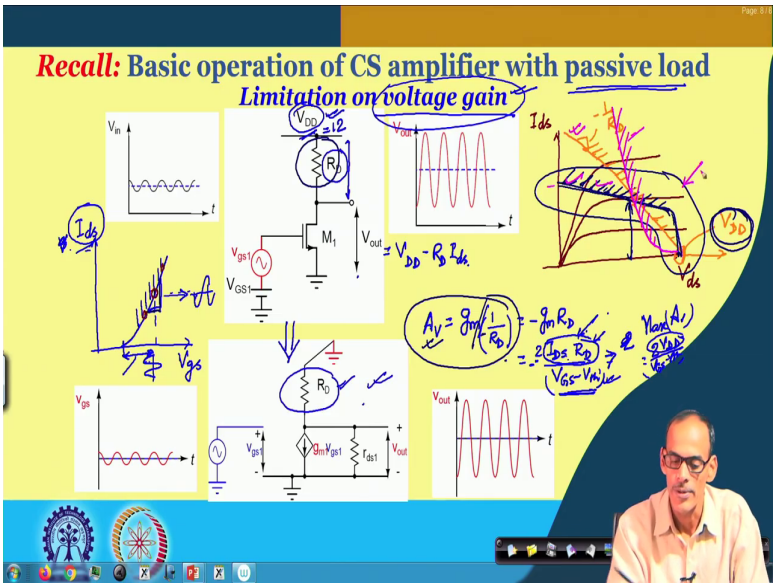

Yeah. So, welcome back after the short break. And we were discussing about the limitation of the voltage gain of the common emitter and common source amplifier particularly if it is having passive load. And intuitively we are understanding that, how it can be enhanced. Namely in case if we can get some characteristic load line characteristic like this, instead of having a linear characteristic. In fact, that is the center point of getting higher gain of any amplifier using active load.

I must also say in this context that in case if you are putting some arbitrary active load thinking that that may be improving the gain, but then it may not. Say for example, in case if you are increasing the slope here, instead of decreasing the slope then it may be rather the gain it may be lower. So, for example, in case the iv characteristic it is non-linear, but in case if it is having say this kind of load line characteristic where the slope of this load line it got increased. So, naturally it is expected that since the slope of this reflected it got increased compared to the passive load. Then the gain instead of increasing with this pink color load line, it will decrease ok; anyway.

So, let us see what kind of implementation we can think of to get this kind of non-linear load line, particularly this one which is giving us the gain. So, in the next slide we do have common source amplifier with active load.

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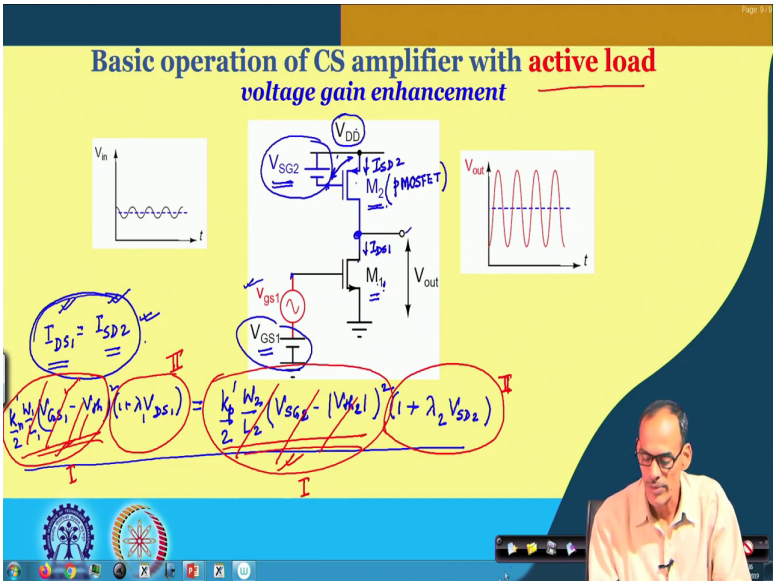

So, here the lower part we are retaining same and same circuit we do have the M 1, which is receiving the signal at its gate along with the DC voltage. But then it is also having the load, which is instead of having passive load, but it is having a transistor M 2. Note that this transistor m 2, this is PMOS transistor right.

And its source it is connected to VDD and the gate it is receiving DC voltage defined by say VSG with respect to VDD. Theoretically you may say that this gate voltage may be with respect to ground also, but we prefer to denote the biasing of this transistor M 2. In this way because the VSG of this transistor it is defining its current. Now of course, this transistor 2 based on its DC voltage it may define its own ISD current ISD 2; likewise transistor one based on its VGS 1 it may define its IDS current.

Now naturally, then who defines this current? For proper operation, we require both the current should be equal and we need to satisfy some condition to ensure that IDS 1 and IDS; ISD rather ISD 2 they should be equal.

Well, at this node we do not have any other circuit connected. So, it is very natural to say that why do we require any condition for this two current to be equal; because it is kcl as we do not have any other circuit connected here. Then the answer is that we assume that both the devices are in saturation region and in saturation region their current should be equal. If you are not paying good attention and if you are simply saying that I do not have any other circuit connected and the current of the two devices they must be equal. Then what it may happen that that ah one of these two devices will be forced into entering into a triode region, the other one may be remaining in saturation region and it will be having a huge consequence on the gain.

So, I must make you aware that we have to pay additional attention. So, that the both the devices are in saturation region and of course, their current should be equal. So, whenever we say that these two are equal what we mean is that, the devices are in saturation region and in saturation region whatever the current we do have they are equal.

In other words the VGS 1 VGS 1 minus V th square into its corresponding k called kn dashed W by L of transistor. 1 by 2 into 1 plus lambda VDS should be equal to kp dash W by L of the second transistor and its corresponding VSG minus its V th. So, this is PMOS transistor. So, threshold voltage may be negative.

So, that is why I am putting mod here then 1 plus its corresponding lambda multiplied by VSD. Now, this condition need to be satisfied to ensure both the devices are in good condition. Now you may say that this part, we may ignore or you can approximate these two parts they are equal into one, but then rest of the things this part and this part should be equal. So, for the time being to appreciate the basic operation of this common source amplifier with active load; let me assume that this this part. And this part they are equal these two parts referred as first order part and these two parts on the other hand particularly this part 1 plus lambda VDS.

And this one plus lambda VSD they are referred as the second order part; because they are influenced on the current as long as the devices are in saturation region is very small. And these two term on the other hand they do have strong influence on defining the corresponding current. So, we assume that this part and this part they are equal that is ensured now assuming that these two are equal let us see its operation.

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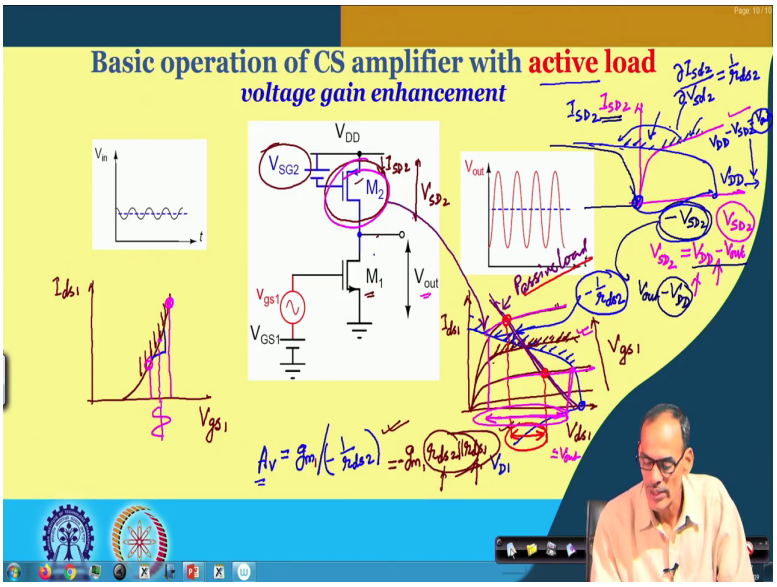

So, again to come back to the basic operation of the device particularly for M 1, we do have I ds versus V gs characteristic curve and this is beyond threshold this is square law. And then at I at the output node, if you consider both the pull down element namely I ds versus V ds characteristic curve and it may be triode region and then saturation region like this depending on different value of the V gs and so and so on.

Now this is where we are increasing the V gs 1. Now on the other hand if I consider the iv characteristic of this transistor that is very tricky. So, to get the corresponding load line first of all let me draw the and the current flow here namely ISD 2 as function of VSD; for a given value of the VSG 2.

So, as you may recall from our device characteristic, if we plot the ISD ISD 2 versus VSD 2 and its characteristic it is like this similar to NMOS transistor. So, now this ISD 2 it is not

same as V out though VDS 1 equals to V out, but this is not V out. However, this is related to V out which is equal to VSD 2 equals to VDD minus V out right. So, the VSD 2 equals to this. Now to match this x axis or this characteristic curve we need to eliminate this minus sign and also we need to eliminate the VDD. And to get that to do that last time as we have done, we need to flip this characteristic curve in the second quadrant.

So, which means that if I plot the IDS ISD 2 versus minus VSD 2; then I will be getting this characteristic curve and the moment I put say if I consider minus VSD, then this part it becomes V out minus VDD. Now to get rid of this minus VDD part, what you can do here it is, we can simply shift this characteristic curve by an amount of VDD. So, this point we shifted to VDD point which means that, now this new x axis is this part plus VDD and that is equal to.

So, this new x axis it is VDD minus VSD 2 and that is incidentally equal to V out and that is matching. So, this blue characteristic curve if I consider then I do have ISD 2 versus V out so, that is what you are getting. So, this blue line characteristic curve, now we can superimpose here. So, we may consider this blue line characteristic curve and how is it defined? First of all this point it is VDD. And then whatever the slope it was having original slope it is having this slope got changed, but the magnitude wise this slope remains the same.

So, this blue line it is working as load line for this common source amplifier having active load. Now if I compare the slope of this line and then if I compare the slope of this line. So, that gives us the gain of the circuit. So, intuitively you may say that the voltage gain A v equals to slope of this line it is gm, divided by slope of this line. And what is the slope of this line? Minus whatever it is. So, if you consider slope of this line, it is slope of this line it is change in IDS or ISD with respect to V VSD. In fact, this is nothing, but one by rds of transistor 2.

So, since the slope here it got change here so; that means, the slope of this line it is remaining same magnitude wise and hence slope of this blue line ; it is minus 1 by rds or r whatever you say essentially both are same. So, slope of this line it is minus 1 by rds. So, the voltage gain here it is gm divided by 1 by rds 2. In fact, there is a catch that so, so far we used to ignore the slope of the slope of this iv characteristic namely for NMOS iv characteristic. That is because

whenever you are having passive load here compared to the slope of the load line we use to ignore that.

Now; however, now we do have load line slope and the pull down characteristic slope they are comparable. So, we should also consider the slope of this line. In fact, if I consider if I rather ignore this slope or if I say that the device; the pull down device iv characteristic it is having almost 0 slope then this is the correct expression of the voltage gain. But then if I consider finite slope here then, I need to consider this slope also and it can be shown that ah. So, that part it is coming here as gm.

So, if I ignore the slope of the NMOS characteristic, then the expression of the gain it is gm 1 multiplied by rds 2 on the with a minus sign. On the other hand if I consider slope of this line, then instead of considering rds 2 I should also consider rds 1 and that is coming in parallel. In fact, whenever we will be talking about small signal equivalent circuit, this will be very clear. So, as long as if I say that both the slopes are comparable, I have to consider both the rds together.

So, in summary what do you obtain here it is that, because the load line slope, it got changed compared to the earlier slope; earlier slope means the passive load line slope. For the same operating point if I consider this is the sorry this is the load line for passive load. And this is the load line for this active load coming from the MOS. So, naturally the if I am having given variation of the input signal say with respect to quiescent point, we do have a variation here and here.

And let you consider this variation and this variation are essentially representing this characteristic curve and this characteristic curve with respect to the quiescent point. Then with active load what we have here it is, the output it is changing from here to here. So, so it is a big change versus if I consider on the other hand it is passive load for the same variation the intersection point of the device characteristic and the passive load line it is one is here, another is here.

So, if I compare the corresponding output here it will be only this one. So, with passive load we do have only this much of output; on the other hand if it is active load if it is active load here, then the output it is much higher. So, intuitively at least it is very clear that how it is helping to enhance the output signal amplitude for the same variation of the input signal here. So, this is intuitively and we can also analyze this circuit using its small signal equivalent circuit.

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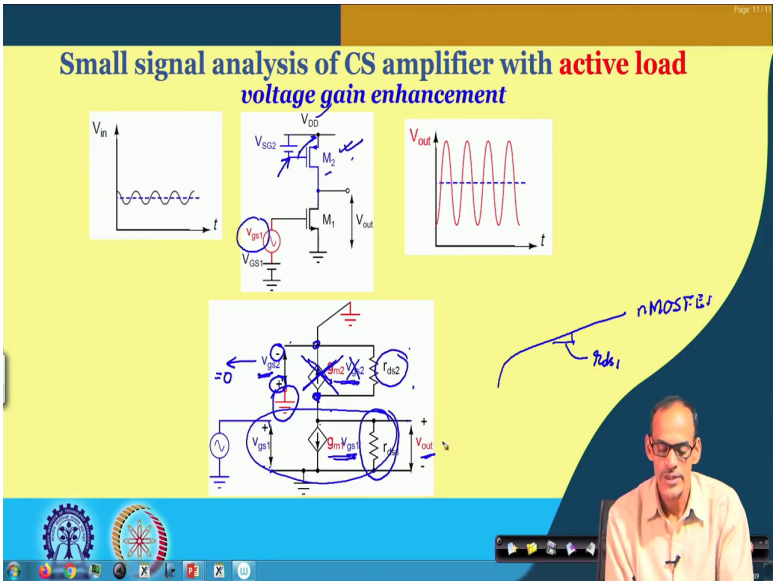

So, in the next slide we do have the we have drawn the small signal equivalent circuit for the common source amplifier having active load. So, here let us see, what are the what is the information we do have. First of all transistor one transistor one its model it is given here by the voltage dependent current source of gm 1 multiplied by V gs 1.

In fact, this V gs 1 it is defining the small signal current here, which is gm 1 into V gs one in addition to that to take care of the finite slope of the MOS. In the n MOS transistor to take care of this finite slope, which is rds; rds 1 we need to consider this also. Likewise if I consider say PMOS transistor M 2 it is having voltage dependent current source and its current is flowing from drain to source. And then the current is gm 2 of this transistor multiplied by V gs and V gs is this voltage where we are calling this is V gs.

So, the gate voltage it is positive and then source is negative. But since we do not have any signal here, this is also DC voltage. So, we can see that this is AC ground and this is also anyway this is DC voltage so, that is also AC ground. So, we can say for this circuit we do not have any signal. So, in small signal we consider this is equal to 0. Since this is 0 so, we can say this part is 0. So, we do not have this element. So, that makes the pull up element or the load part simply getting replaced represented by this corresponding rds 2.

So, if I analyze this circuit ignoring this current and then, whatever the voltage will be getting here due to this signal that is the final signal voltage. So, let me do the simple analysis.

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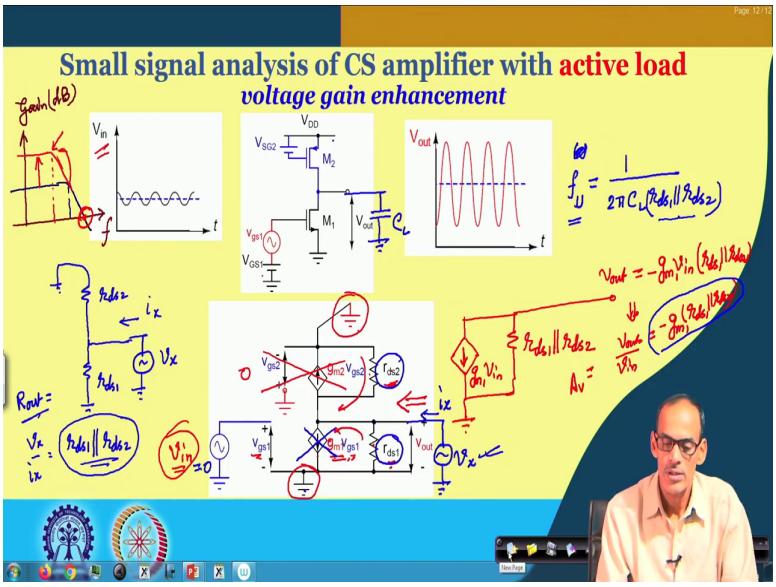

So, first of all if I call this is v in; so, we call this is say v in and we are applying this V in with respect to a DC voltage and in AC signal of course, the DC part it is it is not shown here; incidentally this V in equals to V gs 1. So, the current flow here it is gm 1 into V gs 1 and as I said that this part it is 0.

So, we do have only this rds. So, this current gm 1 into V gs 1 it is flowing through rds 1 as well as rds 2. In fact, the other end of rds 2 it is connected to AC ground rds 1, it is connected to ground. So, I should say that this current while it is propagating through both the registers I can simply combine these two registers. And then you may say that the simple circuit it becomes like the 2 rds, they are coming in parallel rds 1 and rds 2. And the current flow here it is gm 1 into V gs 1 which is incidentally equal to v in.

So, this side it is ground and whatever the voltage you do have here it is the output voltage. And that is equal to since the current is flowing in this direction that is equal to gm minus gm 1 into v in multiplied by rds 1 in parallel with rds 2. And that gives us the voltage gain v out by v in equals to minus gm 1 into rds 1 in parallel with rds 2 right. So, that is what the small signal analysis it is giving us ah. In addition to the gain, we can also see, what is the corresponding output resistance. And to get the output resistance what you have to do in the small signal equivalent circuit, we need to stimulate this circuit by signal source at this point.

And let you call this is vx and let you observe the corresponding current and while we are doing this exercise, we have to make this is equal to 0. So, if I make this is 0, this is also 0. So, this is also getting removed. So, what we have here it is only rds 1 and rds 2 connected to their corresponding ground. So, naturally if I simplify this circuit with this stimulus, what we have here it is the stimulus called vx. And then we are observing the corresponding current here ix. And inside the circuit we do have rds 2 and rds 1 connected to their respective ground.

So, it is very trivial now the circuit becomes very trivial. So, we can say that vx by ix is nothing but the resistance rds 1 coming in parallel with rds 2 and that is what the output resistance of this circuit. So, along with the voltage got increased the corresponding resistance also got increased. You may recall if it is a passive load say rd then the output resistance predominantly it was defined by the passive load rd. Now this resistance in this active load since it got increased.

So, the upper cutoff frequency if it is defined by output resistance and the load capacitance C L, then of course, the corresponding upper cutoff frequency omega or let me write in terms of Hertz in the unit of Hertz. So, upper cutoff frequency f u it is defined by 1 by 2 pi; then the corresponding load capacitance and then the resistance which is rds 1 coming in parallel with rds 2.

So, with passive load of course, this resistance it was lower and then the bandwidth it was higher. Whereas, for this case the in the resistance got increased as a result the corresponding

upper cutoff frequency got decreased. So, if I compare common source amplifier having passive load and active load and then if we see their gain and bandwidth particularly, what kind of comparison will you get for passive load? Let me use this space to compare. So, this is the frequency axis and this is the gain in d B.

So, for passive load suppose we do have a gain here and then the corresponding 3 d B bandwidth for a given c L. And then in active load circuit we do have gain got increase because the output resistance got increased, but then bandwidth got decreased. And both of the changes are both of the changes are getting created by the same entity called R out. So, as a result this bandwidth here it got decreased by the same factor as the gain got increased.

And their gain bandwidth product if I say here it is single pole role, then gain bandwidth product it is remaining same. Similar kind of things you can get for common emitter amplifier also and let us see the corresponding yeah.

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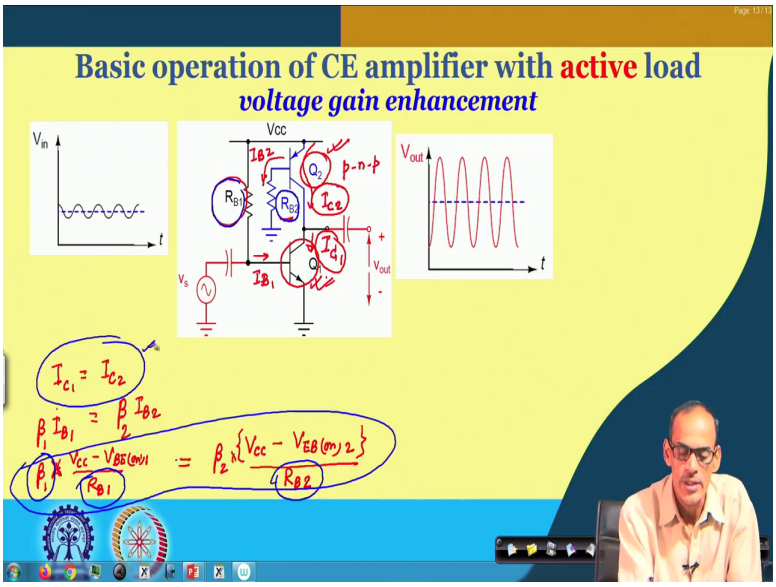

So, here we do have the corresponding circuit; namely common emitter amplifier having active load. So, we do have transistor 1 the main amplifying device here we do have relatively more practical circuit. The device 1 it is getting biased by its cone own resistance RB 1.

So, it defines the IB and then it defines the corresponding DC current IC and likewise transistor 2. So, this is p-n-p transistor and its current particularly the base current it is flowing in this direction through RB 2. And this IB 2 it is also defining the collector current IC 2. Now in this case similar to common source amplifier, we have to pay attention additional attention. So, that these two currents should be equal of course, again there is no other DC path we do have. So, natural question is that anyway both the current should be equal from kcl, but then we also like to keep both the devices in active region of operation.

So, in active region of operation these two currents IC 1 and IC 2 must be equal. And IC 1 it is defined by its corresponding beta multiplied by its IB. On the other hand the second transistor its collector current is beta its own beta and then IB 2. And then the base current here it is coming from its bias circuit namely these RB 1. So, we can say that V IB 1 equals to VCC minus VBE on of transistor 1 divided by RB 1. So, this is what the IB part. So, that should be equal to beta 2 multiplied by VCC minus VEB on of transistor 2 divided by RB 2.

So, if you see here in case beta the 2 transistors betas are different, then you may appropriately adjust the corresponding bias element. So, that eventually both the devices currents should be remaining equal if they are even if they are in active region of operation. So, we need to have appropriate fine tuning of these two resistances to ensure this condition. Now here for basic operation of this circuit let we assume that this has been achieved by some means and then we proceed for the subsequent analysis. So, that is the assumption that proper care has been taken care and that ensures these two currents are equal. And then the signal point of view.

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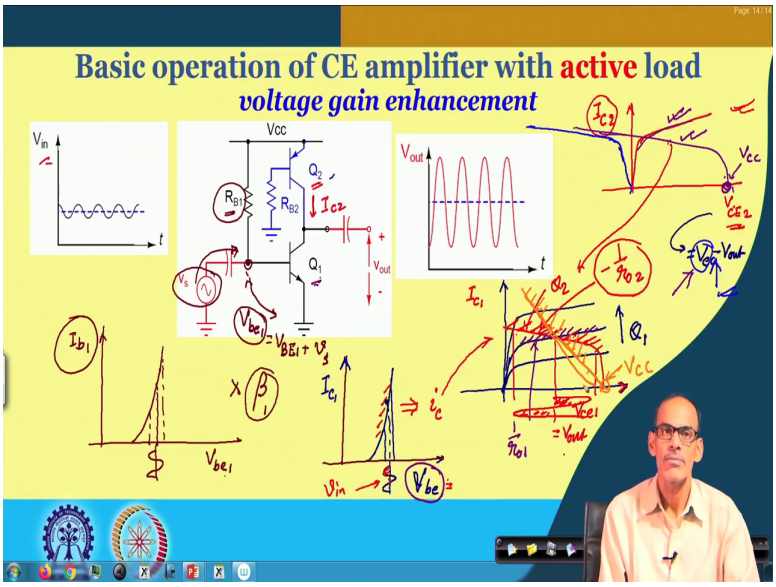

Now, at the base of transistor 1 we do have the I b versus I b 1 versus V be 1 and this V be 1 it is at this point. Of course, it is having a DC voltage without considering the signal part, but the moment we apply the signal here the voltage here it will be the voltage here it will be the corresponding DC voltage in addition to that, whatever the signal we do have.

So, we may say that capital V small be 1 it includes both the DC part plus this signal part and this signal part we are assuming it is directly coming there. So, the operating point it will be decided by this RB 1, but then with respect to that we do have the small signal also. And then if I multiply with beta, if I consider this current and if I multiply with the current gain of this transistor 1 so, that gives us so, that gives us I c let me use different color.

So, that gives us I c 1 with respect to V be 1 and again here we do have the exponential relationship. And so, this is the operating point with respect to that would it may be having

variation because of the signal we are applying there. And then at the output at the output port what we have here it is similar to the common source amplifier. Q 1 it is having the characteristic which it is known, initially it is in saturation then after that it enters into active region and so and so.

So, these are the characteristic curve for the pulldown element namely for Q 1. On the other hand if I considered Q 2 it is similar to the PMOS transistor, but we can say that its id or ISD rather ISD versus VDS curve we have seen for this case we can see IC 2 versus. So, IC now it is flowing in this direction IC 2 versus VCE characteristic. So, this characteristic it is similar to n-p-n since we are considering VCE 2. So, it is and also the direction of this current it is from emitter to collector. So, this is also positive and hence it is coming in the first quadrant.

Now, if you see this x axis this is V ce of transistor 1, which is V out and of course, the y axis it is I c 1. Now this I c 1 and I c 2 whether it is DC or small signal wise they should be equal. And to superimpose this load line characteristic here the corresponding x axis should also be equal. Now again similar to MOS transistors circuit this is not equal to this axis. However, this is equal to V cc minus V out.

Now again to get rid of this minus sign here and then this V cc part here what you have to do we have to do the 2 operation. Namely we have to flip the characteristic curve to get rid of this minus sign here. And then we have to shift the characteristic curve by a VDD amount to get rid off this part. So, as a result the original red color characteristic curve we are transforming into this violet color where this point it is V cc and this entire characteristic curve which is it is getting flipped here. So, now, we can superimpose this transform characteristic curve and that characteristic curve it is coming like this.

So, this is the characteristic curve obtained from the p-n-p transistor Q 2 and these are the characteristic curve of Q 1. So, again here since we do have the slope of this active load it is quite small. So, we are expecting the gain it will be quite high. In fact, this slope if you see it is minus 1 by r o of transistor 2. As you have discussed for P MOSFET similar to that for this p-n-p transistor the slope here it is minus 1 by ro 2. On the other hand slope of the this

characteristic curve, as I said that since these two slopes are comparable we need to consider both the slopes and this slope it is 1 by r o 1.

So, the overall gain starting from V be if I call this is the input, if I say that the input we are applying here. So, if I call this is it is having the DC plus the input part here. So, v in this v in it is getting reflected by this mirror. In the form of small I c this small I c, it is coming here and then it is getting reflected by load line. So, it is getting reflected here and in this form. So, now, again in comparison with the passive load; if I consider the load line passive load line, it is going through this operating sorry it is going through the operating point and the VDD point here or in this case rather VCC point.

So, the slope of this passive load line since it is small. So, expect and earlier the gain it was lower now that got gain got increased. So, again for this circuit, we can do the small signal analysis. And then we can find that how the gain as well as the bandwidth it is getting changed similar to common source amplifier.

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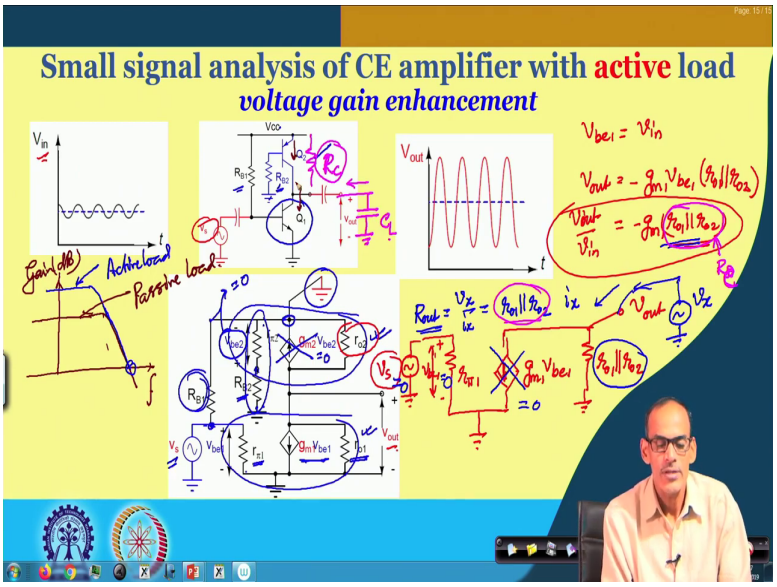

So, here we do have the small signal equivalent circuit to do the analysis here, similar to the previous case. The small signal model of Q 1 it is given here consist of gm into V be 1 and then ro 1.

And then r pi in addition to that we do have this bias element; similarly for Q 2; we do have the small signal equivalent circuit given there. And then it is having the bias circuit it is connected to ground here. Now the emitter node it is connected to VCC. So, that is AC ground and the this end also the other end of RB 2 it is also connected to ground. So, as a result there is no signal in this path, which means that this V be 2 it is equal to 0; that implies that this current is also 0.

So, that converts this small signal equivalent circuit, it is much simpler where we do have only this ro 2 we do have ro 1 and then gm into V be r pi and since the signal we are directly given

here. So, even though this is connected to ground this RB 2, it is not having any role to play. So, the small signal equivalent circuit what we have it is gm gm 1 into V be 1. And then we do have the r pi here r pi 1 and the signal we are feeding here, it is vs and the resistance ro 1; connected to ground and eventually this ro 2. It is also coming in parallel with that.

So, I should say this resistance it is ro 1 and ro 2 coming in parallel and this is connected to ground v be 1 it is defined here this is plus and this is minus. And then whatever the voltage it is developing here it is the output voltage v out. So, here again if you see eventually this vbe it is same as the signal here which we may call it is input signal we are applying here. So, V be 1 equals to v in and v out equals to since the current is flowing in this direction it is minus gm 1 into vbe 1 multiplied by the resistance, which is ro 1 coming in parallel with ro 2.

So, this is minus gm 1 into ro 1 in parallel with ro 2 multiplied by v in. Or you may say that if I consider v out divided by v in is equal to gm into ro 1 into ro 2. So, the gain again it is getting increased because of the slope of the two devices active device characteristic it is very small rather resistance is high. And also the resistance output resistance, if you see at this point. So, to get the output resistance the method it is same we can stimulate this circuit with say signal source of vx and then if you observe the corresponding current ix keeping this signal equal to 0. So, if this is 0, this is also 0. So, that makes this portion it is equal to 0 and that gives the output resistance equals to ro 1 in parallel with ro 2.

So; that means, the vx by ix which is defining the output resistance. So, that is equal to ro 1 in parallel with ro 2. So, in summary that we have the output resistance it is getting increased. And the gain it is also getting increased by the same factor in comparison with earlier what we have here it is here we are having RD. In case, we are having or RC rather RC in case if we have say, passive element RC and same thing here also and as a consequence that if.

If you consider the load capacitance equals to C L then the bandwidth in the previous case it was bandwidth it was defined by this resistance and C L and in this case in the output resistance it is now ro 1 in parallel with ro 2. So, similar to CE amplifier here also with passive load gain if we plot say gain in d B with respect to frequency in log scale. Then suppose for passive load gives a gain and then corresponding bandwidth here. On the other hand with

active load the gain got increased, but then bandwidth got decreased by the same factor. And as a result the gain bandwidth product it is remaining same.

So, this is with active load and the other one it is the with the passive load ok. So, so far we are talking about the circuit with maybe a little bit idealistic situation and then also we say that the two currents and this current and this current quiescent current should be equal that can be tackled by some practical circuit. So, let me touch upon that practical circuit.

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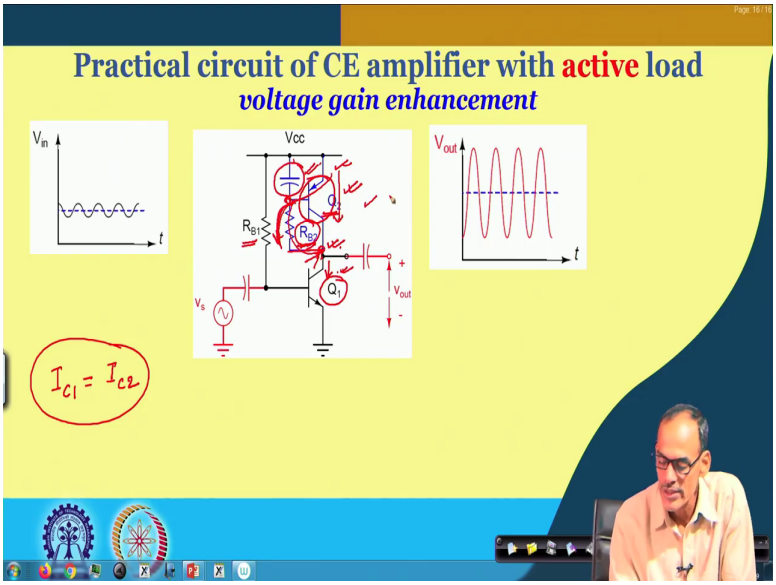

So, here is a small change now you can see here that the yeah. We do have let me use red color this RB 2 instead of connecting to ground we are intentionally connecting this to the collector and that gives that creates a feedback. In fact, later we will be discussing this part.

So, depending on the value of this resistance and the condition of or the DC voltage here, the current here the IB it will be defined. And whatever the resistance you are taking here that primarily defines this current. And this transistor it is very now it becomes it is accommodative to whatever the current it is defined by this Q 1; namely if the current here it is more than this voltage may become lower that makes this IB it is higher that makes its corresponding I c it is also higher.

So, this RB 2 as it is giving the information of the output voltage to its base we may say that it is working in feedback connection. However, you need to be careful that while this RB 2 connected to the output node it is providing a negative feedback to stabilize the operating point and it ensures that the operating point it is easily achieved. Namely it ensures this I c 1 into equals to I c 2 easily, but at the same time there is a chance that this RB 2; it may feed the signal back to this transistor and it may and that may reduce the gain of the circuit. To avoid that, we put some extra capacitor here.

So, that the V be voltage or V be voltage of transistor 2 signal wise it remains 0. At least in the mid frequency range this additional capacitor; it ensures that this this transistor it is really working only for giving the support not for any amplification or any feedback operation in the mid frequency range ok. So, if you consider it is a small signal equivalent circuit which is shown here in the next slide yeah.

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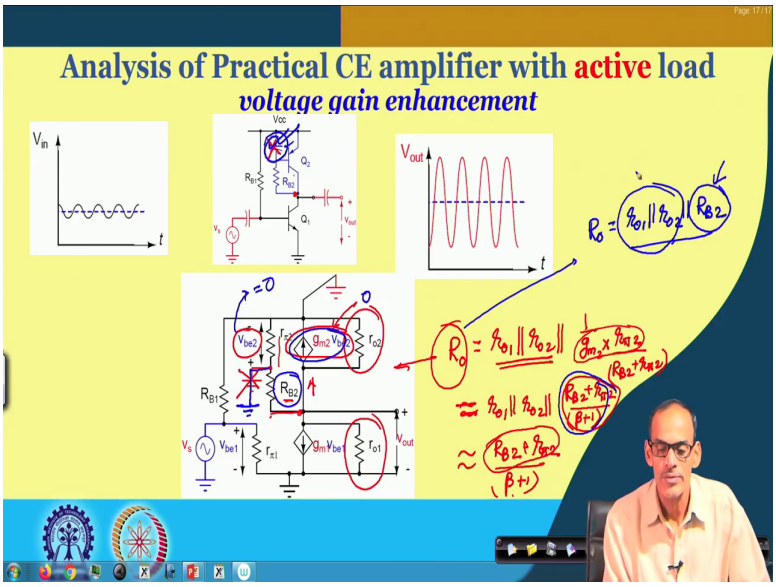

So, this is what the discussion here that if we connect this RB 2 here; that means, this RB 2 it is connected here it is not connected to ground. So, if we do not put this capacitor here then naturally then it will be providing one nonzero value of V be 2 as a result this current it will be flowing as a non 0 entity. And there is a consequence in fact, looking into this circuit this active device it will provide additional conductance.

So, the output resistance it is not only ro 1 and ro 2 coming in parallel. In fact, for this circuit if I do not consider this capacitor and hence if I do not consider this connected to AC ground, then R o you can find that this is coming in equals to small ro 1 ro 2 in parallel with 1 by gm 2 into r pi 2 divided by RB 2 plus r pi 2. In fact, you can simplify it further you can consider this is equal to beta. So, that is equal to ro 1 coming in parallel with ro 2 in parallel with RB 2 plus r pi 2 by beta. In fact, if I also need to consider this path.

So, it may be even the additional one also. And the this is equal and that becomes primarily dominated by this and it may be reducing the output resistance drastically. And the consequence is that if the output resistance it is drastically getting reduced from whatever our original target of ro 1 in parallel with ro 2 only that will drastically that may affect the gain. In fact, that will affect the gain drastically.

And that makes the even though the active circuit we may call it is active circuit gain of the circuit it may go back to the previous circuit. Numerically we will see that how if I consider practical value of this RB 2 and then beta then, we will see that gain it may not change much compared to common emitter amplifier with passive load. So, to overcome this problem what we are considering now it is, we are putting this circuit here. And the moment we put the circuit there it is basically we are making this is ground and that makes this V be equals to 0 and that makes this part equal to 0.

And that makes this circuit going back to the previous one except of course, this RB 2 it will be coming in parallel. So, instead of this part if I put the capacitor bypass capacitor here then the corresponding R o it will be ro 1 coming in parallel with ro 2 coming in parallel with RB 2. Well, even though in this case this RB 2 it is coming in parallel with ro 1 and ro 2, but we know that the typically value of this base register it is quite high. And all practical purposes it may remain unchanged almost unchanged and hence the gain of the circuit it will be very good.

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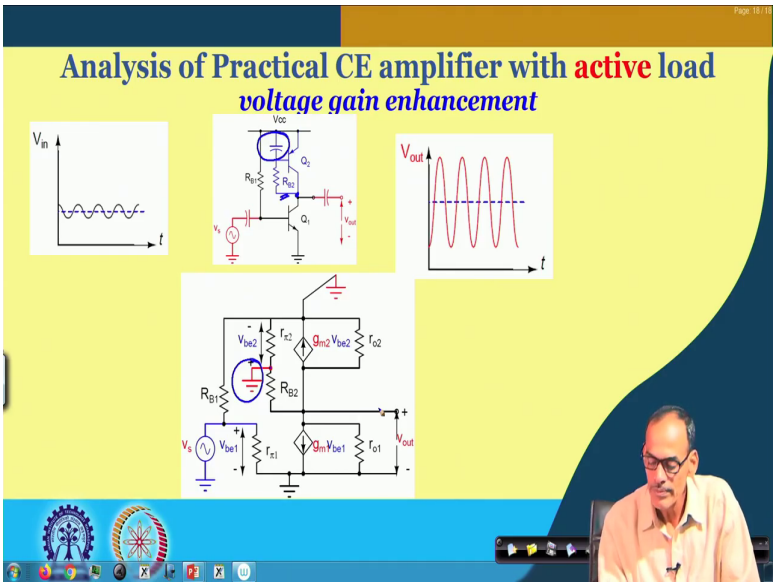

So, in summary of this modification what we like to say here it is. In this case by making the connection of this RB 2 to the output node, we are making the operating point easily achievable. And then to avoid the it is adverse effect on the gain namely the reduction of the gain we are putting this extra capacitor which is making the base node of transistor to ground and hence the corresponding gain it is remaining high. So, numerical value we will see it later.

So, similar kind of practical circuit can be obtained for common source amplifier also.

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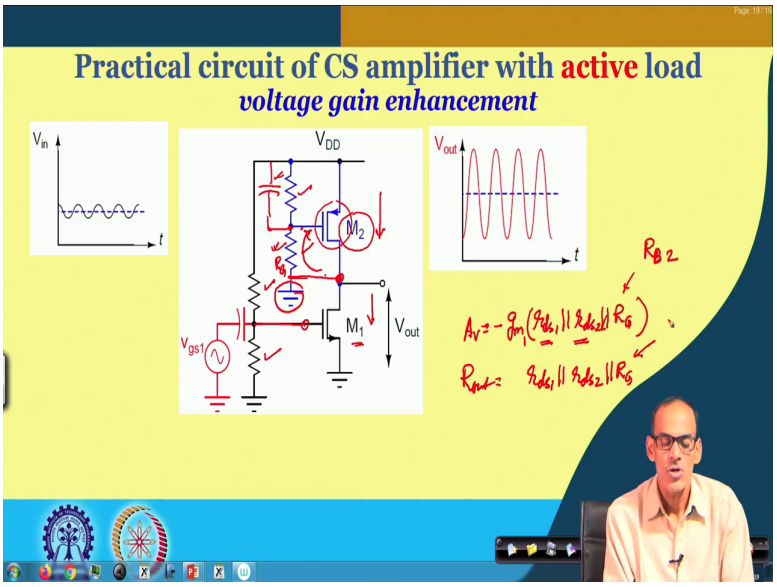

This is what it is shown here. I will not be going in detail, but just to say that the we do have say one register here. We do have another register here to define the gate voltage of transistor 1 and likewise we do have two more registers here to define the gate voltage of transistor 2. And then we have to ensure that these two IDS and ISD they should be equal and both of the transistors should be in saturation region.

Now, to avoid the fine tuning and all or rather to get this condition easily achievable instead of connecting this to ground we can connect this to output node. But then again we must be aware that, the moment we connect this register to the output node it may feed the signal back here and that may reduce the gain of the circuit because that reduces the output resistance. To take care of that you can put here AC grounding capacitor making the signal coming back here it is bypassed and making the active part of this device equals to 0.

And then we can get the high gain and for this case if you put this register and if I call this is a RG just RG; then the voltage gain for this case it will be gm 1 multiplied by rds 1 in parallel with rds 2 in parallel with RG with a minus sign. And the output resistance it is rds 1 in parallel with rds 2 in parallel with RG. In fact, if you if you see the previous circuit also, now if it is BJT there we have seen similar kind of things namely this was ro 1 this was ro 2 and this was RB 2 and same thing for this also instead of RG it will be RB 2.

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So, we need to cover the practical circuits. So, that will be covered in the next class. So, in conclusion what we have covered today it is, we started with basic motivation of going into active load. Namely in improving the performance specifically the voltage gain of common emitter and common source amplifier and then we have discussed about the basic operation of

common source and common emitter amplifier having active load. And then we have done the analysis to get the expression of voltage gain.

And then output resistance for considering the idealistic bias condition. And then we have discussed about practical amplifier circuit where the operating point is possible and achievable with active load. And then we have seen the consequences or at least we have highlighted the consequences. Namely the gain may get affected by those practical circuits having feedback. And then we considered bypass capacitor there to avoid the adverse effect on the gain. And the other two things we yet to cover it as on this topic is that numerical examples may be little bit on the guidelines, but that will be covered in the next class.

Thank you for listening.