

**Analog Electronic Circuits**  
**Prof. Pradip Mandal**  
**Department of Electronics and Electrical Communication Engineering**  
**Indian Institute of Technology, Kharagpur**

**Lecture – 66**  
**Multi-Transistor Amplifiers:**  
**Amplifier with Active Load (Part A)**

(Refer Slide Time: 00:26)



The image shows a presentation slide for NPTEL Online Certification Courses. The slide has a yellow background with a blue geometric shape on the left side. At the top, there are two logos: the IIT Kharagpur logo on the left and the NPTEL logo on the right. Below the logos, the text reads "NPTEL ONLINE CERTIFICATION COURSES" in orange. Underneath, it says "Course Name: Analog Electronic Circuits" and "Faculty Name: Dr. Pradip Mandal". The department is listed as "Department : *Electronics and Electrical Communication Engineering*". The topic is highlighted in red: "Topic: Amplifiers with active load". The slide is displayed on a computer screen, with a Windows taskbar visible at the bottom.

Dear students welcome back to NPTEL online certificate certification course on Analog Electronic Circuit. Myself Pradip Mandal from E and EC department of IIT Kharagpur. So, to continue this course today's topic of discussion it is Amplifier with Active Loads. We may be having multiple amplifiers but, primarily we will be talking about common emitter and common source amplifier today.

(Refer Slide Time: 00:59)

Page 41

## Flow of Discussion (Bottom-up) – Building blocks

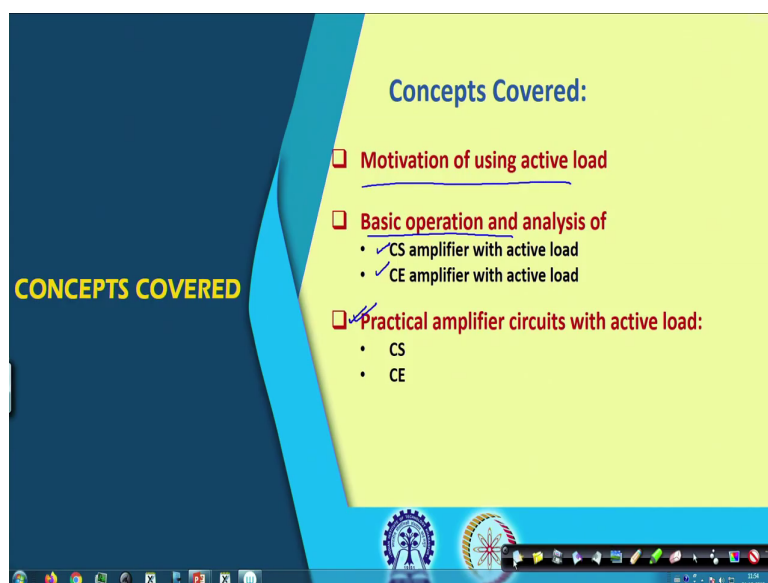
- **System/ Sub-systems** (for specific application)
  - **Modules** (performing specific tasks)
    - **Building blocks** (having specific characteristics)
      - Components (devices/circuit elements)
- **Week 6:**
  - ✓ Multi transistor Amplifiers (operation and analysis):
    - CE-CC; CS-CD; CC-CC; Darlington pair etc.
  - ✓ Cascode amplifiers
    - CS-CB and CS-CG
  - **Amplifier with active load.**

The slide features a yellow background with a blue wave-like graphic on the right side. A small video inset in the bottom right corner shows a man with glasses and a light-colored shirt speaking. The bottom of the slide has a blue bar with several logos, including the Indian Institute of Technology (IIT) logo.

Compared to our overall weekly plan we are in week 6, I should say module 6 and we are. In fact, we already have completed these two sub topics namely Multi Transistor Amplifiers and then Cascode amplifiers. And today we are going to talk about Amplifier with active load. In fact, incidentally when we talk about active load, the amplifier it is having multiple transistors.

So, you may say that this is also a special kind of multi transistor amplifiers. But we like to explicitly say that it is having unique characteristic, where the passive load it is getting replaced by a load utilizing MOS transistor or BJT transistor. So, that is why though it is multi transistor amplifiers, but basically characteristic wise the load part it is getting replaced by another transistor.

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Now, today what we are planning to cover it is under this active load amplifiers, we do have to start with we do have motivation of using this active load. Then, from that we will we will be talking about basic operation of amplifier having active load and their corresponding circuit analysis including, small signal model and then finding the gain or maybe intuitively explaining the gain and so and so.

And then we will be talking about practical circuits having the active load and for both the basic operation as well as for practical amplifiers. So, we do have two main amplifiers in our discussion, one is common emitter and common source amplifier. Numerical examples and design guidelines it will be covered in the next class. So, to start with let we go for the motivation of going for active load.

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**Recall: Basic operation of CE amplifier with passive load**  
*Limitation on voltage gain*

The slide illustrates the basic operation of a common-emitter (CE) amplifier with a passive load. It features two circuit diagrams and two graphs. The top diagram shows a CE amplifier with a collector resistor  $R_c$ , a base-emitter junction, and an input signal  $V_{in}$ . The output is  $V_{out}$ . The bottom diagram shows a similar circuit with a base-emitter junction, a collector resistor  $R_c$ , and an input signal  $V_s$ . The output is  $V_{out}$ . The graphs show the input and output signals over time.

This is a recapitulation or recalling whatever we know about CE amplifier and not only we will be talking about CE amplifier. But basic operation of the CE amplifier just to see that, what is its limitation of the voltage gain.

In fact, if you recall that this is the this is the main amplifying transistor and it is at the at the input we do have the signal we are feeding along with the along with the DC component. So, that the transistor it is in active region of operation. In addition to that we also have the RC connected to the collector to the supply voltage  $V_{cc}$  and the connection of this RC it is such that the transistor here it is in active region of operation.

So, this RC it is having dual role to play, first of all it provides appropriate region of operation. And the second one it is it also converts the current into voltage, because primarily at the output we observe the signal in the form of voltage  $V_{out}$ . So, by applying a voltage at

the input port namely at the base it is given here which is having a DC voltage along with the signal. We are changing the collector current with respect to it is question current and that variation or change or the signal part it is getting converted from voltage to sorry from current to voltage by this resistor  $R_C$ .

So, this resistor typically it is referred as load and it is if it is passive component which is providing linear IV characteristic. Of course it works fine, but to some extent it is having limitation to give the voltage gain. I should say rather it is having good gain the CE amplifier basic CE amplifier it is having good gain. But in case if you want to enhance the gain further, then there is a scope of improving the gain and that may be done by replacing this passive element by it is active equivalent circuit. So, let us see that where the limitation it is coming from particularly for the voltage gain.

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**Recall: Basic operation of CE amplifier with passive load**  
**Limitation on voltage gain**

$A_v = \frac{V_{out}}{V_{in}} = \frac{V_{ce}}{V_{be}}$   
 $A_v = -g_m R_C = -\beta \frac{r_i}{R_C}$   
 $V_{out} = V_{ce} - V_{RC}$   
 $V_{ce} = V_{CC} - I_C R_C$   
 $V_{be} = V_{BE} + v_{be}$   
 $V_{out} = V_{ce} - V_{RC}$   
 $V_{be} = V_{BE} + v_{be}$   
 $V_{out} = V_{ce} - V_{RC}$   
 $V_{be} = V_{BE} + v_{be}$   
 $V_{out} = V_{ce} - V_{RC}$   
 $V_{be} = V_{BE} + v_{be}$   
 $V_{out} = V_{ce} - V_{RC}$

To come to the basic at the base, what we are doing is we are changing the voltage at the base or either you say base voltage or base to emitter voltage. And if you observe the based the current flowing through the base terminal say  $I_b$  instantaneous current having both DC as well as the small signal part as function of  $V_{be}$ , which is also having a DC part as well as a small signal part. As you know that it is having exponential dependency.

Now, this base current it is getting converted into collector current and that we may call capital  $I_c$  and this  $I_c$  it is flowing through this RC and it is creating a drop across this register called  $V_{RC}$  and then we do have the supply  $V_{cc}$ . So,  $V_{cc}$  minus  $V_{RC}$  that gives us the  $V_{out}$ . So, this is  $V_{cc}$  minus  $V_{RC}$  and then this  $V_{RC}$  as I said that it is having RC it is expression is RC in multiplied  $I_c$ .

So, pictorially if you see the output for characteristic, namely if we sketch the  $I_c$  versus  $V_{out}$ . So, you may recall for a given value of current at the base the corresponding collector current it is having IV characteristic like this. So, in the active region the current  $I_c$  it is almost independent of  $V_{out}$ . But then if you go very low then of course, the device enters into saturation region and then there is a significant or I should say sort dependency of the collector current on  $V_{out}$  or in this case incidentally that is  $V_{ce}$ .

Now, then if we consider the load line characteristic, as you have discussed load line characteristic it is given by essentially IV characteristic of this RC. And we have discussed that how we obtain this load line characteristic; namely if you plot the voltage the current through this resistance RC with respect to it is it is voltage across it is  $V_{RC}$ . Actually this load line characteristic is linear.

But then to match the x axis this  $V_{RC}$  instead of writing  $V_{RC}$  we prefer to write this as  $V_{cc}$  minus  $V_{out}$ . So, to match this x axis with this the  $V_{out}$  what we have what we have done or we in fact we have discussed that we do flip this x axis. So, that the characteristic it becomes in the second coordinate and then after that we shift it, so that then the load line then we get the load line. Where the shift it is  $V_{cc}$  amount.

So, this point it is  $V_{cc}$  and then slope of this original IV characteristic it was  $1/R_C$  and the slope of the transformed load line characteristic it is  $-1/R_C$ , so that is how we obtain this load line. So, the slope of this line it is  $-1/R_C$  and the amount of shift we have done here to get rid of this  $V_{cc}$  part to match the  $V_{out}$  axis with this  $V_{out}$  axis, we have shifted this point here.

So, that gives us this point of the load line characteristic it is  $V_{dd}$ . So, that gives the one age of the load line  $V_{cc}$  or  $V_{DD}$  in this case  $V_{cc}$  and the slope it is  $-1/R_C$  that gives the other end of the load line it is equal to  $V_{cc}$  divided by  $R_C$ . Now we know that once you have this load line and once we have the device characteristic intersection of these two characteristic gives us the final  $V_{out}$  and also of course it is giving the corresponding current call  $I_c$ .

So, this  $I_c$  and this  $V_{out}$  it is basically the solution point. Now whenever we are giving a signal as you may recall whenever we are giving the signal with respect to a DC operating point. So that means, we are changing the device characteristic up and down with respect to it is actual the exponential relationship, that makes the device characteristic namely the we call this is pull down element characteristic it goes down or up.

And as a result the since the operating point it is changing by wearing this voltage and incidentally that is also changing the changing the  $V_{out}$  namely the output voltage and that is how we are getting the output signal right. Now if you see that the gain starting from the input which is getting converted into current  $I_b$  and then through the multiplication of beta then we obtain  $I_c$ . So, this  $I_b$  it is getting converted into  $I_c$  by multiplying with beta and then again by this load line the signal part it is getting converted back into this voltage.

So, I should say that we do have a voltage here, voltage it is getting converted into current and then this current it is coming to this y axis and then this load line characteristic it is converting back this current into voltage. So, we can see that we do have two reflectors, one is  $I_b$  versus  $v_b$  characteristic reflector multiplied by beta and then we do have the other reflector.

In fact, if you combine this multiplication and then this exponential relationship, namely if we plot the  $I_c$  versus  $V_{be}$  characteristic curve. Then of course this is also exponential. But with it is having different scale because of the beta.

So, this  $I_c$  versus  $V_{be}$  characteristic curve it gives us one conversion from voltage to current, so that gives us the current. And then this characteristic curve it is converting back this current into voltage. So, naturally the gain of this conversion input to output gain it depends on the conversion rate here and then also it depends on the conversion rate at the other reflector.

So, if I intuitively if I say that if the slope of this reflector it is very stiff, on the other hand if the slope of this reflector it is say very small then we can get high gain. So, the mathematically you can see that gain when you say gain  $A_v$  equals to  $g_m$  into  $RC$  with a minus sign right. So, since the gain it is  $g_m$  into  $RC$  and the slope of this line it is nothing but  $g_m$  and slope of this line on the other hand it is minus 1 by  $RC$ .

So, I should say that the gain is essentially slope of this mirror multiplied by reciprocal of the slope of the other mirror. Why the reciprocal? That is because, this second mirror it is converting the y axis into the x axis. So, that is why we do have the slope it is getting flipped. So, I should say this is equal to  $g_m$  ratioed with one by  $RC$  with a minus sign.

So, now in case if we want to really increase the gain, of course it is having a limitation of the gain will be talking about that also. If you numerically see what is the value here, if you put the expression of  $g_m$  into this equation that gives us that is  $I_c$  question current  $I_c$  multiplied by  $RC$  divided by  $V_T$ . Because  $g_m$  into  $g_m$  equals to  $I_c$  divided by  $V_T$  and  $I_c$  multiplied by  $RC$  it is nothing but this voltage drop DC voltage drop.

So, and on the other hand the  $V_T$  it is thermal equivalent voltage. So, we can say that maximum limit of this gain it is the drop across this  $RC$  resistance divided by thermal equivalent voltage. And if we have the  $V_{cc}$  supply here, obviously this drop across this  $RC$  cannot exceed that. In fact, that should be practically that should be lower than  $V_{cc}$ , because we require some drop across this device. So, in extreme case even if I considered and say drop



across RC equals to close to  $V_{cc}$  then the gain of the amplifier it is  $V_{cc}$  divided by  $V_d$ . So, that is the theoretical limit of the amplifier gain.

So, that is what we see that limitation of the voltage gain, in this circuit because the  $g_m$  it is good in this circuit the gain value it is very decent. But in case if you want to further enhance then we may look for some alternative. Now what may be the alternative? Let us try to intuitively understand that what may be the scope of improvement of this gain.

So, we the slope of this line it is coming from  $1/RC$  and suppose this is the equation point with respect to this question point. If we want to increase the increase the gain naturally you may be thinking that suppose if I make the load line like this, which means that if I decrease the slope of the load line. Which means that, if I increase the value of this resistance  $RC$ , then from this analysis what we say it is that voltage gain it is  $g_m$  which is the slope of the first mirror and then divided by inverse of rather slope of the second mirror.

So, if I decrease the slope of the second mirror, since it is coming in the denominator so we may say that will be increasing the gain. So, this red colored mirror it is supposed to be increase in the gain. In fact, intuitively it is also clear that for the same kind of variation if you see for this curve and this curve of that device, the intersection point it is here and then the other intersection point it is here. So, it is expected that the corresponding signal it will be getting amplified like this.

But what is the what is the problem here, we are looking for a meeting point of the load line which is much higher than whatever the earlier meeting point and this meeting point it is nothing but the  $V_{cc}$ . Now if you are looking for higher value of  $V_{cc}$  which means that I am looking for higher supply voltage.

Well, theoretically it is that is what it is, but practically if the supply voltage is more there are two issues, one is power dissipation it will increase for the same coefficient current. If this voltage it is higher necessarily the power dissipation it will be a problem and also

instantaneously if the output voltage here it is higher, then that may exceed the breakdown limit of the device, so this may not be allowed.

Some extent it is possible to increase the gain, but then you cannot make this  $V_{cc}$  arbitrarily high to enhance the gain. So, the natural question or a natural intuition it may be or rather I should say smarter intuition maybe, that can I can I increase this rather decrease this slope without changing this voltage? Well, that is also possible maybe we can keep this point here and then we can try to decrease this and decrease this slope of the second mirror. But then the corresponding equation point it should be coming down here, which means that I may be looking for equation point somewhere here instead of this one.

Where the  $g_m$  it will drastically drop. So, if I try to decrease this slope without changing the supply voltage then I have to decrease the  $g_m$  and anyway the  $g_m$  it is also coming in the expression of the gain. So, naturally it is not helping well. Then what may be the solution ah? Suppose if I decrease this slope, but then if I do not do not allow this supply voltage to be increase. So, we can probably you can terminate this characteristic here.

Which means that, in case if we have an option to have IV characteristic which is not completely linear, but over this range it is linear and then it is having sharp non-linear to terminate to the and to the available supply voltage. And then what we are getting by this blue line blue load line, it is we are decreasing the slope of the second mirror and at the same time supply voltage we are not changing and also the equation point here we are not changing.

Which means that without changing the  $g_m$  here we are able to decrease the slope of the load line and at the same time since the supply voltage it is remaining same. Then we do not have any increase of the power dissipation we do not have any fear of whether the device it will be entering into the breakdown ok. So, that is that is what we replacing this passive load by active load ok.

So, anyway so what we said is that limitation of the voltage gain or the standard CE amplifier namely CE amplifier with passive load and it is gain it is primarily it is getting restricted by the voltage drop across this resistance divided by  $V_T$ . So, I should say  $A_{v\max}$  it is the voltage

drop across this RC divided by  $V_T$  and that can be extended by going for some alternative of this.

Similarly, if you look into the common source amplifier on the other hand it is philosophically it is same, only thing is that the IV characteristic instead of  $I_c$  versus  $V_b$ , now we have to  $I_{ds}$  versus  $V_{gs}$ .

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**Recall: Basic operation of CS amplifier with passive load**

**Limitation on voltage gain**

The slide illustrates the basic operation and limitations of a common source (CS) amplifier with a passive load. It includes the following components:

- Graphs:**
  - $V_{gs}$  vs  $t$ : Shows an input sine wave.
  - $I_{ds}$  vs  $V_{gs}$ : Shows the drain current characteristic curve.
  - $V_{out}$  vs  $t$ : Shows the output voltage sine wave.
  - $V_{gs}$  vs  $t$ : Shows another input sine wave.
  - $V_{out}$  vs  $t$ : Shows another output voltage sine wave.
- Circuit Diagrams:**
  - A MOSFET  $M_1$  with a load resistor  $R_L$  connected to  $V_{DD}$ . The output voltage  $V_{out}$  is taken from the drain. The equation  $V_{out} = V_{DD} - R_L I_{ds}$  is shown.
  - A MOSFET with a load resistor  $R_L$  and a source resistor  $R_S$ . The output voltage  $V_{out}$  is taken from the drain.
- Equations and Notes:**
  - Handwritten equation:  $A_v = \frac{g_m}{1/R_L} = g_m R_L = 2 \frac{I_{ds} R_L}{V_{gs} - V_{th}}$
  - Note:  $V_{out} = V_{DD} - R_L I_{ds}$
  - Note:  $V_{out} = V_{DD} - R_L I_{ds}$

So, as I said that for common source amplifier also we do have the similar kind of problem, to name with that namely the gain voltage gain it will be limited.

And in this case the voltage gain in fact it is much lower than common emitter amplifier. In fact, we have seen that for in the numerical examples we have seen that common emitter amplifier it is having a typical gain of say 100 or more. Whereas, for common source amplifier

for practical purposes we have seen that with passive load the gain it is even less than 10, so that definitely it is a serious matter.

So, whatever the modification we are going to discuss it is more significant for common source amplifier if not important for common emitted amplifier. So, first of all we do have  $I_{ds}$  versus  $V_{gs}$  characteristic curve and here again if you plot the sorry this is  $I_{ds}$  versus  $V_{gs}$  characteristic curve and in this case it is not exponential rather it is a square law right. But then philosophically again it is it is working as a reflector like a mirror, which converts the  $V_{gs}$  variation  $V_{gs}$  variation it converts into current.

So, it converts into current either you can see this way or this way, but basically it converts into the corresponding current variation. And then if you see the output voltage which is supply voltage  $V_{DD}$  minus this  $IR$  drop. So, which is  $I_{ds}$  multiplied by  $R_D$  and mathematically we can say that  $V_{out}$  it is  $V_{DD}$  minus  $R_D$  multiplied by  $I_{ds}$  and this  $I_{ds}$  it is given here.

And pictorially on the other hand you may see that this is we do have  $I_{ds}$  versus  $V_{ds}$  characteristic curve. And if I consider device it is initially in entire region it was like this and then after that it enters into saturation region at say some operating point. In case if the  $V_{gs}$  it is lower then the corresponding  $IV$  characteristic it comes down like this. On the other hand if it is higher, than the corresponding characteristic of the device namely pull down element it is like that.

And then we do have the load line we do have the load line as you may recall, which is similar to the CE amplifier and the point here intersection point here it is the supply voltage. In this case it is  $V_{DD}$  and slope of this line it is  $1$  by  $R_D$  with a minus sign. So, here again this is working as the load line it is working as reflected and this may be say question point and in this case the expression of the  $g$  voltage gain  $A_v$  which is  $g_m$ ,  $g_m$  is the slope of this mirror slope of this  $IV$  characteristic multiplied by or divided by slope of this characteristic.

So, that is divided by  $1$  by  $R_D$  with a minus sign or you can say this is minus  $g_m$  into  $R_D$  and this  $g_m$  if you recall it is expression this is  $I_{ds}$  divided by  $\mu_m$ . In fact, this will be 2 times  $I_{ds}$

divided by  $V_{GS} - V_{th}$ . So, it depends on how we express this  $g_m$ , but of course this is one expression. So, this multiplied by  $R_D$  with a minus sign. Again this part if you see it is nothing, but the drop across this  $R_D$  and it is its upper limit it is of course the supply voltage. In fact, practically it is lower and all practical purposes we like to take this  $I_{DS}$  versus  $R_D$  equals to half of  $V_{DD}$  rather than trying to stretch to  $V_{DD}$ .

And then depending on this  $V_{GS} - V_{th}$  which is commonly known as overdrive voltage of the transistor beyond the threshold voltage. So, typically this voltage overdrive voltage which is  $V_{GS} - V_{th}$  and that is a much higher than thermal equivalent voltage which it was there for  $V_{gt}$ . So, as a result in fact  $V_{GS} - V_{th}$  may be in the order of maybe 1 or 2 volts for discrete component. So, if I say that upper limit of  $I_{DS}$  versus  $R$  multiplied by  $R_D$  is  $V_{DD}$ . So, we can see that this is the upper limit  $V_{DD}$  and so this maybe that gives us the max of the voltage gain max of  $A_v$  equals to 2 times  $V_{DD}$ , divided by whatever  $V_{GS} - V_{th}$  right.

And since this part it is restricted by the supply voltage, then again it is having the limitation of the voltage gain. Numerically you have seen that if you take this is 12 volt then practically is to take  $I_{DS}$  multiplied by  $R_D$  it is 6 volt and then 6 multiplied by 2 it was that was 12. And the practical value of this  $V_{GS} - V_{th}$  we have taken say 1 or 2 and that used to give a gain of only 2. So, sorry used to give a gain of 12.

So, again the conclusion is that with passive load the voltage gain it is really limited and we are looking for it is corresponding alternative. And of course, this is the corresponding analysis if it is a passive circuit passive load, then the corresponding load it was it was playing a role to define the gain. So, I will not be going detail of this one, but we may come back to the small signal analysis when we will be talking about the active load amplifier.

Now, here again we like to replace this load or the load line characteristic, we like to get something like this. Where the slope of this IV characteristic it is a small, but then it should it should converge to this  $V_{DD}$  point  $V_{DD}$  point. So, we are looking for IV characteristic like this for this element. So, that the first of all the operating point remains unchanged the corresponding current it will be the same. So, the  $g_m$  here it will be the same. On the other

hand slope of this line it is getting decreased. So, if the slope of this line it is getting decreased then this part 1 by RD part it will be getting increased.

And hence there is a scope of increasing the gain and also without that can be obtained without changing the supply voltage. So, we will take a short break and then we will be coming back to discuss about the both the amplifiers with active load.