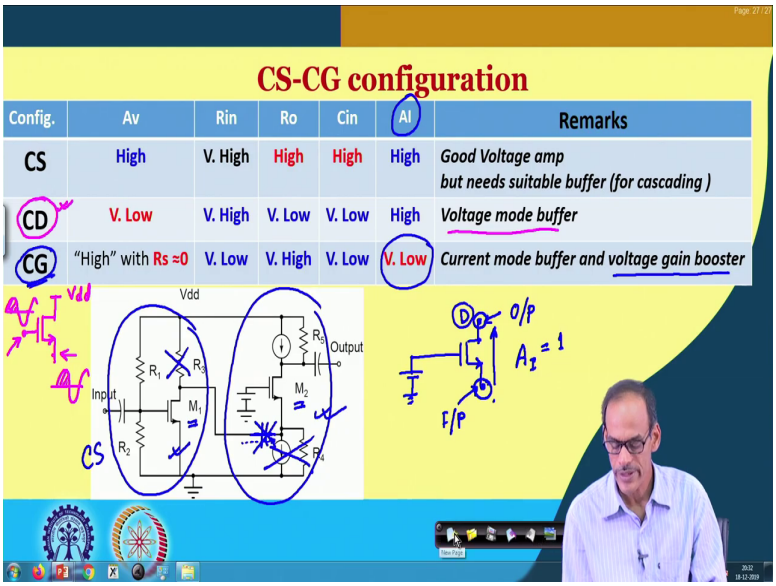
**Analog Electronic Circuits**
**Prof. Pradip Mandal**
**Department of Electronics and Electrical Communication Engineering**
**Indian Institute of Technology, Kharagpur**

**Lecture – 62**
**Multi-Transistor Amplifiers: Cascode Amplifier (Part B)**

Start sir.

(Refer Slide Time: 00:29)




So, welcome back after the short break. So, now let us move to the cascode configuration using MOSFET. But as I said, that the cascode configuration it is combination of common source followed by common gate. And, similar to BJT where we have discussed about CE followed by CG.

So, here also the basic purpose it is to have that configuration. We need to again summarize and want to know what is the purpose of this configuration. Particularly, cascading common source with common gate. Before I go into that, here also I like to say that when we talked about CE CC amplifier we said that that circuit it is referred as emitter follower.

So likewise, when you talk we refer to say common drain stage where input we give at the gate and then output we observed at the source. And drain node typically it is connected to supply voltage. And we have discussed about its basic purpose and the gain voltage gain from gate to source, it is approximately 1. And also the phase shift is 0 degree.

So, if I give a signal at the gate like this, at the source what you observe it is almost replica of that signal and hence the common drain circuit it is referred as the source follower. So, source is trying to follow the gate. So, likewise when you talk about the common gate circuit, and for common gate circuit what we do the signal we feed at the we feed at the source node.

So, this is the input port and the gate it is connected to a DC voltage which is AC ground. And then we observe the corresponding signal at the drain terminal. And typically instead of considering the signal in the form of voltage, here we prefer the signal to be treated in the form of current both at the input port as well as the output port.

And its current gain current gain it is approximately equal to 1. In fact, I should say it is 1. So, the current gain since it is 1, it is this circuit is referred the common gate circuit is referred as again current conveyor.

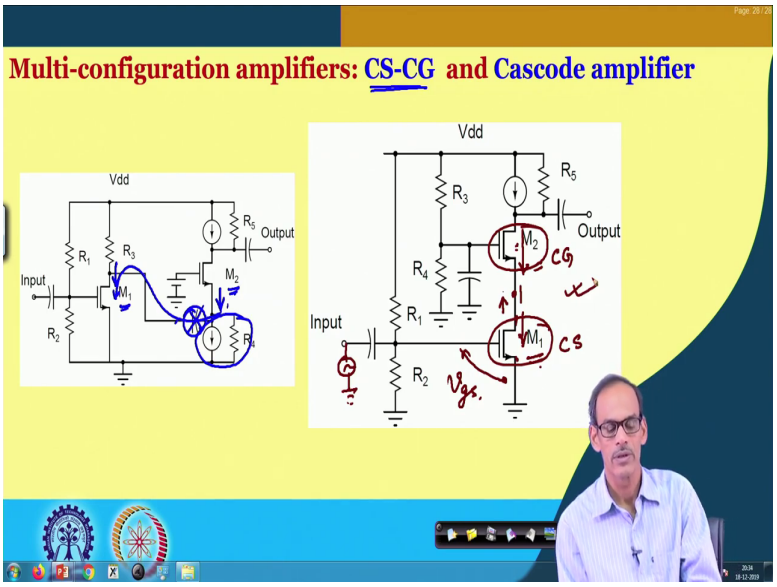
So, it conveys the current from the source node to the drain node without any amplification. But here the purpose here it is to convey the current from low impedance node, source node to the high impedance node the drain node ok. So, now coming to the main discussion how the common gate amplifier it can be used as a voltage gain booster along with the common source amplifier.

So, here we do have the common source stage, followed by the common gate stage. Similar to CE followed by CB, here also either we can isolate the DC operating point of the 1st stage and 2nd stage by placing a DC decoupling capacitor there, and only feeding the signal from 1st stage to the 2nd stage.

The; however, the better version it is that we can probably directly couple the signal without this capacitor. And whatever the bias requirement for M-1 and M-2, we can try to see whether they can complement each other and then they can help us to avoid this bias circuit and this bias circuit.

So, that gives us the cascode configuration. So, the circuit what we have drawn here initially it is common source followed by common gate and then if you do this kind of modification that gives us the cascode amplifier in the MOSFET version. So, similar to BJT, here also it is feasible in the next slide we are discussing that.

(Refer Slide Time: 05:28)




So, here we do have the circuit we do have the original common source followed by common gate. And as I said that if we remove this capacitor, and then what we are looking for M-1. It required some DC current need to be supplied to its drain. And at the same time M-2 needs its source current need to be consumed by some bias circuit.

So, if we directly couple here then what you can do the source terminal current of M-2, it can directly supply the required drain terminal current of M-1. So, here what we can see the current of M-1, it is helping to provide the bias for sorry current of M-2 it is helping to provide the bias of M-1 and vice or vice versa.

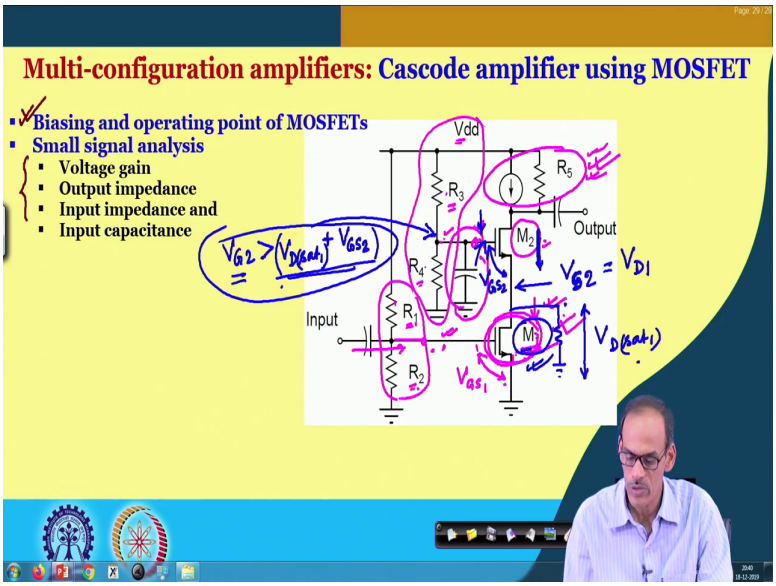
So, here the connection it is direct connection and similar to BJT cascode, here we are we will be discussing that how the signal it is propagating from this stage; the common source stage to

the common gate stage. So, we can say that M-2 it is performing the common gate configuration. Whereas M-1 it is performing the role of common source configuration.

Now first of all the signal we are giving the giving at the gate of transistor 1 which is making meaningful V gs here. And this V gs it is producing GM into V gs voltage dependent current. And that current we are expecting it is coming from transistor 2 or if I say that we are producing a signal current in this direction this current it is entering into this one M-2.

Now, how much portion of this current it will be entering into M-2? That can be; that can be analyzed by considering small signal equivalent circuit or the this cascode amplifier. So, in the next slide we will be talking about the small signal equivalent circuit of this cascode amplifier. Maybe you can independently try it out.

(Refer Slide Time: 08:10)



So, this is the; this is the cascode amplifier circuit and then the biasing. So, the analysis part it will be done by considering its small signal equivalent circuit. But just prior to that, let me put few words about the biasing and operating point of the 2 MOSFET transistors.

So, what we have here in the biasing side? For M-1, we need to provide a voltage here, at its gate sufficiently high. So that this transistor it will be on and that is done by this potential divider which is getting constructed by R-1, R-2 and the supply voltage.

So likewise, at the gate or transistor-2, we are giving a DC voltage which is coming from this potential divider constructed by R-3 and R-4. So depending on their ratio we are generating a voltage here. Likewise, depending on the R-1, R-2 ratio, we are providing a voltage here. Now we are feeding the signal at this point, but at this node we want this signal this node to be AC ground for proper operation.

So, this node we are at this node we are connecting a large capacitor to ground to make it really AC ground. Now, while this M-1 it is getting its gate voltage and source node it is connected to ground. So, that gives us V GS for this transistor. And then this V GS and its dimension it provides a an expression of this current. Now this current it is coming from M-2. So M-2 is not having any problem.

But then this current whatever the current it is defined by size of M-1 and its corresponding bias it must be consistent with whatever the bias circuit we do have here. So, similar to BJT counterpart, the matching of the current source here and the DC current or transistor 1 coming from its bias is very important. If it is not taken care then probably M-2 it will be entering into triode region.

And if it is further mismatch it is there then, maybe M-1 also entered, will be entering into the triode region. Or there is another possibility of course, that it may push this circuit into malfunction. And as a result the consequence it will be that the amplifier may not give good performance. So, while we will be designing this circuit, we need to take care of proper matching of DC current of transistor 1 and whatever the bio-circuit we do have.

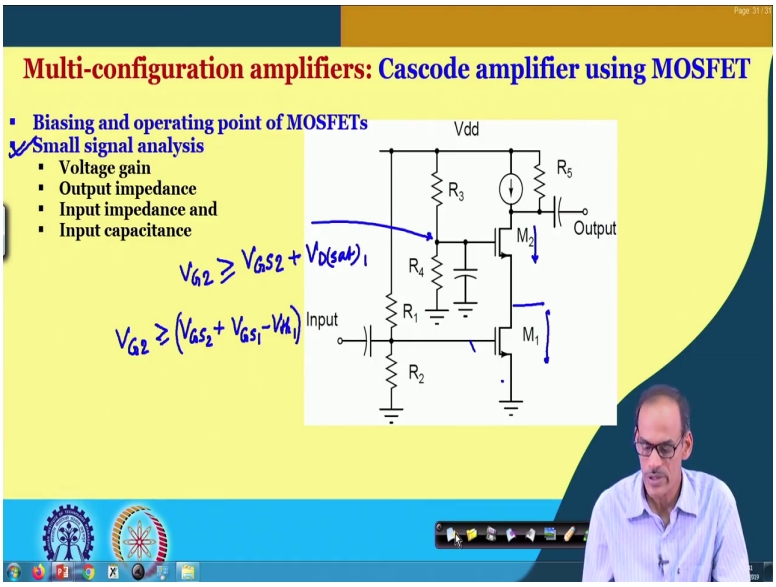
On the other hand, while we are providing the gate bias at the gate of M-2. Then, to support this current it itself adjusts its V GS V GS-2. In other words, based on the voltage at this point minus this V GS or transistor 2 provides the DC voltage here. Which is of course, the source voltage or transistor 2 which is also equal to drain voltage of transistor 1.

So, we need to maintain this transistor into saturation region; otherwise its output the drain to source resistance it will be; it will be small, and that may create a problem. So, for proper operation we will like to keep transistor 1 in saturation region and that should be done by maintaining at least some minimum voltage here, which is referred as VD sat or transistor one.

So, this voltage if it is higher than VD sat, then of course there is no problem. In the in other words, the voltage here the gate voltage of transistor 2 it should be sufficiently high compared to minimum required VD sat here for transistor 1. Plus, whatever the V GS-2 that is necessary to support this current.

So, as long as the gate voltage here it is, this gate voltage it is higher than this limit, then we do not have any problem. So, it may not be very difficult to satisfy this condition, but unless you pay attention you may miss out this important information; and that may force the transistor particularly this transistor into triode region.

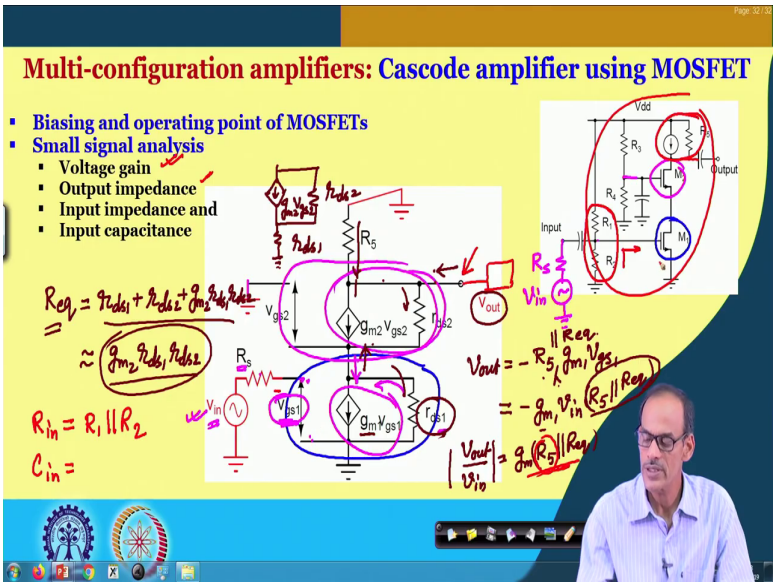
(Refer Slide Time: 13:50)




So, in summary what we, in summary what we like to say here that the gate voltage here V G2 should be more than or equal to required V GS2 to support this current Plus, VD sat or transistor 1 and VD sat of this transistor 1 eventually it is this VGS minus V th.

So, I should say V G 2 should be higher than V GS 2 plus V GS1 minus V th 1 ok. So, if you satisfy this condition then there is no problem, ok. Now, once we get the proper DC operating point, next thing is that the analysis for voltage gain and output impedance and so and so. And to do that, we need to draw the small signal equivalent circuit similar to BJT cascode amplifier. We also have drawn this small signal equivalent circuit here.

(Refer Slide Time: 15:05)




So, this part it is this part it is for M 1. On the other hand, this part it is for M 2 and the gate of M 2 it is connected to AC ground here. And at the gate of M 1 we are feeding signal. We are feeding signal V in and the signal source may be having a source resistance of R s.

And then we do have V gs getting developed, based on the input signal here. So, we can say that drop across this R s, it is DC wise it is 0. Even, signal wise you may ignore. So, we can say that V gs 1 it is same as V in. Unless, otherwise we consider the input capacitance here. Note that here we do not have R pi namely gate two source resistance is infinite.

So, this circuit it is, in fact, simpler than the BJT version. So, now, this input which is appearing across this gate 2 source of transistor 1, it producing it is producing gm into V gs,

here. And, this current you can say that it is coming from this circuit. And of course, this current part of the current it may be coming from this r ds 1 also.

But typically, the impedance looking into; looking into this circuit it is much smaller than whatever the impedance we do have. So, we can say almost this entire current it is coming through this circuit. And as a result, it is arriving to the output node, and if it is while it is flowing through this R 5 it is producing the corresponding voltage, V out. So, the V out we can say it is minus R 5 multiplied by gm 1 into V gs 1. And so, this. In fact, part of this current it will be flowing through this as well as this also.

So, I should not say this current it will be flowing only through R 5. In fact, I should consider parallel connection of whatever the equivalent resistance we will be getting here. In fact, it can be shown that this final V out it is minus gm 1 into V gs 1 which is V in. And this multiplied by R 5 in parallel with R equivalent.

In fact, this is the output resistance. So, if we look into this circuit that is the output resistance. And, we also have discussed about the R equivalent resistance for such kind of circuit. And the this circuit, what is the specialty of this circuit? We do have the active device, providing voltage dependent current source then r o or r ds 2.

And this is gm 2 into its corresponding V gs 2. And then we do have resistance here which is r ds 1 connected to ground. So, we can say this R equivalent it is r ds 1 plus r ds 2 plus gm 2, r ds 1 multiplied by r ds 2. That can be well approximated by the luster namely gm 2, r ds 1 into r ds 2. So, this resistance it is quite high. So, the that may give very good gain.

So, if I say the voltage gain V out divided by V in; and particularly its magnitude, it is gm 1 multiplied by R-5 in parallel with this R equivalent. And this R equivalent it is quite large. And to get very good gain what you can do we can try to increase this R-5 also in the same order. That can be obtained by considering active current source there.

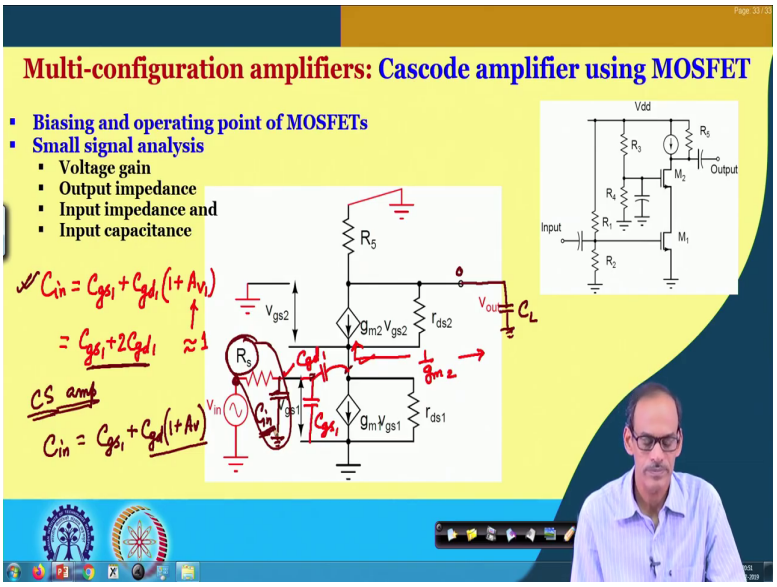
Maybe, cascode current source we can put there and then we can get very good gain. So, that is how we can say that it is helping us to get higher voltage gain. But then of course, the output impedance here it will be quite high to achieve the gain.

So, if we try to directly sense this voltage through some subsequent circuit which may offer significant amount of capacitance. So, that may limit the bandwidth. So, that is of course, is an issue that can that may be addressed by putting a buffer here. Namely, common drain kind common drain stage which we already have discussed.

But if I focus only on this circuit, I should say it is having potential to increase voltage gain by increasing the output impedance. Now, input resistance of course, here it is I should say, this circuit provides input resistance, it is infinite. So, whatever the input resistance we will see it is coming from R 1 parallel R 2.

So, R in of this cascode amplifier it is R 1 coming in parallel with R 2. On the other hand, the input capacitance C in, it is coming from the C gs and C gd or transistor 1. So, let me erase and then make the space for calculation or expression. C in it is coming from CGS.

(Refer Slide Time: 22:03)




So, that C gs is coming as is in parallel with C gd, but that is affected by Miller factor. So, C gd 1 multiplied by 1 plus whatever the gain we are getting from this node to this node.

And again, here we may consider that the impedance at this node coming from the upper circuit, it may be in the order of 1 by gm 2. So, that gives us the corresponding voltage gain here it is approximately 1. So, the input capacitance here it is C gs 1 plus 2 times C gd. On the other hand, if I consider simple common source amplifier, as we know that for common source amplifier, the corresponding C in it is C gs plus C gd multiplied by 1 plus its voltage gain.

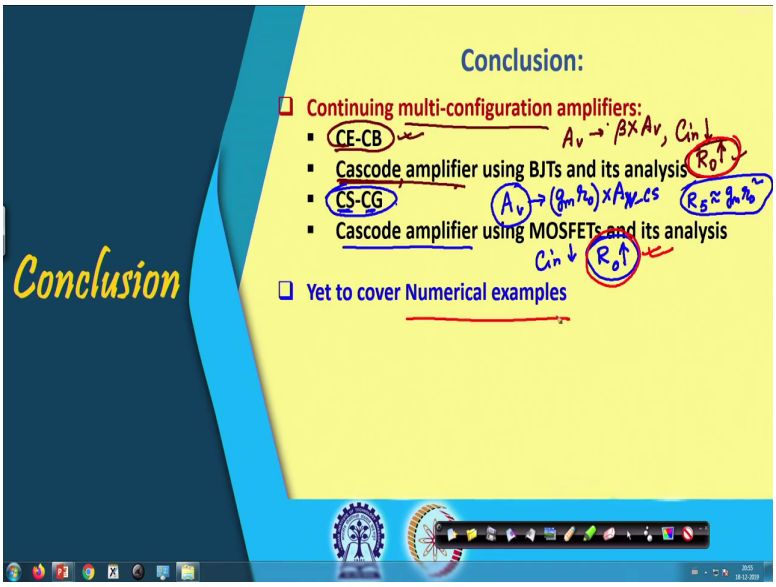
So, because of the reduction of the voltage gain here then input capacitance it is getting reduced. What is its consequence? In case if the bandwidth of the whole system it is defined by

this R s and the input capacitance coming at this node, then we can say that if we can reduce this C in, that helps us to extend the bandwidth, ok.

So, based on the situation we may say that this is giving us some advantage particularly in terms of extending the bandwidth. But the assumption of course, here it is we assume that the system bandwidth starting from this point till the primary output, it is predominantly defined by this RC time constant. Then only that claim it is valid.

Otherwise, if the upper cut-off frequency it is defined by say CL and say R out then of course, by reducing this input capacitance, it will not be helping to improve the bandwidth. I think most of the things we have discussed whatever we have planned today.

(Refer Slide Time: 25:02)



So, in conclusion what we have is that, we have continued the multi-configuration amplifiers. And today, what we have discussed, it is that common emitter amplifier cascaded with common base and with some modification in the biasing arrangement. What we obtained it is something called cascode amplifier. Note that this cascode this word it is not grammatically correct.

But technically, that is the name it is used. Then we have seen the advantage of this cascode amplifier compared to standard CE amplifier. Namely, the voltage gain it got increased by a factor of almost beta. So, this got increased by a factor of Beta of cascode transistor compared to CE amplifier. Also, we have seen that input capacitance it got decreased.

But then the drawback of course, the output resistance got increased. And that need to be handled by some means. So, as long as this is allowed we can go for this cascode amplifier. So, on the other hand for MOS-based circuit, we have seen the common source followed by common gate. That gives us the with bias modification; biasing modification we have obtained the cascode amplifier.

And there also we have seen that the voltage gain. So, voltage gain got increased by a factor of intrinsic gain of the cascode transistor. Provided the load part it is properly implemented namely in our example. Assuming this R 5 it is in the order of gm into R naught square.

So, if this is valid then you can say that the gain of the cascode amplifier it is gm times R naught times whatever the gain we do have on the common source amplifier. AV of common source amplifier. So, and also we have seen that input capacitance it got decreased.

And because the first stage gain it got decreased. And then, but then the cost is output resistance got increased. So, this is of course, it is not a good thing, similar to this one. So, as long as it is allowed to increase the output resistance this may be a good scheme we yet to cover the numerical examples. Probably in the next class or next to next class we will be talking about that. I think that is all I do have.

Thank you for listening.