Analog Electronic Circuits
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Lecture – 59
Multi-Transistor Amplifiers (Contd.):
Numerical Examples (Part B)

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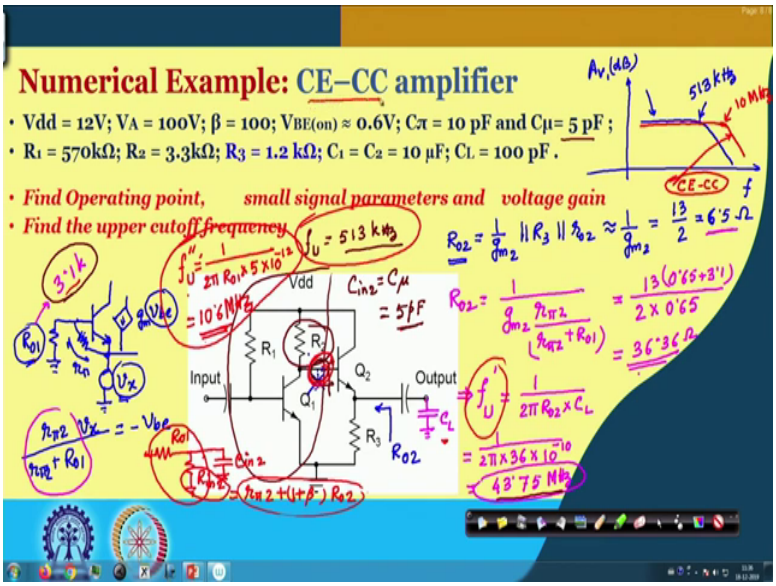

Welcome back after the short break. So, we are talking about the CE CC and now we will be moving to MOS counterpart.

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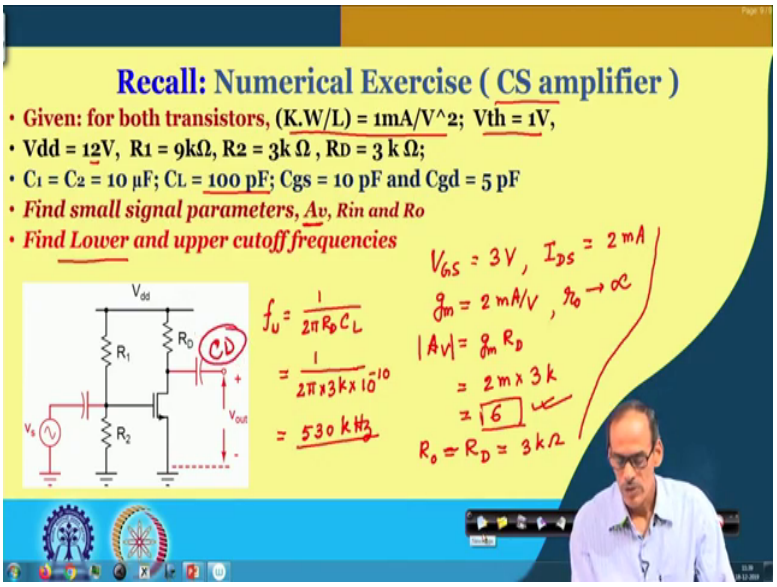

So, in the next slide we will be talking about see common source amplifier again this numerical exercise we have seen before. So, this is prime and the main common source amplifier and sorry and then we have the information given here about the device namely K into W by L which is 1 milli ampere per volt square, threshold voltage it is 1 volt, supply voltage it is 12 volt and so and so.

And, we have seen that using this information we obtain V GS equals to 3 volt and then I DS we obtain it was 2 milli ampere and then corresponding small signal parameter g m it was 2 milli ampere per volt. So, the corresponding voltage gain; voltage gain it was g m into output resistance and you may ignore the r naught or other r naught we may consider this is very high assuming lambda is very small. So, the voltage gain it was g m into R and so that becomes 2 milli into R D is 3 k; 3 k.

So, the corresponding voltage gain it was only 6. So, whatever it is and then the output resistance for this case we see it is primarily defined by R D and that is 3 kilo ohm. So, the upper cut off frequency for this case f u it was 1 by 2 pi R D into load capacitance of 100 pico Farad. So, it was 1 by 2 pi and then 3 k into this one 100 pico; that means, 10 to the power minus 10 yeah. And in fact, if you calculate it this gives us 530 kilo Hertz.

So, the common source amplifier it is primarily it is having a gain of 6 and then upper cut off frequencies 530 kilo Hertz, we are not going to calculate the lower cut off frequency primarily because our intention here is to see the enhancement of the bandwidth by the use of common drain stage. So, please recall or try to remember this information. In our next exercise where we will be cascading this CA stage by common drain stage.

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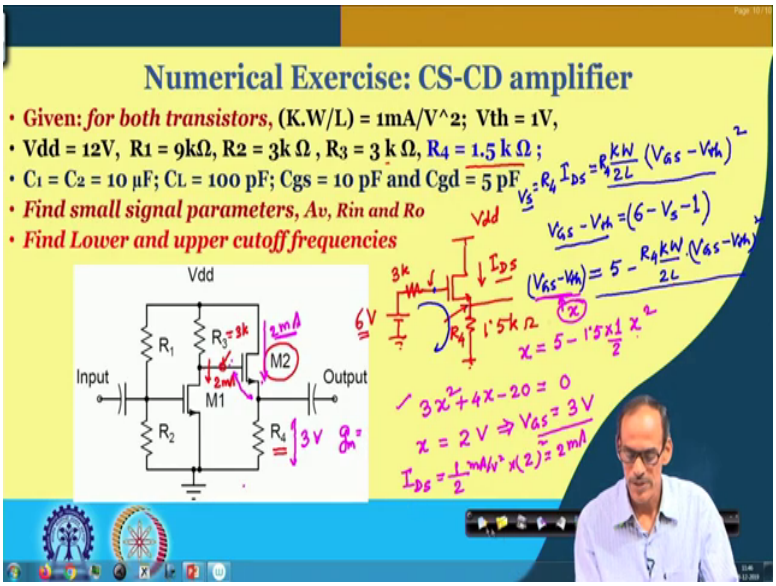

So, we do have in the next slide we do have that example here. So, all the information's are we are keeping it same we do have additional C common drain stage coming out of the transistor M2 and the its bias circuit R 4 and R 4 it is given here it is 1.5 kilo ohm

Note that its biasing it is done directly from the DC voltage available at the drain of transistor 1. So, the DC voltage coming here if you see the current flow of here it is 2 milli ampere and R 3 it is 3 k. So, drop across this 3 k it is 6 volts. So, we can say that we do have a DC voltage of 6 volt coming to the gate of transistor 2.

So, we do have R 4 here 1.5 k and its drain it is connected to V dd. Now, how do you find the corresponding current here I DS? So, there is a method first of all this I DS flowing through this R 4 creating a drop which is defining the source voltage here and then at the at the gate we do have 6 volt.

And since there is no current flow even if you consider the 3 k resistance here, but still we can say that gate voltage it is 6 volt. So, if I consider the loop here if I consider this loop and if I consider we do have 6 volt coming here. So, we can say that the I DS I DS equals to whatever KW by L by 2 into V GS minus V th square and then if I multiply with R 4.

So, if I multiply with R 4 here. So, that gives us the source voltage, but then gate voltage it is 6 minus 6 voltage. So, we can see that V GS; V GS minus V th equals to 6 volt minus this V s minus V th is 1 volt ok. And so what is this one we do have 5 here and then V s we do have this expression which is given here.

So, you can say directly this is 5 minus R 4 KW by 2 L into V GS minus V th square. So, that is the expression of the V GS we are getting. So, now, we are we do have one equation here which is in terms of V GS minus V th. So, if we can find the V GS minus V th, then we can see that we can find the corresponding current.

Now, since this equation it is coming primarily in terms of V GS minus V th let me consider this is x. So, we can say that this is x equals to 5 minus R 4 it is 1.5 k and KW by 2 L it is 1

milli. So, we can say k and milli they are getting cancelled and then we do have V GS minus V th, so that is x square all right yeah.

So, we do have by 2 also yes. So, now, from this one what we can we can rearrange this equation. So, that gives us in fact, 3 x square plus 4 x minus 20 equal to 0. So, if you solve this equation second order equation what you will get here is one solution it is x is equal to 2,you will get x is having some other value also, but that value it is impractical.

So, we can see that x is equal to 2 volt which gives us V GS equals to 3 volt because x is V GS minus V th. So, this quantity V GS minus V th we have considered it is x. In fact, if you plug in this V GS value, we can get the I DS equals to we do have I DS equals to 1 milli ampere per volt square by 2.

So, 1 divided by 2 here. So, that is milli ampere per volt squared into V GS minus V th and that is 2 square. So, that gives us 2 milli ampere. So, we do have a current flow here it is 2 milli ampere. In fact, you can verify that if 2 milli ampere of current is flowing here from drain to source the drop getting created here it is 3 volt and we do have 6 volt here.

So, that makes the V GS is also 3 volts which is consistent because if I am having V GS 3 volt then only it will support the current of 2 milli ampere of course, assuming this transistor it is in saturation region of operation. So, that is how you can get the operating point of the transistor in CC stage and using that you can calculate what will be their corresponding gm.

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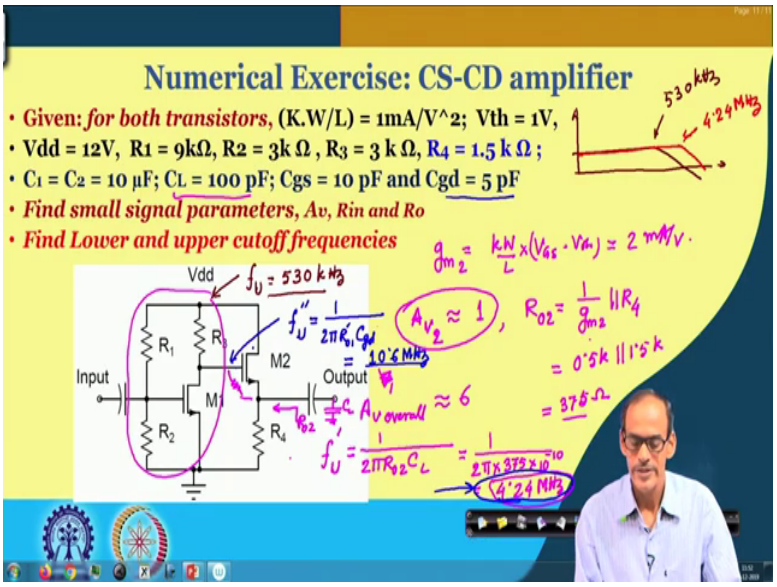

So, the gm of this transistor it is let me create some space here. So, gm of transistor 2 it is we do have KW by L into V GS minus V th. So, here also we got g m 2 equals to 2 milli ampere per volt and then the output resistance and of course, since we do not have the equivalent whatever R pi we are having in BJT.

And so the calculation here it is much simpler and you can approximate that the gain here A v 1, it is very close to 1 and output resistance not A v 1 A v 2 rather second stage gain and output resistance of the CC stage it is one by gm 2 it is in parallel with R 4 ok. So, 1 by gm 2 it is 0.5 k and R 4 it is 1.5 k.

So, that gives us I think 300 something I do have a calculation yeah. So, that gives us 375 ohm. So, since the gain here it is approximately 1, so the overall gain it is primarily coming

from the first stage. So, the overall gain A v overall it remains 6 only, but then the upper cut off frequency f U.

Now, if I call it is f U dash it is having 2 candidates to define the upper cut off frequency; one is R o 2. So, this is 2 pi R o 2 and the corresponding load capacitance we do have C L. So, if we connect the C L here. So, then the upper cut-off frequency it is 1 by 2 pi into 375 into 10 to the power minus 10 and yes I do have calculation here, it is 4.24 mega Hertz.

So, you may require you can compare this frequency with respect to whatever the original pole of this CA stage it was there. So, that was f U it was 530 kilo Hertz. Now, also we have to consider the other candidate of defining the upper cutoff frequency coming from this point and that is let me denote that by f U double dash and its expression is 1 by 2 pi R o 1 and then Cgd.

So, Cgd it is 5 pico Farad and. So, the value of this this cutoff frequency in fact, since this is 3 kilo and this is 5 pico earlier we made this calculation and it was 10.6 mega Hertz.

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Now, if I compared these two poles together of course, this is lower. So, the net upper cutoff frequency it is four point, so 4.24 mega Hertz. So, here also the same conclusion it is namely originally the CS common source amplifier it was having a gain of 6 and then it was having a; it was having a the upper cutoff frequency it was 580 kilo Hertz. Now, we are by the virtue of the common drain stage along with the CS.

So, this gain it is almost remaining the same and its bandwidth got extended to 4.24 mega Hertz ok. Now, so that gives us the flavour of why we go for cascading CC and CD. In fact, you can try out with the other CE amplifier which is cell biased configuration.

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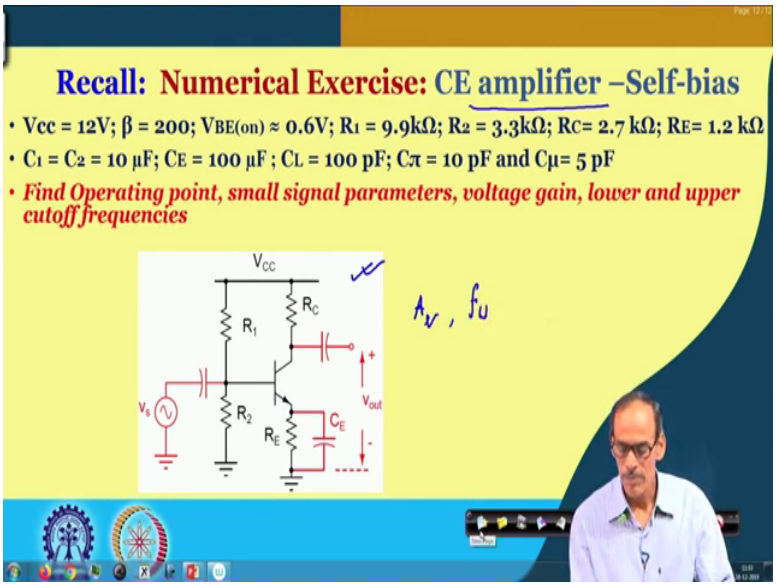

So, this exercise we have done before. So, probably you can calculate what is its voltage gain and the upper cutoff frequency.

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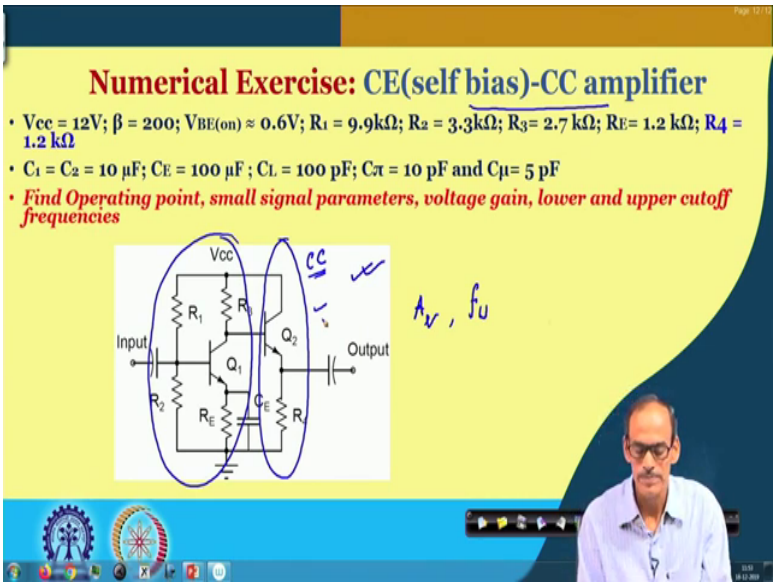

And then you can compare this with the cell biased CE amplifier sorry cell biased CE amplifier along with say CC stage. So, we do have the CC stage here and you can find that again this CC stage it is helping to extend the bandwidth. So, probably you can work out on this one. I do have another interesting example, but again due to the probably the shortage of time.

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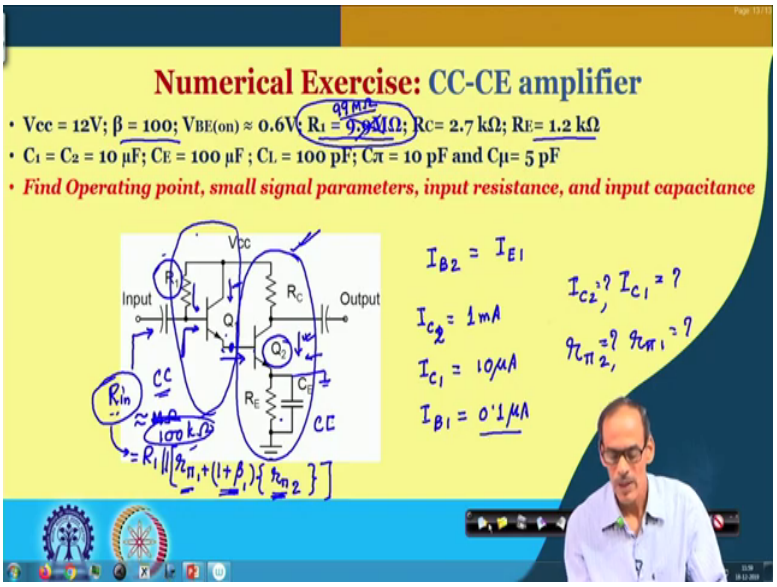

I will just give you some brief and then I will be leaving it to you to solve this problem. What we have here it is yeah; what do we have here it is this is the CE stage assuming we do have a meaningful DC voltage coming here from the previous circuit and then that is preceded by CC stage. Note that I am not providing any separate bias here for CC stage and on the CE stage.

So, we are assuming that whatever the current is coming from Q 1, its emitter current it is getting consumed by the base terminal of Q 2. So, I should say that I B 2 is equal to I E 1 indicating that the current level here it is much lower than whatever the current level we do have. In fact, if you consider for both the transistors beta is say 100.

So, whatever the current we do have you can imagine that this current it will be 2 order magnitude lower. So, say for example, if I consider I C 1 it is 1 milli ampere. So, we are

expecting that sorry I C 2 if I consider I C 2 is 1 milli ampere, then I C 1 it is only 10 micro ampere and the corresponding I B I B 1 it is only 0.1 micro ampere.

So, we require very very small current here as a result the corresponding R 2 here; R 2 here we are expecting it will be sorry R 1 resistance bias resistance R 1 to support this much of current it should be definitely in maybe 10s or maybe even 100s of mega ohm. So, if you put some value of say even say close to 10 mega ohm you will see that the corresponding current here it will be quite high.

But, whatever the biasing condition you can get with this one probably you can see and then you can find what is the I C 2 and then I C 1 and then from that you can calculate what is the R pi 2 and R pi 1. From that you can see what is the input resistance it is coming here and you will see that by adding the CC stage the input resistance it will be quite high.

So, the input resistance expression you may recall it is coming from R 1 in parallel with whatever the input resistance we can see at the base of transistor 1 and that is R pi 1 coming in series with 1 plus beta 1 multiplied by R pi 2 and then if I consider this is ac ground.

So, only this much I will be having. So, you can see that this R pi 1 since its current level it will be quite small this will be quite high and then even though say R pi 2 may not be having. So, high value, but since it is getting multiplied by beta 1 the corresponding value of this resistance it will also be quite high as a result this R in 1 it may be in the order of mega ohms.

So, if I am having only on the other hand if I consider the input resistance of this stage only the R pi 2, it may be in the range of kilo ohms and the corresponding resistance we are getting here it is getting multiplied by 100. So, I should not say mega ohm it will be in the order of sub mega ohms I should say 100s of kilo ohms.

So, you can solve this problem by considering say R 1 is equal to say this mega ohm and maybe you can consider this resistance of 1.2 kilo sorry you should not take 9.9 mega ohm

rather 99 mega ohm. You can consider 99 mega ohm and then you can calculate what is the corresponding input resistance here see.

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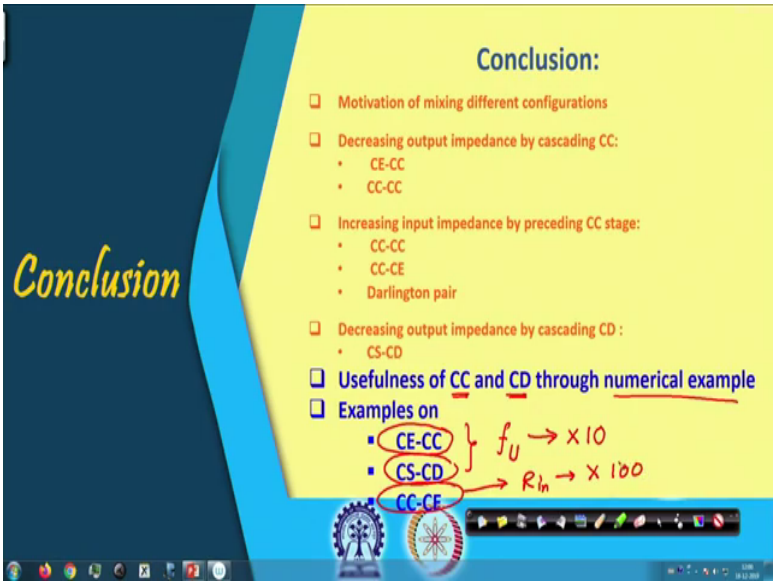

I think let me then summarize most of the things whatever we have planned we have covered here. So, in this session what we have learned here it is the usefulness of the common collector and common drain and we have we have demonstrated through numerical examples.

Basically, by considering CE and CC together and then CS and CD together to enhance the bandwidth upper cutoff frequency particularly getting increased by a factor of as is maybe a factor of 10 or more. And, also we have given one framed one example CE if preceded by CC to (Refer Time: 24:32) increase the input resistance R in by a factor of 100 ok. I think that is all I need to share.

Thank you for listening this talk.