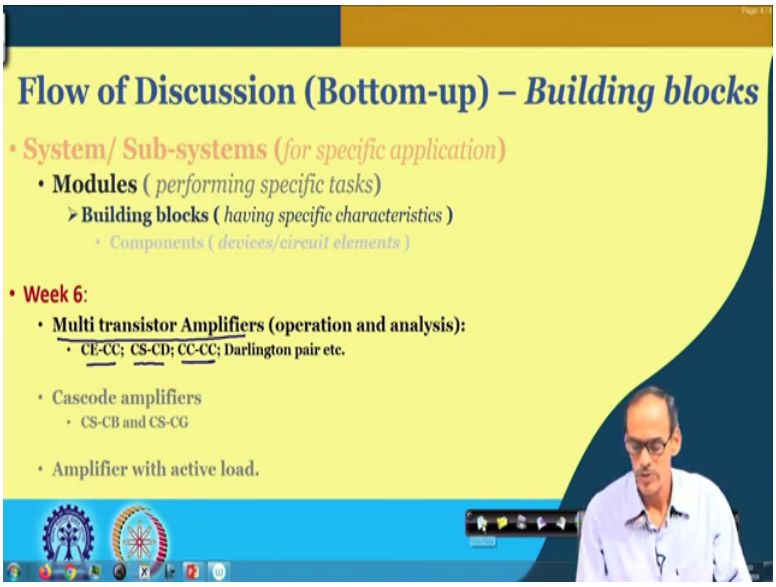
Analog Electronic Circuits
Prof. Pradip Mandal
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture – 58
Multi-Transistor Amplifiers (Contd.): Numerical Examples (Part A)

Dear students, welcome back to our online certification course on Analog Electronic Circuits. Myself, Pradip Mandal, from E and EC Department of IIT, Kharagpur. Today's topic of discussion it is Multi Stage Amplifiers rather continuation of multi stage amplifier. And, in the previous three lectures so, what we have seen is the theoretical aspect of going for multi transistor amplifiers where we do have mixed configurations namely CE, CC, CM and so and so.

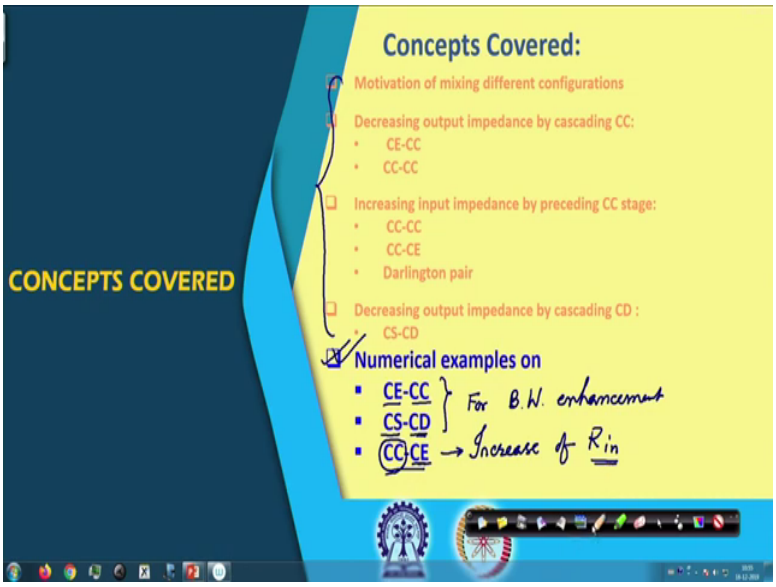
Today, we are going to discuss little more about numerical problems and demonstrating the same conclusion what we have discussed theoretically.

(Refer Slide Time: 01:20)



So, as I said that our according to our over overall plan we are at multi transistor amplifiers and theoretical parts of CE-CC, then common source-common drain, then common collector-common collector, Darlington pair. Those configurations it has been discussed from the circuit analysis point of view and today we are today we are going to have more numerical problems.

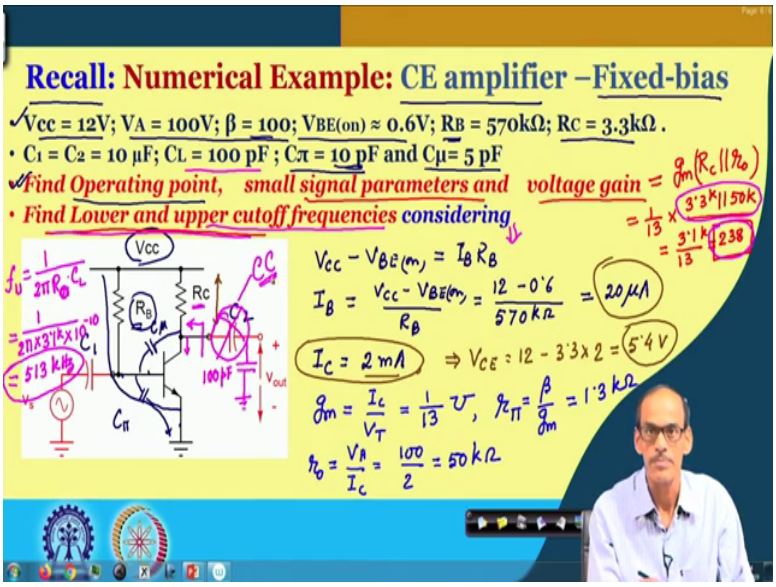
(Refer Slide Time: 01:54)



So, here again the same summary here the concepts we already have covered particularly the theoretical aspects of mixing different configurations are covered. And, we are going to discussed about numerical examples of particularly for CE followed by CC common collector stage to enhance the bandwidth of the amplifier and. So, similarly for MOS counterpart common source followed by common drain, it gives the enhancement of the bandwidth.

So, these two configurations are for bandwidth enhancement and the third example it is to demonstrate that increase of input resistance R in. So, compared to CE amplifier whatever the input resistance we have seen here we will demonstrate that if you precede this circuit by common collector stage the input resistance it is getting increased.

(Refer Slide Time: 03:27)



So, let us go to the numerical example. So, this slide is a recapitulation of one of our previous numerical examples where we have discussed about CE amplifier having fixed bias arrangement and different different parameters are given here including the supply voltage of 12 volt, then device parameters including beta of the transistor, early voltage, then V BE on and then also we do have the bias circuits resistances are given here R B then collector resistor and so and so.

And, the coupling capacitors informations are also given and then the device in intrinsic capacitances namely C pi and C mu are given are here as. So, this is C pi as and it is value it is given 10 pico Farad and C mu it is 5 pico Farad. And, based on that information what we have done is that we obtained operating point. So, just for your information I will repeat some part of it and then we will see that how enhancement can be made on this one.

So, let us try to see the operating point of the transistor. So, whatever the arrangement we do have here namely the fixed bias V BE and then V BE at this node essentially the V CC it is directly coming to the base node through this R B and if I consider the K CL as you may recall K CL from supply voltage to ground and the drop across this R B then V BE drop we can get the expression of the I B and then we can get the numerical value of the I B.

So, we can say that V CC minus V BE on. So, that is equal to I B multiplied by R B. So, that gives us I B equals to V CC minus V BE on divided by R B. So, it is value it is now 12 minus 0.6 divided by R B it is given as 570 kilo ohm. So, that gives us the I B current of 20 microampere and then using this information and the beta information we are getting the collector current which is equal to 2 milli ampere.

Now, with this information we can find the value of the small signal parameters namely g m. In fact, let me complete this part and then I will be coming to the small signal parameter. So, we do have I C equals to 2 milli ampere then drop across R C equals to 2 milli ampere multiplied by R C it is 3.3.

So, that gives us V CE equals to 12 volt minus 3.3 into 2 which is 5.4 volt. So, the operating point it has given here and based on this operating point we can now calculate the small signal parameters value namely g m equal to I C divided by V T and this is 1 by 13 mu and then the r pi which is beta divided by g m.

So, that is equal to 1.3 kilo ohm and then r naught it is V A divided by I C. So, that is equal to 100 divided by 2, 50 kilo ohm. And, from that we can get the voltage gain. So, now, we obtained the small signal parameter now we can get the voltage gain. So, voltage gain it is g m into R C in parallel with r naught. So, the g m we have 1 by 13 and R C it is 3.3 k in parallel with 50 k. So, probably you can approximate this by 50 or probably you can calculate this parallel resistances together and then you can find what is the output resistance.

So, that is coming close to 3.1 in my calculation it is 3.1. So, that gives us 3.1 k divided by 13. So, that is 230, in my calculation it is 238. So, that is the gain we are getting. Now, next thing is that we can find the lower and upper cutoff frequency.

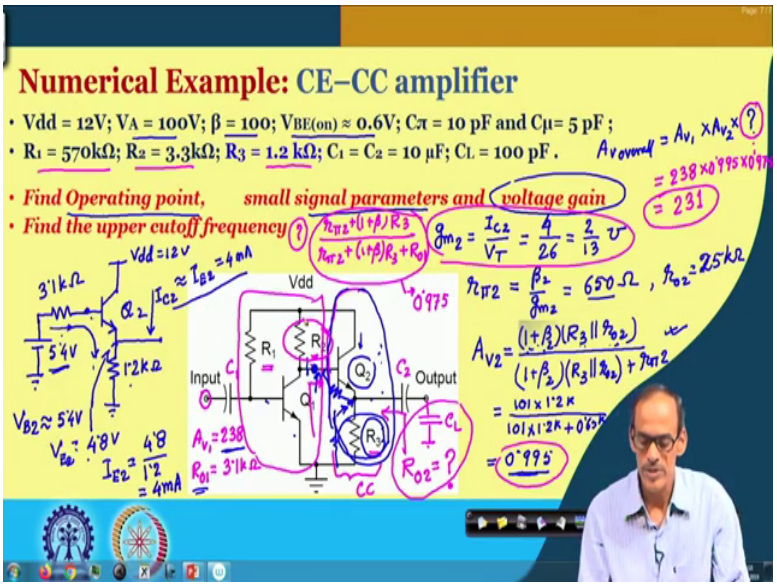
So, this is the; this is the exact statement of the problem we have address earlier. Now, for our main focus to demonstrate how the bandwidth it will be extended we can probably calculate only the upper cutoff frequency using whatever the information we do have and you may recall the upper cutoff frequency it is considering whatever we do have here.

So, upper cutoff frequency let me use the space it is expression is 1 by 2 pi then R out of this stage multiplied by whatever the C L we may be having and the value of the C L it is given 100 pico Farad. So, that multiplied by C L and this resistance if I call R O, let me call this is R O and we already have done this calculation on this R O which is 33 kilo 3.3 kilo in parallel with R O here.

So, the value of this upper cutoff frequency can be obtained by considering that 3.1 k multiplied by 10 sorry 100 pico Farad which is 10 to the power minus 10. And, that gives us I have done the calculation for you. So, this is coming 513 kilo Hertz.

So in summary what we have circuit performance why should you have the circuit gain is 238 and then the upper cutoff frequencies 513 kilo Hertz. Now, the exercise we are going to do it is that we are going to put in this case instead of putting the capacitor here we can probably directly put a CC stage here and rest of the things we will be keeping same. And, then we will see that how this the bandwidth particularly bandwidth is getting extended by putting the CC stage there.

(Refer Slide Time: 13:09)



So, in the next slide we do have the a CE followed by CC and the information about all these biases are maintained namely R 1 earlier it was R B and then R 2 it is actually the R C of the first stage and then we do have the CC stage. So, the CC stage it is this has been added here and the value of this resistance it is bias circuit it is given you as 1.2 kilo ohm and the C 1 and C 2 we are keeping same. C 1 and C 2 it is 10 micro Farad and then C L instead of connecting the C L at this node we are connecting the C L after the CC stage.

And, to get the overall gain starting from the primary input to primary output first of all this part we already have done and we have seen that it is gain it is if I call AV 1 it is gain it is 238 and then it is output resistance if I call R O 1 which is 3.1 k and then. So, these two informations are important and then to get the overall circuit performance we need to see what

is the; what is the small signal parameters we do have out of this CC stage. But, to get the small signal parameter we need the operating point of the this Q 2, so, how do you find?

We know that dc voltage coming here it is 5.4 volt in our previous analysis we have done that. So, if I say that we do have a 5.4 volt DC. So, that is 5.4 volt along with it is Thevenin equivalent resistance which is R O1. So, that is 3.1 kilo ohm that is coming to the base of transistor 2 and the transistor 2 emitter of transistor 2 it is connected to ground through this R 3 and R 3 it is 1.2 kilo ohm. So, this is our output and this node it is connected to the supply 12 volt.

Now, if I analyze this circuit and again if I consider device parameter same as Q 1 namely V BE beta and early voltage it is a same and then analyzing this loop what you can get is the value of the I B value of the I E and so and so on. So, you may ignore the drop across this resistance due to flow of I B. So, you can see that this 5.4 volt it is directly coming into this. So, we can say that V BE 2 it is approximately equal to 5.4 volt.

And, then we do have 0.6 voltage based to emitter voltage and then we can see what is the voltage here coming here it the voltage DC voltage coming here it is 4.8 volt. So, that is the emitter voltage and that gives us the current flow through transistor 2 which is 4.8 divided by 1.2. So, we can say that the emitter current it is equal to 4 point not 4.2 4.8. 4.8 divided by 1.2. So, that gives us 4 milliampere of emitter current and we may approximate that the collector current it is also equal to emitter current. So, I E 2 equals to 4 milli ampere.

So, using this information what we can get the small signal performance parameter namely g m 2. So, the g m 2 it becomes I C divided by thermal equivalent voltage which is equal to 2 4 divided by 26; that means, 2 divided by 13 mho and the r pi 2. So, that is the that is beta divided by g m. So, that is equal to 650 ohm ok. So, you might have observed that the r pi here and r pi here they are different because they are current levels collector current levels they are different. Now, using this we can find what will be the gain of the CC stage.

So, what is the expression of the gain of the CC stage? If I call this is A V2 gain voltage gain of the second stage if of course, it will be very close to one that is the anticipation, but to get

precise value you may recall it is expression it is 1 plus beta into the resistance here in fact, you may ignore r naught. So, of course, this r naught it is 25 kilo ohm.

And, this 25 kilo ohms you may ignore compared to whatever 1.2 kilo ohm we do have and then the expression of the voltage gain it will be 1 plus beta multiplied by this R 3 in fact, this is in parallel with r o 2 which can be ignored and then 1 plus beta 2 multiplied by R 3 in parallel with r o 2 plus r pi 2.

So, if I consider we do have a signal at the base and how much the voltage it is coming here that can be obtained by considering this. You may recall that the this equation in case if you are unable to really you know intuitively get a feeling of that you can think of that we do have r pi here and at this point we do have an impedance coming from this resistance seen from the base. And, this resistance it will be seen at the base after multiplying with 1 plus beta and this resistance of course, we do have r naught 2 it is coming in parallel.

So, beta plus 1 into R 3 in parallel with r o 2 is essentially the resistance at this emitter and effect of this emitter rather seen at the base. So, whatever the impedance we can see here from here to here effective impedance seen from the base it is 1 plus beta times the corresponding resistance. But anyway you can consider their numerical value and so, this is 101 multiplied by 1.2 K and then we do have 101 into 1.2 K plus r pi 2 which is 0.65 K. So, that is giving very close to 1. In fact, I do have the calculation for you it is coming 0.995.

So, we do have the first stage gain here and then we do have the second stage gain. So, the overall gain. So, we can say the overall gain A V overall equals to A V 1 multiplied by A V 2 and also of course, we will be having some attenuation due to the loading effect coming there. So, we will see this part. So, what will be this part? It is the impedance at this node essentially it is loading the first stage. So, this factor whatever the question mark we are seeing here let us try to see that part.

It is the attenuation coming due to the loading effect and the load here it is the r pi 2 plus 1 plus beta into R 3 and that is loading the first stage which means I have to consider output

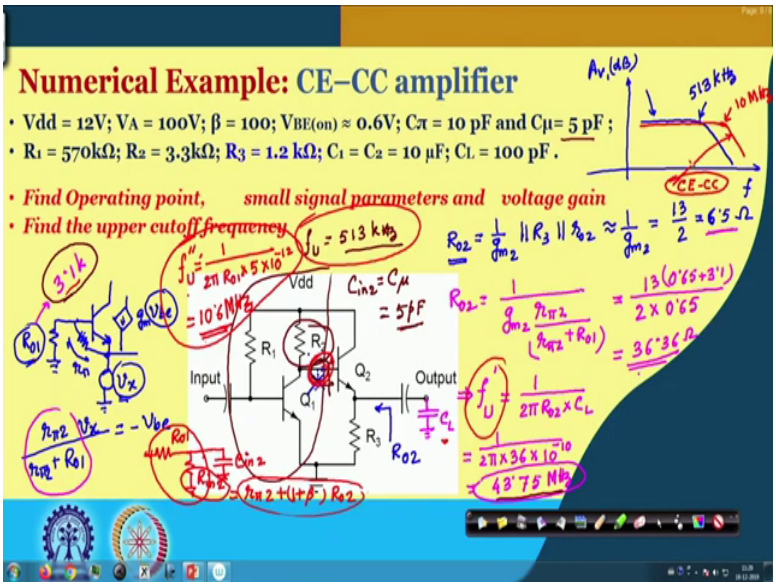
resistance of the first stage. So, this divided by r pi 2 plus 1 plus beta into R 3 plus R O 1. So, this is the attenuation factor.

So, that factor if you put it here in fact, if you put the value here whatever the value you will be getting this factor it is approximately coming very close to 1 in my calculation it came 0.975. So, I should say that the overall gain it is 238 multiplied by A V 2 which is 0.995 and then multiplied by 0.975 and that is coming very close to the original gain and it is in my calculation it comes 131 ok. So, that is a change, but the change is very small as anticipated.

Now, next thing is that how the a CC stage it is enhancing the bandwidth. So, how do we calculate the bandwidth first of all we have to see the corresponding g m and then we have to see what is the corresponding impedance coming there namely we need to calculate what is the R O coming from the CC stage namely R O2 we need to find and then we can find what is the corresponding cutoff frequency defined by this R O2 and C L together and then also we do have another candidate to define the cutoff frequency that whatever the input capacitance we do have coming from the second stage multiplied by whatever R O1 we do have.

So, to calculate the upper cutoff frequency we have to consider these two time constant ok. So, I will be using the same slide. So, let me clear whatever the clumsy equation now we have created.

(Refer Slide Time: 26:54)



So, let we consider the output resistance here. So, if I call this is R O2 ideally, if the this node is AC ground then R O2 should be equal to 1 by g m 2 in parallel with R 3 in parallel with r o2. So, that we may approximate by 1 by g m 2 and that is 13 by 2 that is point 6.5 ohm, but then this is not possible. We cannot do the AC ground here. So, we have to consider the corresponding resistance here.

In fact, for the CC stage we have to consider that the resistance at the base and this resistance is R O1 right and then we have to see what is the corresponding output resistance we do have. That can be obtained by considering the considering the drop it will happen across this r pi in presence of the R O1 while we are see stimulating this circuit by say V x.

So, I should say if I am applying V x at the emitter then base to emitter voltage it will not be exactly minus V x. As a result whatever the internal current source namely g m into V BE; so,

this V BE part it will not be entirely coming from minus V x rather this V x it is having some attenuation here. So, what is the attenuation coming due to this R O1 which is unbypass that is r pi divided by r pi plus R O1. And, in this case so, I have to consider r pi 2, this r pi 2 and then of course, if I multiply with V x so, that gives us minus V BE.

So, whatever the expression we obtained for this R O2 assuming that it is base node it is properly getting grounded that need to be change. So, what is the changed output resistance R O2 should be 1 by g m 2 multiplied by this attenuation factor. So, that attenuation factor it is r pi 2 divided by r pi 2 plus R O1.

So now we know the value of different parameters. So, we do have this is 13 by 2 and then r pi it is some r pi it is 0.65 kilo and R O1 it is R O1 earlier we have calculated it has 3.1 K. So, if I consider that 3.1 K and 0.65 3.1 K and that gives us the different value of on this R O2 and I do have this calculation for you. It is coming 36 36.36 ohm.

So, note that this is different, but still it is quite low and the pole it is getting created by this R O2 and then the C L. So, that gives us the new upper cutoff frequency. So, if I call this is f U dash and if you find what will be it is value that is 1 by 2 pi into this R O2 into C L.

So, that is so, that is becoming 2 pi into 36 into 10 power minus 10 Farad and in my calculation what I was getting here it is 43.75 mega Hertz. So, now, we may recall this is you can compare this value and previously obtained upper cutoff frequency, originally it was f U that was 513 kilo Hertz if we consider only this circuit, then if we connect the C L here then the bandwidth the or the upper cutoff frequency it was this one.

But, of course, this is not this is not this is not the only candidate to define the upper cutoff frequency you also have to see that what is the f U we are getting due to this R O1 and the input capacitance coming from this stage. And, what is the input capacitance we do have? C in 2 equals to C mu and the value of the C mu it is given here it is 5 pico Farad. So, the I should say a intrinsic or I should say device capacitance of say 5 pico Farad and then R O2 which is a 3.1 K they are providing the other possible option of the upper cutoff frequency.

In fact, not only you have to consider R O1 you have to consider the input resistance of this circuit also. So, at this point let me use different color here at this point whatever the pole we will be getting it is coming from we do have R O1 and then R in of the second stage and then we do have the capacitance coming from the second stage which is C in 2. So, I should say these two resistors they are coming in parallel to define the corresponding R.

So, the new candidate or the other candidate to define the upper cutoff frequency let we call it is f U double dashed and so, this is equal to 1 by 2 pi then 3.1 and we do have the this resistance. Of course, we the that resistance we have calculated, but somewhere we have we have missed it and what is it is expression it is r pi 2 in series with 1 plus beta times R O2.

So, you may ignore this part, but even if you consider this the corresponding resistance here it is coming very close to R O1. So, you can consider this is R O1 multiplied by now it is 5 pico Farad, instead of having 100 pico Farad of C L now we do have only 5 pico Farad seen by this resistance and this is 5 into 10 to the power minus 12 and it is value incidentally it is coming 10.6 mega Hertz.

So, I should say even though we do have now two candidates to define the upper cutoff frequency one is f U double dash and also we do have f U dash. So, these two if I compare this is lower. So, eventually this is defining the upper cutoff frequency, but still if I compare with the original upper cutoff frequency this adding the CC stage it is helping us to extend the bandwidth.

So, in summary we can say that if the original CE amplifier it is having a frequency response like this. So, it is having a gain. So, this is A V1 in dB and this is frequency in Hertz in log scale and this one was 513 kilo Hertz was the upper cutoff frequency. Now, by adding this CC stage what we have here it is the gain got slightly decreased, but then bandwidth got extended and this bandwidth it is 10 mega Hertz. So, almost 20 times enhancement of the in the bandwidth. And, this is due to so, this is due to the CC stage in fact, CE and CC together ok.

So, let me take a short break and then we will come back for the mass counterpart and then we will see that they are also by using common drain stage how it is helping us to extend the bandwidth ok.

Thank you.