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**Lecture – 57**  
**Multi-Transistor Amplifiers: Operation and Analysis (Part C)**

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**Multi-configuration amplifiers: Composite transistor**

Config.	$A_v$	$R_{in}$	$R_o$	$C_{in}$	$A_I$	Remarks
CE	High	High	High	High	High	Good Voltage amp & Current amp but needs suitable buffers (for cascading)
CC	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer and Power amplifier
CB	"High" with $R_s \neq 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and voltage gain booster

CC, CE  
CC-CC, CC-CE

So, dear students welcome back after the break. So we are talking about composite transistor. And what we said is that if we have amplifier particularly multi configuration amplifiers where two transistors are having different configuration or maybe the same configuration. Then the analysis can be done slightly you know smarter way.

And to do that what you can do two transistors together we can consider a single one say for example, you do have Q 1 and Q 2 together. Where Q 1 its collector is connected to supply V dd. And its emitter it is directly connected to transistor 2 and then at the emitter will

may or may not be having this bias current. And then the second transistor collector we can consider it is C collector of the composite structure. And then emitter of Q 2 it can be considered as emitter of the composite structure on the other hand base of the Q 1 transistor it can be considered base of the composite structure.

So, with that here the whole thing, the shaded portion if I consider one transistor and then if you find its small signal parameter. And then we can use this transistor for two configuration say common collector configuration and then common emitter configuration. So, the moment you make this composite structure in CC configuration then what will be we getting how CC followed by CC configuration we can get. So, likewise if the composite structure or composite transistor if you connect in CE configuration, then we can get CC followed by CE configuration ok. So, let us try to see that how we are getting it say.

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**Multi-configuration amplifiers: Composite transistor**

Config.	$A_v$	$R_{in}$	$R_o$	$C_{in}$	$A_i$	Remarks
CE	High	High	High	High	High	Good Voltage amp & Current amp but needs suitable buffers (for cascading)
CC	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer and Power amplifier
CB	"High" with $R_s \neq 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and voltage gain booster

CC-CE

We do have the basic composite structure here whether we do have this bias circuit or not if we connect the circuit in say CE configuration. So, which means that the emitter we can connect to ground and at the collector we can put a bias resistor  $R_C$  connected to  $V_{DD}$  supply. And so, we can call this is the output port and at the base we can connect maybe  $R_B$  providing the bias current for  $Q_1$  base bias current for  $Q_1$  and then we can feed the signal there with a meaningful DCA.

So, what is this circuit configuration we are getting is that, so what you are doing is that composite structure we are making in CE configuration. And then internally if you see that this stage this stage it is coming in CC configuration on the other hand and this stage this stage it is in CE configuration. So, CE configuration for composite transistor resulting us CC followed by CE. So, likewise if you consider say the CC configuration, so now, let me consider CC configuration.

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**Multi-configuration amplifiers: Composite transistor**

Config.	$A_v$	$R_{in}$	$R_o$	$C_{in}$	$A_i$	Remarks
CE	High	High	High	High	High	Good Voltage amp & Current amp but needs suitable buffers (for cascading)
CC	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer and Power amplifier
CB	"High" with $R_s \neq 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and voltage gain booster

The diagram shows a composite transistor circuit with two transistors, Q1 and Q2. The base of Q1 is the input (i/p) and is connected to a bias current source (BIAS) and a capacitor (C1). The collector of Q1 is connected to the base of Q2. The emitter of Q2 is the output (o/p) and is connected to a capacitor (C2). The collector of Q2 is connected to the supply voltage (Vdd). Handwritten annotations include 'CC' in a circle, 'CC-CC', and 'Vdd' labels.

So, we can connect maybe a bias current here or maybe a resistor and let you call this is output since this is CC configuration the collector may be connected to supply directly. And at the base will be giving the signal may be directly or maybe through a capacitor with bias arrangement. But, whatever it is we do have the input coming to the base of Q 1 and output we are observing at the emitter of Q 2.

So, that makes the composite transistor in CC configuration and that results into say first stage it is CC configuration. And then the second stage is also in CC configuration, which means that if we connect the composite transistor in CC configuration we are eventually getting CC configuration. Now, how do we then analyze this circuit as I said that either you can consider the entire circuit and then analyze. And then may be the better way or smarter way what we can do the entire composite structure you can translate into single one.

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**Multi-configuration amplifiers: Composite transistor**

Config.	$A_v$	$R_{in}$	$R_o$	$C_{in}$	$A_i$	Remarks
CE	High	High	High	High	High	Good Voltage amp & Current amp but needs suitable buffers (for cascading)
CC	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer and Power amplifier
CB	"High" with $R_s \neq 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and voltage gain booster

*Small signal param...*

$\beta^{(c)}$   
 $r_{\pi}^{(c)} =$   
 $g_m^{(c)}$   
 $r_{\pi}^{(c)}$

So, if I say that entire circuit equivalently it is working as one transistor where the collector we call C superscript C, emitter it is E superscript C and then base is B superscript C. Then whenever we like to get see performance of the corresponding amplifier coming out of this composite transistor first thing we need small signal parameter. So, what are the small signal parameter? So, beta of the transistor then  $r_{\pi}$  collector to emitter resistance. Then trans conductance and then base to emitter resistor resistance  $r_{\pi}$ .

And just to consider this is this set is parameters of the composite transistor let you put the superscript C here for each of the parameter. Then we can find the expression of each of this parameter in terms of the internal and then parameters of the internal or constituent transistor namely Q 1 and Q 2. So, in the next slide we will be having that let us yeah.

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**Analysis of CC-CE and CC-CC amplifiers:  
Composite transistor (contd.)**

**Small signal Parameters:**

$$\beta^{(c)} = (1 + \beta_1)\beta_2$$

$$r_{\pi}^{(c)} = r_{\pi 1} + (1 + \beta_1)r_{\pi 2}$$

$$g_m^{(c)} = \frac{(1 + \beta_1)\beta_2}{r_{\pi 1} + (1 + \beta_1)r_{\pi 2}}$$

$$r_o^{(c)} = r_o 2$$

So, here we are in listing the small signal parameter and they are given in terms of the small signal parameter of the constituent transistor namely Q 1 and Q 2. So, how do you get that if you draw the small signal equivalent circuit of the entire circuit. So, say for Q 1 we do have say  $g_m$  into  $V_{be}$  of transistor 1, and then we do have the  $r_{\pi}$  of transistor 1. So, this node it is the base of the composite transistor.

Now, here this is connected to DC when you have, so this is connected to AC ground and we may or may not be considering this  $r_{\pi}$  of transistor 1. So, this is connected to AC ground and then the, so this is the model of Q 1 and then we do have the model of the Q 2. So, Q 2 we do have  $r_{\pi 2}$  and then we do have voltage dependent current source  $g_{m 2}$  multiplied by the  $V_{be 2}$ . And then we do have the  $r_o$  of transistor 2 and then finally, we do have the emitter terminal.

And this is the emitter of the not only  $Q_2$ , but the composite transistor. And here we do have the collector of  $Q_2$  which is also collector of the composite transistor. So, externally we do have these three terminals and then internally whatever the components are there. Now, if I call this entire structure as one transistor then we can translate this entire circuit into equivalent one transistor. And then whatever the voltage we do have here at  $V_C$  to  $V_E$  that is  $V_{be}$ . And then from the collector to emitter whatever the current is flowing that is  $g_m C$  multiplied by this  $V_{be}$ . And then collector to emitter whatever the resistance we do have that is called  $r_{O C}$ .

So, if I draw the equivalent circuit of the composite transistor. So, we do have  $g_m C$  multiplied by the corresponding  $V_{be}$  namely  $V_{be C}$  and then we do have  $r_{O C}$ . So, this is emitter and then we do have  $r_{pi}$  and this  $r_{pi}$  is  $r_{pi}$  of the composite transistor. So, here we do have base and then and you have the collector right. And if I compare see this equivalent circuit with the whatever the circuit is given here. Then first thing is that the resistance from the collector to emitter it is directly coming from this  $r_{O 2}$ .

So, that probably we can say that  $r_{O C}$  is equal to  $r_{O 2}$ , so that is the first thing and then, so this is very straightforward to get. Then next one it is if you see the beta of the transistor which means that the current gain current gain if I consider we do have some base current is flowing and then whatever the current is going flowing through the collector to emitter which is  $\beta C$  times this  $i_b$ . So, that gives the corresponding beta of the composite transistor.

Now, if I am having say  $i_b$  of the composite transistor flowing here  $i_b$ . So, that is eventually same as  $I_b$  of transistor 1. So, the current flowing through this emitter which is  $1 + \beta_1$  times this  $i_b$  and eventually that is that is giving us the base current of the second transistor. So, this current if I multiply with beta of the second transistor then I will be getting the  $i_c$ . So, this  $i_c$  it is  $1 + \beta_1$  times  $i_b$  times  $\beta_2$  and that is the  $i_c$ .

So, if I take this ratio of  $i_c C$  and  $i_b$  whatever we do have which is  $1 + \beta_1$  multiplied by  $\beta_2$  that is what the beta of the composite transistor. So, that is how we are getting the expression of the beta. So, now likewise if I see the base to emitter resistance let me use

different color yeah. So, to get the  $r_{\pi C}$  if you look into this circuit we do have  $r_{\pi 1}$  coming in series with this resistance, but then this resistance it is working as emitter de-generator for  $Q_1$ .

So, whatever the resistance we can see effect of this  $r_2$  it is it is  $1 + \beta$  times of transistor  $1$  multiplied by  $r_{\pi 2}$ . So, the impedance at the base  $2$  with respect to its emitter it is  $r_{\pi 1}$  in series with  $1 + \beta$  times  $r_{\pi 2}$ . So, that is why we do have  $r_{\pi C}$  equals to  $r_{\pi 1} + 1 + \beta$  times  $r_{\pi 2}$ . Now, this part of course, it is not really playing any role to define  $r_{\pi C}$ . And once we have this  $r_{\pi C}$  next thing it is getting the  $g_m$  just we have to take ratio of the  $2$ .

So, if I take a ratio of the  $2$  then we are we are getting the corresponding  $g_m$ . In fact, the  $g_m$  you can get it through different approach also you will be converging to this only ah. So, how do you get the  $g_m$  alternatively if I consider this is the  $V_{be}$  entire  $V_{be}$  it is from here to here. And part of it is appearing here as  $V_{be 2}$  and this  $V_{be 2}$  after multiplying with  $g_{m 2}$  it gives the collector current.

So, effectively I can say that the  $g_{m C}$  this  $g_{m C}$  it is essentially  $g_{m 2}$  multiplied by whatever the fraction of the  $V_{be C}$  coming as  $V_{be 2}$ . And what is this fraction? We do have a an impedance here and also we do have an impedance here and this impedance is  $r_{\pi 2}$ . And the, so the and the impedance here if you see this part ignoring this part that you can ignore. So, we can say that some and that impedance is  $r_{\pi 1}$  in parallel with  $1 + \beta$ .

So, the fraction we are getting here it is  $r_{\pi 2}$  divided by this resistance plus  $r_{\pi 2}$ . In fact, if you simplify it if you simplify it you will get the same expression here ok. So, anyway, so what you can say that from this equation we can say that  $g_{m C}$  it is slightly smaller than  $g_{m 2}$  I should say it is slightly if you see the equation. And most important thing is that this resistance is got increased and also the  $\beta$  of the transistor it is basically product of  $\beta$  of the  $2$  transistors.

So, I should say the main advantage of going for this composite structure is basically improving the  $\beta$  and then increasing the resistance while maintaining the  $g_m$  almost the



same and maintaining the  $r_{\pi}$  almost the same. So, that is how we can probably you can consider the you can get the small signal parameter and then utilizing that those small signal parameter you can find the gain of C and C C.

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**Analysis of CC-CE and CC-CC amplifiers:**  
**Composite transistor (contd.)**

**Small signal Parameters:**

$$\beta^{(c)} = (1 + \beta_1)\beta_2 \quad r_o^{(c)} = r_{o2}$$

$$r_{\pi}^{(c)} = r_{\pi1} + (1 + \beta_1)r_{\pi2}$$

$$g_m^{(c)} = \frac{(1 + \beta_1)\beta_2}{r_{\pi1} + (1 + \beta_1)r_{\pi2}} \approx g_{m2}$$

$$A_v = -g_{m2} R_c \parallel r_{o2} \approx -g_{m2} (R_c \parallel r_{o2})$$

$$R_{in} = R_B \parallel r_{\pi}^{(c)} = ?$$

$$R_o = R_c \parallel r_{o2} = R_c \parallel r_{o2}$$

So, in the next slide probably we can discuss that yeah. So, let we let you go one by one, so let you consider say CC CE stage which means that this composite structure we can connect in CE configuration. So, to make this circuit in CE configuration let we connect R C at here and then to the supply. And the emitter we can make it to ground and then at the base we can put a bias resistor called R B connected to V dd and then you can feed the signal.

So, that gives us the internally that gives us a CC CE circuit, so we call this is the output. Now, we know that the circuit it is actually this composite structure it is in, so this is whole transistor it is in CE configuration. And for CE configuration what are the expressions of the

different parameters or the and the voltage gain namely which is  $g_m$  multiplied by  $R_C$  in parallel with  $r_{out}$ . And with  $g_m$  now we have to consider we have to consider  $g_m C g_m$  of the composite transistor.

So, likewise  $R_C$  anyway it is external, so likewise  $r_{out}$  it should be  $r_{out}$  of the composite transistor. So, now we do have the expression of the  $r_{out} C$  which is  $r_{out}$  of transistor 2 and then we do have the expression of  $g_m C$ . So, this it can be well approximated by say  $g_m 2$ , so I should say it is  $g_m 2$  multiplied by  $R_C$  in parallel with  $r_{O2}$ . In fact, this is very much of course, with a minus sign here I sorry I forgot that there is no surprise if you see this circuit the primarily what we obtain the voltage gain we are getting from the second stage the coming from the  $Q_2$ . And  $Q_1$  since it is connected in CC configuration its voltage gain it is approximately 1.

So, that is how we can directly get the voltage gain. Now, the input impedance on the other hand, so for CE configuration input impedance is  $R_B$  in parallel with  $r_{pi}$ . And in this case which  $r_{pi}$  this should be  $r_{pi}$  of the composite transistor and expression of the  $r_{pi}$  it is given here ok.

So, that is the expression of the  $r_{pi} C$ , so you can get its value and likewise ha output  $R_O$  it is a output resistance  $R_O$  it is  $R_C$  in parallel with  $R_O$  of the composite transistor and eventually this is same as  $R_{O2}$ . So, we can say that this is  $R_C$  in parallel with  $r_{O2}$ . So, that is how we can get the performance expression the namely the output voltage and sorry output resistance and input resistance and the voltage gain of the CC CE configuration.

So, likewise if you connect the circuit in CC configuration you can find the corresponding the voltage gain, input resistance, and output resistance. So, let us see how we are getting it or probably you can try yourself and you can connect the circuit in CC configuration.

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**Analysis of CC-CE and CC-CC amplifiers:  
Composite transistor (contd.)**

**Small signal Parameters:**

$$\beta^{(c)} = (1 + \beta_1)\beta_2 \quad r_o^{(c)} = r_o$$

$$r_{\pi}^{(c)} = r_{\pi 1} + (1 + \beta_1)r_{\pi 2}$$

$$g_m^{(c)} = \frac{(1 + \beta_1)\beta_2}{r_{\pi 1} + (1 + \beta_1)r_{\pi 2}}$$

$$R_o \approx \frac{1}{g_m^{(c)}} \approx \frac{1}{g_{m2}}$$

*Handwritten notes on the slide:*  
 $A_v \approx 1$   
 $R_{in} = R_B \parallel (r_{\pi 1} + (1 + \beta_1)r_{\pi 2})$   
*output*

So, to connect the circuit in CC configuration you can directly connect these to Vdd you can probably connect a bias circuit here bias current source. And then this is the output port and then we can connect a bias circuit here R B and then you can feed the signal here at the base of the composite transistor. And we know the voltage gain it is approximately 1 and then input resistance.

So, in case if we have some R L connected here, then the input resistance of the composite structure it is R B in parallel with whatever the resistance we do have which is  $r_{\pi}$  of the composite transistor. In series with 1 plus beta of the composite transistor multiplied by R L.

Now, again we do have the expression of  $r_{\pi C}$  and then beta C it is given here, so from that you can find the expression of the input resistance. It may be observed that from this part impedance of this part it is in fact, it is quite high. And in presence of this R B of course, this

R B it may be dominating that. So, if you are constructing this circuit with this R B you may not be really seeing much change, but internally the circuit input resistance it is quite high.

So, on the other hand output resistance R O we can approximate this by  $1/g_m$  and this is  $1/g_m C$  and this is given by  $1/g_m^2$  ok, so I should say this is approximation ok. So, that is how we can analyze the CC CE and CC CC configuration using composite transistor concept.

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**Multi-figuration amplifiers: Darlington pair and CC-CE**

Config.	$A_v$	$R_{in}$	$R_o$	$C_{in}$	$A_I$	Remarks
CE	High	High	High	High	High	Good Voltage amp & Current amp but needs suitable buffers (for cascading)
CC	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer and Power amplifier
CB	"High" with $R_s \approx 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and voltage gain booster

Op-amp

cc-ee

Now, let us move to MOS Tran MOS based circuit in fact, sorry before we go to the MOS circuit we do have one more information to we like to share.

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**Summary of Performance metrics of CS, CD, CG configs.**

Config.	$A_v$	$R_{in}$	$R_o$	$C_{in}$	$A_i$	Remarks
CS	High	V. High	High	High	High	Good Voltage amp but needs suitable buffer (for cascading)
CD	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer
CG	"High" with $R_s \approx 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and voltage gain booster

CS-CD  
CE-CC

Ah We have talked about the CC CE stage sorry, we have talked about CC CE stage. And, so if I if I consider this composite structure and then if I connect this transistor in CE configuration then we are getting basically the CC CE configuration. And what is its main advantage the input resistance it becomes quite high.

Instead of instead of connecting the circuit in this way there is a smarter way where instead of connecting this Q 1 collector of Q 1 to V dd even if you are connecting this to the output then also we can get the input resistance it is quite high. So, that connection whatever the connection just now we are showing that gives us different configuration it is referred as Darlington pair.

So, this Darlington pair I should say it is kind of modified version of CC CE stage, why I am I am sharing this information? Because this Darlington pair it is frequently used for operational

amplifier later we will discuss which is commonly known as op amp. To increase the input resistance of the input resistance of the op amp.

So, you may be surprised that then why we do have a special kind of configuration why not CC CE configuration. As I said that it is it is on principle they are both the configurations are same except this connection. So, I should say this is this kind of modification it gives us the Darlington pair.

Now, let us move to the MOS circuit. Similar to BJT based different basic configuration we can we can also summarize the performance matrices of the common source, common drain, and common gate, configuration coming out of MOS transistor. So, these are the three basic configurations and for each of these configurations we do have we have been listed qualitatively we have been listed different performance matrices.

Namely voltage gain, input resistance, output resistance, input capacitance, and then current gain. So, here again it is I should say most of the information it is very similar to whatever we have seen for BJT. Except this CC stage its input resistance it is very high, as you know that gate to gate to source connection it is through insulator. So, we can see that it is almost infinite theoretically.

So, and that is the only difference as a result we may not be requiring any special circuit to increase the input resistance of the CC's CS stage. But, then to decrease the output resistance of CS stage we can use the common drain amplifier to decrease the output resistance. Mainly, because if you see here the common source amplifier it is it is a very good voltage mode amplifier.

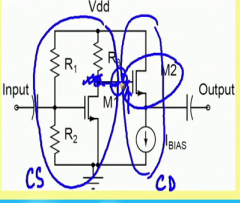
But, main concern is that its output resistance is high and of course, its input capacitance is also high. And this problem the output resistance since it is high that can be avoided or rather that can be you know managed by using common drain stays cascaded with that. So, we can say that common source we can connect with common drain to get a better or I should say lower output resistance.

In fact, that also helps to improve the input capacitance later we will see that. But, so we should say that this configuration it is very similar to whatever the common emitter followed by CC stage. So, in the next slide we will be just summarizing its performance, particularly the common source followed by common drain amplifier yeah.

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**CS-CD configuration**

Config.	Av	Rin	Ro	Cin	AI	Remarks
CS	High	V. High	High	High	High	Good Voltage amp but needs suitable buffer (for cascading )
CD	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer
CG	"High" with $R_s \neq 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and voltage gain booster



The diagram illustrates a CS-CD configuration. It features two MOSFETs, M1 and M2. M1 is configured as a common source amplifier, with its gate connected to the input and its source connected to ground. M2 is configured as a common drain amplifier, with its gate connected to the drain of M1 and its source connected to ground. The output is taken from the drain of M2. A biasing network with resistors R1, R2, and R3 is connected to the gates of M1 and M2. A bias current source is connected to the source of M1. The circuit is powered by Vdd.

So, here we do have the common source. So, we do have the common source amplifier followed by common drain stage. Note that the drain the next stage next stage the second transistor gate it is directly connected to the drain of transistor one. That is because it is very convenient and not only that it first of all we do not require any capacitance here.

Second thing is if you are putting a capacitor here then you need to have separate bias at the gate. And but then whatever the DC voltage it is available at the gate of transistor 1 that may be a sufficient to bias the second transistor and hence it is directly getting sorted.

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**CS-CD configuration**

Config.	Av	Rin	Ro	Cin	AI	Remarks
<b>CS</b>	High	V. High	High	High	High	Good Voltage amp but needs suitable <u>buffer</u> (for cascading)
<b>CD</b>	V. Low	V. High	V. Low	V. Low	High	Voltage mode buffer
<b>CG</b>	"High" with $R_s = 0$	V. Low	V. High	V. Low	V. Low	Current mode buffer and <u>voltage gain booster</u>

$R_{in} = R_1 || R_2$ ,  $A_v = -g_{m1}(R_3 || r_{o1}) \times 1$   
 $R_o \approx \frac{1}{g_{m2}}$   
~~CS-CG~~ MOS  
~~CE-CB~~ BJT

So, this CC rather CS CD amplifier if you see its main advantage it is that the output resistance. So, output impedance it is I should say  $1/g_m$  of the second transistor, and input resistance of course, here we do not have any the rather this input resistance is infinite. So,  $R_{in}$  it is eventually coming from the bias circuit only  $R_1$  in parallel with  $R_2$ .

And then we do have of course, the voltage gain which is coming from the CS stage and that is  $g_m$  of transistor 1 multiplied by  $R_3$  in parallel with  $r_o$  of transistor 1. And this stage the second stage of course, its gain it is approximately 1, so its voltage gain it is essentially coming from the first stage yeah. So, this mixing of the two configurations it is primarily to get the



lower output impedance. In fact, we will we can also have similar kind of mixing namely the CS and CG as I said that CS and CE they are the heart of the amplifier.

And then to have connection with other circuit we need to take help from buffer ah. So, so we will be we are in this case we are taking help from common drain to get to reduce the lower to reduce the output resistance. Likewise, if the common source stage it is cascaded with common gate we will be getting some other advantage particularly that helps to boost the gain.

So, that configuration we can say that common source followed by common gate for this is for MOS family. And likewise common emitter followed by common base which is for the BJT family. And both of these two circuits their purpose is primarily to increase the gain of whatever the gain of the common source or common emitter amplifier we do have. So, that topic of course, that is also multi configuration mixing multi configuration that will be discussed in the next class.

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**Conclusion:**

- ❑ Motivation of mixing different configurations
- ❑ Decreasing output impedance by cascading CC:
  - CE-CC
  - CC-CC
- ❑ Increasing input impedance by preceding CC stage:
  - CC-CC
  - CC-CE
  - Darlington pair

MOS: CS-CC, BJT: CE-CD
- ❑ Decreasing output impedance by cascading CD:
  - CS-CD
  - CD-CE

MOS: CD-CE, BJT: CE-CD
- ❑ Yet to cover Numerical example

So, let me then summarize whatever we have discussed today in 3 parts of this lecture today. It is first we have started with motivation of mixing different configuration and then, we have discussed about utilizing the yeah utilizing the CC stage to decrease the output impedance. And that is done for both cases CE followed by CC and then CC followed by CC for both the cases output impedance it has been decreased.

Then we also have discussed how to use the CC stage common collector stage to increase the input impedance. So, here we are the first CC stage it is helping to increase the impedance of the main one. So, either it may be CC or CE and then also we have discussed about something called a special configuration Darlington pair which is quite popular. But, that is I should say on principle it is same as CC followed by CE. And then also we have just now we are talking about for the decreasing output impedance using the common drain amplifier for MOS family.

So, if we have say a common source amplifier we can cascade with that common drain and that gives us a lower output impedance. In fact, here these two and then here all are pure BJT on the other hand this is pure MOS circuit. There is a possibility of mixing the MOS and BJT to make the multi transistor configuration. And, so see for example, if we have C common source amplifier we can connect this common source amplifier with common collector.

So, this is this is MOS, so this is MOS transistor based and then this is on the other hand BJT right. And the purpose it is seen by now I think you will be able to correctly guess that CC stage it helps to reduce the output resistance. So, likewise we can connect same CE stage preceded by or may be followed by common drain to get the. So, this is this is BJT and this is MOS and like that it can have common emitter preceded with common drain amplifier.

So, if we do this the input impedance it will be increased by this common drain. So, that is how we can mix the BJT configuration along with MOS configuration, provided the situation helps you to do so. We as I said that we had to cover numerical examples either in the next class or next to next class we will be talking about depending on the situation. I think that is all we need to cover today.

Thank you for listening.