Analog Electronic Circuits
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Lecture – 56
Multi-Transistor Amplifiers: Operation and Analysis (Part B)

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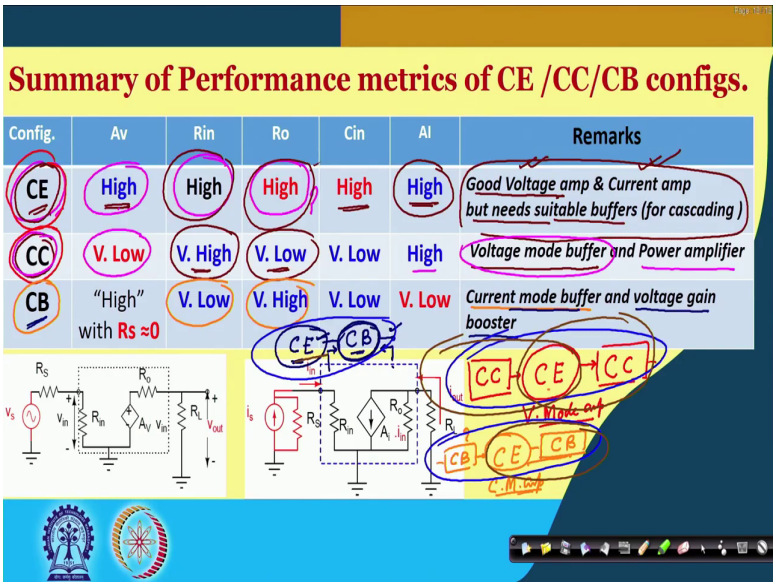

So, we are talking about this different possible configurations meaningful configuration and let we go one by one how they are helping us to improve the performance.

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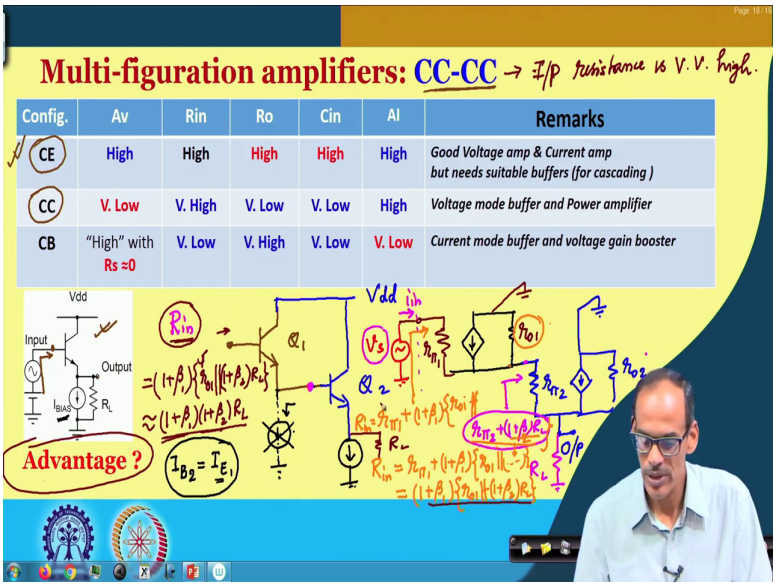

So, in the next slide we will be mixing CE and CC. So, for our reference so, we do have the main table we are keeping it here and we will see that how the CE and CC will be helping us to improve the performance to start with let you consider CC and CCs together and then probably we will see the CE and CC.

So, we do have the basic CC configuration and its main characteristic or main rather from requirement is that input is at the base and output is at the collector. So, if I consider say one transistor we do have see input here feeding at the base of this transistor and let me call this is Q 1 and then it is output it is going to the second transistor. So, we do have the second transistor here and let you call this is Q 2 and of course, the collector here and collector here they should be connected to the main supply, better be connected to main supply.

In fact, we can have some resistance also connected there, but for ideal condition we want that and if you see they are bias conditions. So, I mean think of that it is having a DC current here as we can see here and we may or may not require this DC current depending on the level of the current of the Q 1 and Q 2. So, if I say that if we do not have any bias current here which means that the base current of the second strength transistor it is same as the emitter current of the first transistor. If this is getting satisfied then we do not require.

Otherwise the additional current; additional current of the emitter in case if it is a emitter current of the transistor 1 it is higher than the required base current of the second transistor then we may required this bias circuit. So, that is why I am just putting a dotted line. So, depending on the situation we may or may not consider, but whatever the situation it is small signal wise you may say that for ideal current source here we may think of this is open.

So, if I draw this small signal equivalent circuit and if we are feeding the signal directly to the base to base of the second transistor, then we can draw the small signal model of the first transistor and then followed by the second transistor. Let me use that blue color just for consistency of the other diagram.

So, this is the small signal model of the second transistor Q 2 and this node it is connected to DC voltage which is AC ground and this is also AC ground and of course, we do have the input port. So, we may see that the input signal we are feeding here. So, this is the input signal V s.

Now, if you see that different parameter of the individual transistor we do have r pi 1 and then we do have r o 1 likewise for the second transistor we do have r pi 2 and then r o 2 and this is the output node. So, primary output port it is given here. Now, what we are looking for it is basically two things – one is the increasing the input resistance and also it is we are expecting that this will decreasing output resistance. So, let us see how this configuration on this kind of mixing it is helping to get higher input resistance.

So, R in if I consider to get the R in of course, we can whole circuit, we can analyze we can find what is the corresponding input current going there. And, then if you take the ratio of this Vs and then this i in so, from that you can say what is the expression. Better approach or qualitative approach it is something like this.

Suppose, if you consider the input resistance of the second stage depending on whatever the load we do have here say R L, so, we may say that this resistance looking into the base of transistor 2 it is r pi 2 plus 1 plus beta into R L we can ignore this one and so, that is the resistance.

Now, on the other hand, if you are coming to the primary input port and if you try to see what is the corresponding input resistance you can see that we do have r pi 1 plus beta of the first transistor 1 plus beta 1, it is amplifying whatever the impedance you do have. So, even if you are you may consider this one or you can ignore that, but whatever it is. So, 1 plus beta 1 it is multiplying this r o 1 plus whatever the resistance you already have obtained here. So, in summary so that is in fact, the input resistance of the entire circuit. So, in summary what we can say of course, this beta it is a second transistor beta so, we should write beta 2.

To summarize this input resistance it is r pi 1 plus 1 plus beta 1 into ok. So, this should not be plus it should be rather in parallel with whatever you do have. So, that is r o 1 in parallel with this part. And, if you consider the dominant terms of course, this will be dominating 1 plus beta 1 multiplied by r o 1 in parallel with this one 1 plus beta 2 into R L ok. So, if it is very clumsily for you I am writing the expression here the final expression 1 plus beta 1 multiplied by r o 1 in parallel with 1 plus beta 2 into R L.

In fact, if you ignore this part what you can say here it is 1 plus beta 1 and then 1 plus beta 2 multiplied by R L which means that whatever the load resistance we are connecting here R L to the circuit that is seen by the input signal source through this amplification of the impedance of each of the stages namely 1 plus beta 1, 1 plus beta 2 are getting amplified. As a result you can get really high very high input impedance. So, the purpose of CC stage first one it is input impedance. So, the advantage rather, we are writing here.

So, the advantage here it is the input resistance. So, input resistance is very high very very high. On the other hand, if you see the output resistance and we are looking for this output resistance would be as small as possible. So, if you see ok. So, let me clear otherwise I am not be able to explain to you.

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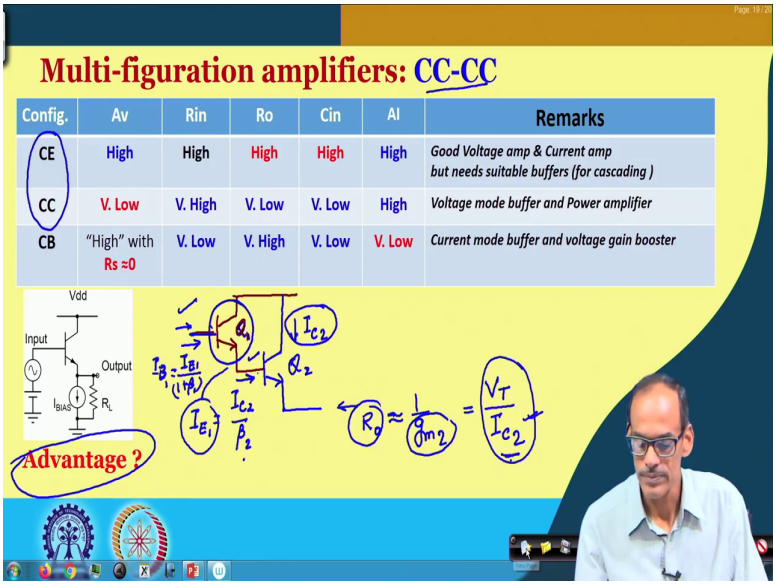

So, the same configuration namely CC followed by CC. So, we do have the CC followed by CC and so, we do have the Q 1 here, we do have the Q 2 here and this is connected to V dd. The output impedance so, we know that this will be in the order of 1 by g m and in this case g m of the second transistor. So, now, the g m of course, it is function of the current ah. So, we do have g m is equal to I C divided by V T or rather one by g m it is V T divided by I C of the second transistor.

And, in this case if you see that of course, it depends on the current. So, higher the value of this current then we can have better situation namely smaller output resistance, but then to support this current in case if you are loading the primary port then it may be a problem.

But, then since we do have the second transistor here to support this high value of I C 2 we require a smaller version of this same current namely I C divided by beta of the second transistor which is eventually this is equal to I E of the first transistor and to support this we require a base current here which is very small namely I E 1. So, I B equals to this I E 1 divided by 1 plus beta.

So, to support this large current we require here it is the required base current is very small. So, this base current it is coming here after this amplification of 1 plus beta 1 of the transistor 1 and then we do have this beta 2 coming from the second transistor. So, what we are getting here it is the again the output resistance because this I C we can support very high value and then you can see that the output resistance of CC – CC stage it is very very low ok. So, that is what that is the advantage of having CC followed by CC.

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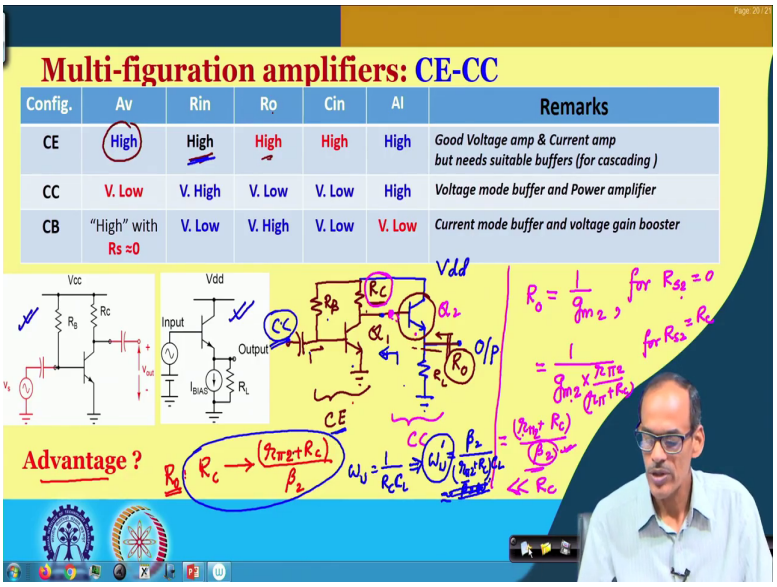

Now, let us see the other configuration namely CE and CC. So, mixing across different configuration. So, we do have the CE stage circuit here CE configuration and then also we do have the CC configuration, and let us see how they can be mixed together to get the combined circuit. So, we do have the first transistor see we do have Q 1 here and its corresponding R C. For simplicity I am not putting any emitter degenerator, we are using fixed bias configuration and then we are feeding the signal here.

And, then this output it is going to the CC stage so, that means, different colored here. So, we do have the CC stage and the collector it is connected to the supply and then we may have the corresponding bias circuit or and or the load resistance here. So, this is the primary output port. So, as we have seen that the CE stage CE stage it is providing good voltage gain and

also it is having decent amount of input resistance and but then output resistance it is high namely it is dominated by R C.

But, then if we simply cascade it with CC so, we are anticipating that the resistance coming to the output port without considering this R L if I consider only up to this one and if I see what is the output resistance. We are expecting that this output resistance final output resistance it should be much smaller than this one. So, what is the output resistance?

You may recall. So, this is CC stage. So, naturally its output resistance expression we are expecting it will be 1 by g m on this transistor. Assuming that whatever the circuit we do have here it is resistance is 0, but. So, this is true if the resistance of the signal source is 0.

So, if I say that corresponding R S is equal to 0, but if it is not; if it is not then 1 by g m 2 as we have discussed earlier this g m 2 it will be getting attenuated by r pi here and whatever the R S will be having and incidentally R S is inter close to R C. So, I should say for R S 2 equals to R C what we have here it is r pi divided by r pi plus R C right.

In fact, you can further simplify this expression which is r pi plus R C divided by g m 2 multiplied by r pi 2 which is beta of the transistor beta 2. So, you may say that since this R C it is getting divided by beta 2, even though we do have the r pi of the second transistor coming in series, but since it is getting divided by beta 2 this is much lower than. So, I should say this is much much lower than R C.

So, what is the conclusion? The main advantage here it is if I am having only CE the R out it was R C that is getting changed to r pi 2 plus R C divided by beta of the second transistor right. So, that makes much smaller and that is useful for the connecting a load. In fact, the not only it is just making the output resistance getting smaller and concluding in that form we can further go and say that what is it is main advantage and motive. By this if the upper cutoff frequency earlier it was decided by see R C with R C L, in case if you are connecting a load capacitance directly there without considering CC stage then the upper cutoff frequency it was like this.

Now, this upper cutoff frequency it is getting changed to 1 by whatever the new output resistance we do have r pi 2 plus R C multiplied by C L and then beta 2. So, approximately if I drop this part for just for qualitative comparison we can say that this is beta 2 times whatever earlier upper cutoff frequency we are having. So, this is the modified one if I say dash and this is the original one. So, we can see that the bandwidth of the circuit bandwidth of the amplifier it is getting extended.

Now, so, that takes care of the output port, similar kind of things it can be done for the input port also namely, if I precede this CE stage by CC stage then we can get the enhancement of the input resistance. So, in case even though whatever the input resistance, so, we do have namely R B and r pi if we are not really happy with that and if you want to further increase it then we can do that we can mix this CC configuration before the CE stage.

So, in the next slide what we are going to do we will be having CC followed by CE.

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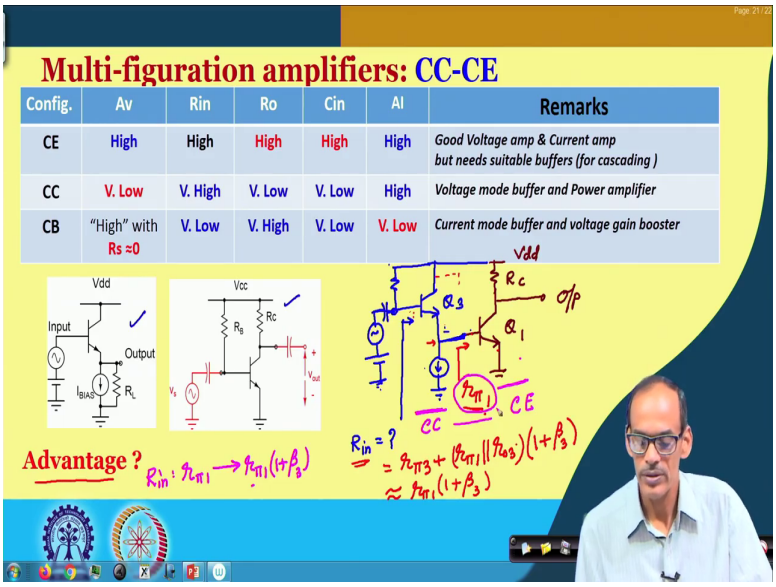

So, here again we do have the individual stages and if we mix them together the circuit configuration we will be getting is the main transistor CE main transistor it is in CE configuration. So, we do have the R C and then let me call this is Q 1 supply we do have the V dd and this is the output port and then we do have the; so, let me call this is Q 3 connected to V dd and so, this is the CC stage and the input we are directly putting here. So, either we may have the bias circuit here or depending on the situation we may put signal with a meaningful DC.

So, of course, if I put bias circuit on the other hand we can put a DC blocking capacitor and then we can feed the signal whatever it is and then of course, in case the emitter current here it is entire emitter current DC current if it is not necessary for the base of the main transistor Q 1, then you may put a current sync path. So, the excess current it will be going here, the other

part the base current it will be go into Q 1. So, whatever it is the input resistance of this circuit small signal input resistance that is our primary interest what is the corresponding expression.

So, if you see the circuit here the impedance coming from the Q 1 at the emitter of Q 3 it is we do have the r pi here. So, we can say that we do have the r pi 1 and then whatever the impedance will be seeing here it is this r pi 1 and then of course, we do have r naught. So, that r naught we can ignore.

So, we can say that at this node we do have essentially r pi 1 and then input resistance at this point it will be r pi 3 of coming from transistor 3 plus r pi 1 in parallel with whatever r o 3 though as I said you may ignore which is getting multiplied by 1 plus beta of transistor 3. So, you can approximate this by saying that this is r pi 1 multiplied by 1 plus beta 3.

So, what is the advantage we are getting here that input resistance this input resistance initially for this stage it was r pi 1 that got enhanced or increased to r pi 1 multiplied by 1 plus beta 3. In fact, this is very common technique it is used for op-amp, we can put this additional transistor here which enhances the input resistance and this is important for BJT circuit for moss we know that gate resistance is very high.

So, such kind of enhancement it is not required for moss configuration. But, for BJT since r pi it is not very high we may require the CC stage to be used to precede with CE stage. So, we do have this CE stage input resistance it is getting enhanced by the CC stage. So, that is the advantage. So, likewise we can go for the other configuration.

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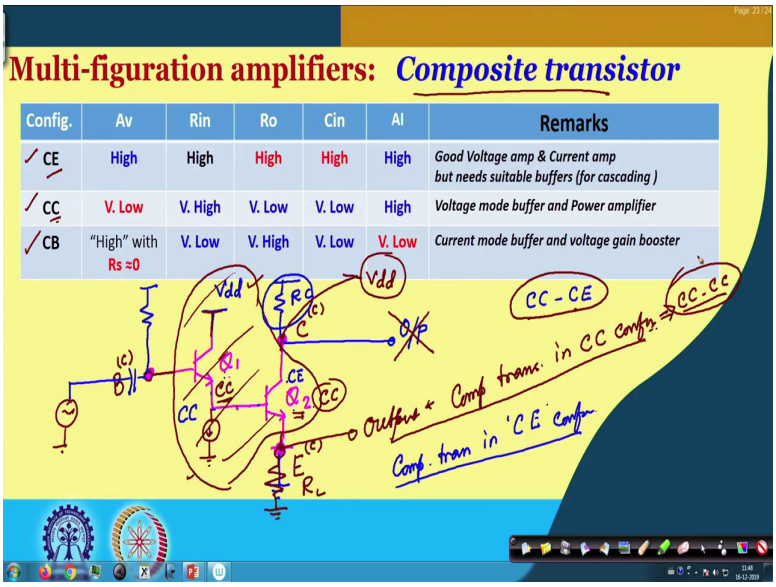

Let me see what are the other configuration I do have.

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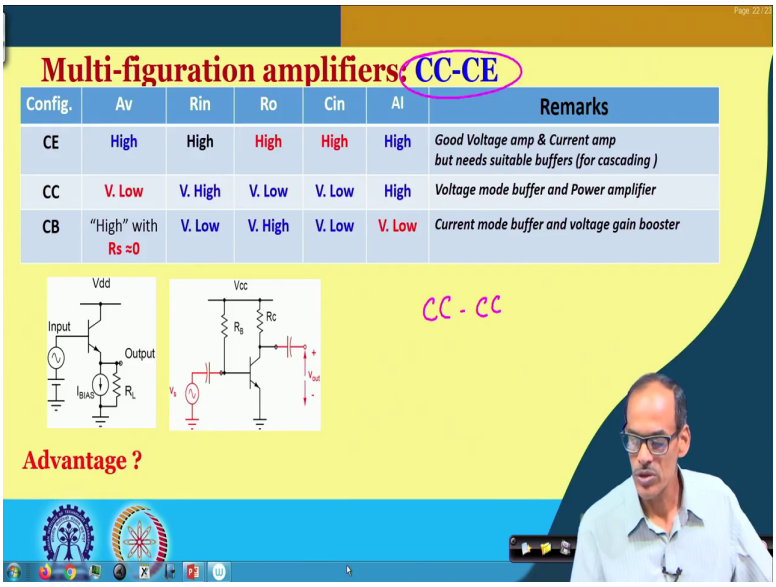

So, before I go to this composite configuration I must say that so far. So, we are talking about CC and CE, we also talk about talked about the CC and CC. So, is there any better way of analyzing this kind of circuit? Just I like to give a little notion of that now we do have the next discussion something called composite transistor.

So, let us see what does it mean. Suppose, we do have see one transistor in general say Q 1 and then we do have another transistor say Q 2. So, whether it is CE – CC or CC – CC this kind of configuration we had seen and see emitter of Q 1 it is directly internally getting connected to the transistor 2.

And, as an user or as a the complete circuit designer we may not be much interested of accessing this node, instead we like to access this node to feed the signal probably or we like

to access a this node to observe the signal and or to access this node. And, at the same time we like to keep the collector of the first transistor to a meaningful voltage called say V dd.

So, if we see this configuration then of course, whenever we do have the emitter current of Q 1 coming here either the entire emitter current need to be consumed by base terminal of Q 2 or we should be having some bias bypassing arrangement here. So, I should say if I am having say this bias V dd and this one then whole thing so, if these two bias is properly arranged then whole thing it can be clubbed together and it can be consider one single transistor where you may call this is the base terminal, this is the collector terminal sorry this is collector terminal and this is the emitter terminal.

Now, incidentally the collector and emitter terminal of Q 2 it is coinciding with this, but then base terminal of Q 2 it is not visible to us or user; on the other hand, base terminal of Q 1 it is defining the base terminal of the transistor or the complete transistor. So, we may call this as composite transistor and if we consider this is composite transistor for one transistor we already have seen that three possible configurations are available.

Now, if I call this is base of the composite transistor and if we denote by B subscript C this is collector of the composite transistor denoted by C subscript superscript C so, likewise emitter superscript C. Now, can I use this entire composite transistor in different configuration? So, let us see suppose if I connect the circuit in say CE configuration.

So, what do I have to do? Let me use some color let me blue color. So, for CE configuration what I have to do I need to put a bias here and then I need to put the signal here and then I need to put some bias circuit here through R C and the emitter we can connect to ground and we call this is the output node. So, what we have done here it is composite transistor in CE configuration.

Now, if I put this in CE configuration internally what we have obtained here it is actually this is CC stage and this is CE stage. So, we can say that if the composite transistor it is in CE

configuration which is making CC followed by CE. So, likewise, if I put the composite circuit or composite transistor in say CC configuration; so, for CC configuration what I have to do?.

I have to rather instead of connecting this to ground then the supply I should connect to rather directly to V dd and instead of calling this as output we will put a resistance here and then we call this is output and then of course, we will be feeding the signal here.

So, now we obtain by this connection by this connection and this resistance here call R L we got composite transistor in CC configuration, but then internally if you see that this is anyway it is CC. So, Q 1 it is in CC and then Q 2 it is also CC. So, in other words, if the composite transistor it is in CC configuration eventually we are getting CC – CC configuration.

So, likewise this composite transistor can be connected. So, in different configuration and the analysis can be whatever the analysis we have done for CE and CC configuration that can be utilized to get the overall performance of the CC – CE or CC – CC configuration ok.

We will continue this one, but let me take a break and then we will get back to it.

Thank you.