Analog Electronic Circuits
Prof. Pradip Mandal
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture- 49
Common Base and Common Gate Amplifiers: Analysis (Part A)

Yeah. Dear students we will come back to NPTEL online certification course on Analog Electronic Circuits. Myself Pradip Mandal from E and EC department of IIT Kharagpur. So, this is continuation of this course and today's topic of discussion it is Common Base and Common Gate Amplifiers.

(Refer Slide Time: 00:55)

So, based on our overall plan let us see what is our situation now it we are in week 5 and we are in the building blocks of analog circuits. And in week 5 we have completed common collector and common drain.

Today we are going to discuss about the common base and common gate amplifiers. Under that we will be discussing about basic operation biasing, analysis and design and numerical examples will be covered will be covering later in the next class. So, whatever the concepts we are planning to cover today it is the following.

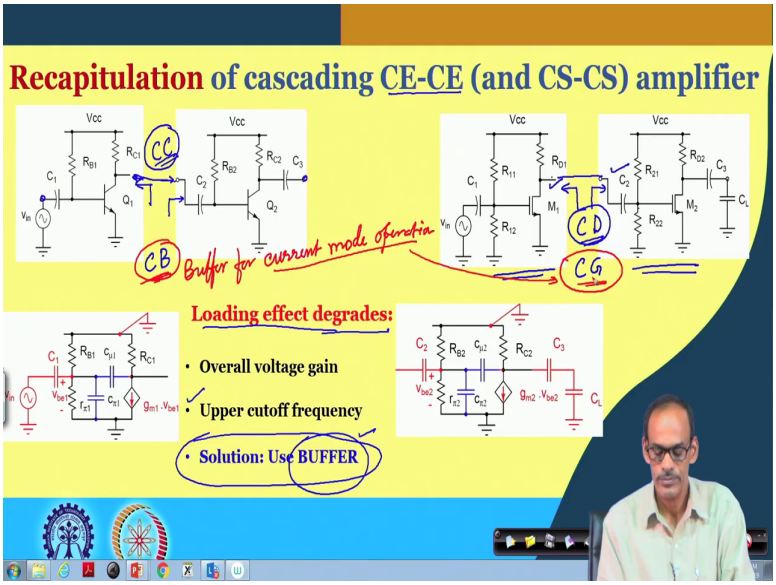
(Refer Slide Time: 01:38)

We shall start with the motivation of going for this new configuration called common base and common gate amplifiers specifically for BJT and MOS based amplifiers.

Then we will be talking about the basic operation of these two configurations. In fact, common base and common gate they are I should say similar kind of configuration common base is used in BJT and on the other hand common gate it is MOSFET transistors. So, after the basic operation we will be going for a biasing of these two configurations; then we will go a little detail of small signal analysis to find the following important performance matrices; namely the voltage gain, input impedance, output impedance. And then we will also see the current gain.

Now, coming to the motivation of these two new configurations; as we have discussed already about the common emitter and common source amplifier followed by common collector and then common drain. Now, we are entering into the third configurations. So, let us see what is the basic motivation as I said.

(Refer Slide Time: 03:31)



So, this is it is again recapitulation over whatever we have discussed before. To start with the motivation, you may recall that common emitter and common emitter cascaded it is having some cascading effect. Namely, the output impedance of the previous stage and the input impedance of the subsequent stages they are creating you know potential division.

As a result we already have seen that due to this interaction what you call it is loading effect. Due to the loading effect it degrades the overall gain starting from the primary input to primary output if you directly connect this one, it also effects the upper cutoff frequency or the bandwidth of the circuit.

Mainly because the output impedance of the previous stage and then input capacitance of the subsequent stage they are forming a pole. So, as a result this additional pole it may restrict the bandwidth of the amplifier. So, what we have seen in the previous class particularly for common collector configuration. What we said that if you put a common collector stage here it helps to improve the circuit performance. In fact, it is similar for the MOS counterpart namely if we have two common collector sorry common source amplifier cascaded together.

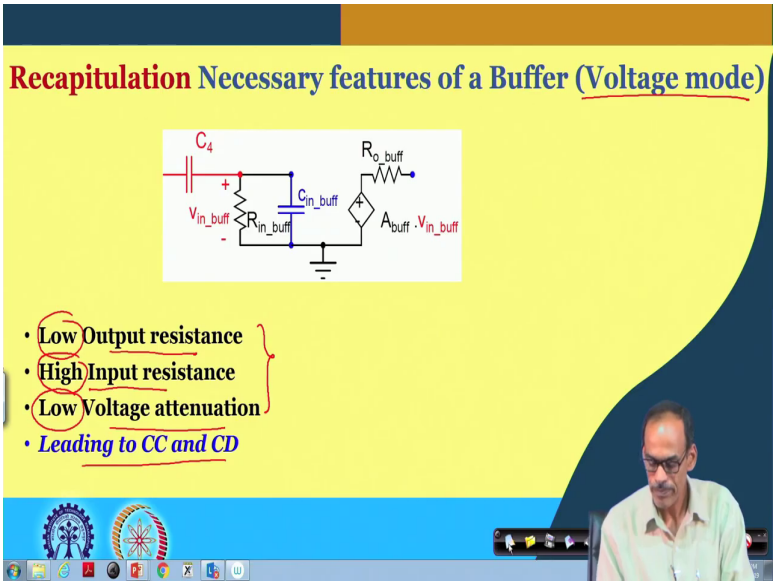
Here also the loading effect at this point namely the output impedance of the first stage and the input capacitance of the second stage. In fact, input impedance also they are creating the loading effect. And again here also the solution it is we have to put a buffer and for MOS based circuit or buffer it is common drain and here we say it common collector. And in these two cases what we have seen here it is the signal here it is in the form of voltage. So, I should say for voltage mode of operation the buffered implementation it is either it is done by common collector or common drain.

So, likewise if the signal if we consider here it is in the form of current, then also we will be seeing that there will be some performance degradation; to overcome the performance degradation we may require a buffer suitable buffer which is current mode buffer. So, coming to what may be the implementation of the current mode buffer, it is for BJT it is common base and for MOS it is common gate. So, I should say that these two circuits namely the only

common base this is working as buffer, buffer for current mode operation and. So, this is buffer for BJT and this is for the mas based.

So, both the common base and common gate essential requirement is it is working as a buffer. So, let us see what is the basic property we are looking out of this current mode buffer or buffered in current mode operation, whether you know the common base and common gate the configurations are they suitable for those requirements that we will see.

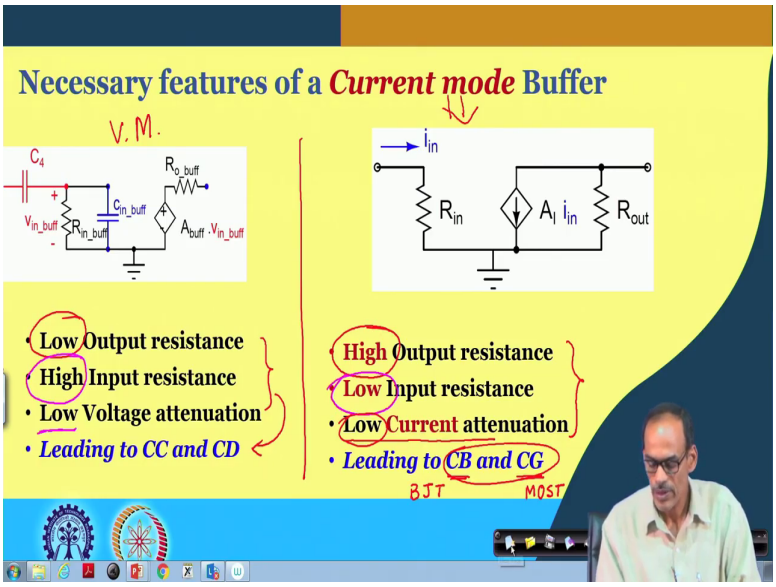
(Refer Slide Time: 07:32)



So, what we have summarized here there is in the previous discussion it is summarized that. For voltage mode operation whatever the buffer we are looking for the basic property, we have seen that the input resistance or input impedance should be high output resistance of the buffer should be as small as possible. And the voltage attenuation offered by this buffer should be as low as possible or you can say that voltage gain should not be much lower than one.

And this requirements are getting fulfilled by common collector and common drain configuration; that we have discussed in our previous years discussion. Now, the counter part of the amplifier in the current domain. So, that is what we will see that the buffer in current mode operation, the requirement here it will be complementary in nature. So, let us see what is the requirement there.

(Refer Slide Time: 08:45)



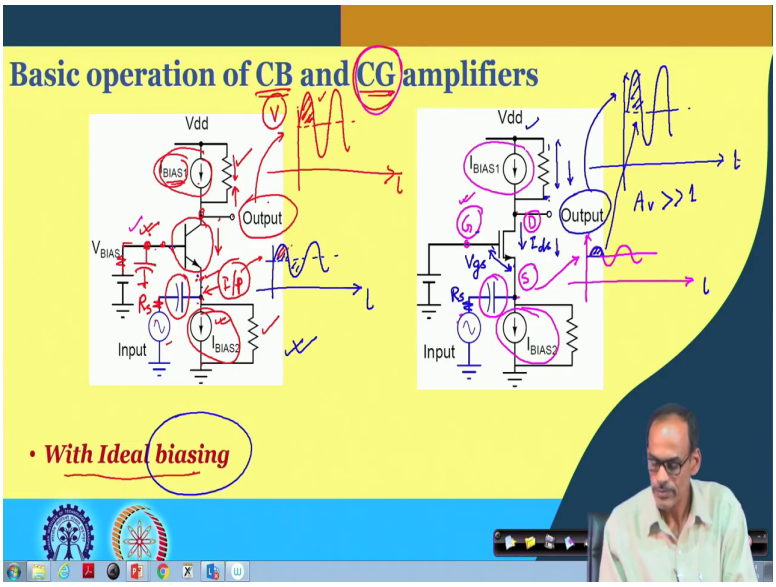
So, this is the current mode buffer requirements it is a listed in this part. So, this is the current mode buffer, this is for our reference we are keeping the voltage mode. So, this is I should say voltage mode a buffer and if you see if you compare the features of these two kinds of buffers; one is voltage mode another is current mode. For voltage mode a buffer output impedance should be as low as possible for current mode output resistance should be as high as possible.

So, likewise if you see the input impedance the requirements are complementary. So, for voltage mode the input resistance should be as high as possible whereas, for current mode buffer the input resistance should be as low as possible. And of course, since it is it is in voltage mode operation we required the voltage attenuation should be as low as possible.

Whereas for this case the current attenuation should be as low as possible. So, this requirement as I said it is getting fulfilled by common collector and or common drain configuration likewise this set of requirement it is getting fulfilled by common base or common gate configuration. Common base is the BJT version and common gate it is the MOS transistor version.

So, that gives us the motivation while we are going for this new configuration namely the common base or common gate configuration. So, let us see basic operation next slide.

(Refer Slide Time: 10:48)



So, the basic operation it is I am keeping both the common base as well as common gate simultaneously because they do have a lot of similarities. So, the analysis can be shared across these two configurations.

So, let us see the basic operation, if I consider the ideal bias situation of course, the input here it is the emitter. So, this is the input node and the output it is at the we are collecting from the collector. And for the time being we know that its basic purpose it is buffered in current mode amplification, but for the time being let we keep our mind flexible this circuit can also be used for voltage mode operation.

So, we will see that why we are insisting for current mode gain later. But let we start with our standard discussion namely the voltage mode operation and then input and output impedance. And then we will be moving towards the current mode gain.

So, coming to the basic operation with ideal bias at the emitter of this BJT we require some biasing arrangement. So, that the DC current need to be supported at the base we require a DC voltage. In fact, we want this node should be the base node should be AC ground. So, if it is DC voltage it is with a 0 resistance it is fine. In case if it is having some resistance here thevenin equivalent resistance coming from the bias circuit, then you may have to add a capacitor here.

But whatever it is signal wise we want the signal at the base should be quote and unquote 0. Now, at the input we can give the signal through a capacitor it may be voltage or current. So, that the DC operating point or at the emitter node should not get disturbed by the DC condition of the input signal source.

So, that is the purpose of adding this DC blocking capacitor. So, the emitter we are giving a signal and as I say that at the output, we are observing the signal either in voltage or current mode. Now, to keep the collector node at high impedance we require a good bias here. So, again this bias purpose of this bias it is to provide the DC current.

Now, these two conductance's finite conductance's, theoretically we are not looking for it, but it may be coming from practical implementation. So, I should say ideally this is good enough and this is good enough and then we are feeding the signal at the source and then we are observing the output and the collector.

So, if you see the signal at the source I should not say source this the emitter rather at the emitter node if you see the voltage wise with respect to time what we are expecting is that we are giving a signal like this. And this signal it is such that the voltage base to emitter voltage it is not taking the transistor into a cutoff region. On the other hand whenever we are applying

the voltage at the emitter what we are expecting at the collector node it is the signal coming. In fact, the signal it is coming in phase.

So, whenever the input it is rising the corresponding output here also it is rising. So, this is the output and this is the corresponding input. So, why it is happening? Let us see if the input at the emitter node the voltage it is rising keeping the base voltage constant DC then v be it is reducing. So, the collector current it is getting reduced. So, if the collector current is getting reduced then drop across this resistance it will decrease. So, the voltage it will increase.

So, in terms of voltage if I see input to output voltage it is having a nice linear relationship and most important thing is that they are in phase hopefully in voltage we are getting a good amplification. In fact, later we will see that it is having very good gain this common base configuration particularly in voltage mode of operation.

So, you may be excited by seeing this you may be thinking that then common base why not it can be used as the voltage amplifier as a voltage amplifier. We will see its limitation, but yes if we have idealistic situation yes, it can be used as voltage amplifier. The major problem starts when you consider the finite source resistance R s and then if I consider input resistance of this circuit ok. I am just giving the hint of the main problem, but anyway we will we are going to cover in detail later.

Now, similar thing it is happening for the common gate circuit. So, for common gate again the we require these two biases current biases they are providing DC support and the DC current support. And then we are feeding the signal at the source node of the moss transistor gate node we are keeping at a DC voltage AC wise it is ground and at the out the output we are collecting at the drain node.

So, since this is common. So, we call it is common gate. So, likewise here also since the base it is common we call it is common base. So, here again if we feed the signal through this DC decoupling capacitor at the source, the signal at the source it should be such that the transistor should not enter into the cutoff region. So, assuming that condition is getting satisfied the

voltage here at the input node or at the source node it is having say sinusoidal form like this and the corresponding output at the drain node.

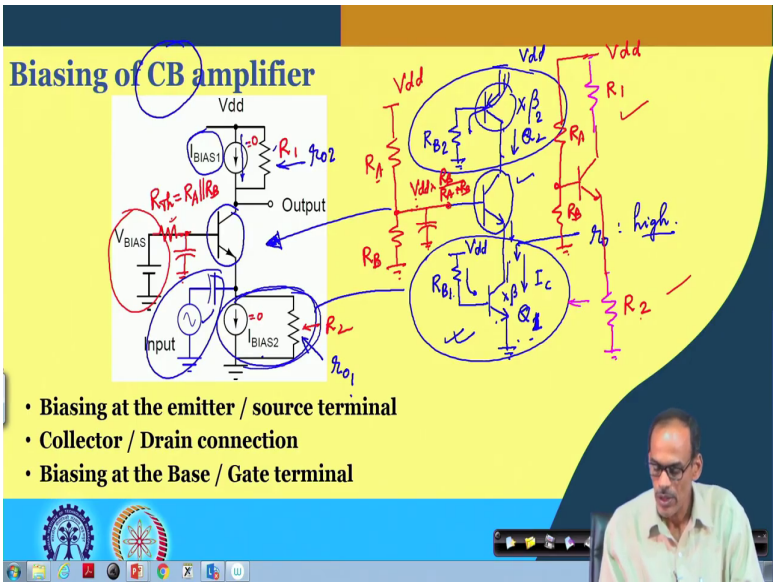
So, we are expecting similar to BJT here also we are expecting amplified signal it will be coming to the drain node why that is, because if the source voltage it is increased by keeping the gate voltage at DC level the corresponding V gs here it is dropping.

So, over this period V gs it is getting reduced compared to its the DC condition. So, the current flowing from drain to source, it is getting reduced and then the drop across this resistance it is dropping. So, the voltage here since this DC voltage so, this DC voltage and the voltage coming at the output which is V dd minus this drop that is getting increased.

So, I should say that input to output they are in same phase. So, this is the output and again similar to common base here the input to output we do get dissent gain voltage gain it is in fact, it is much higher than 1. So, we will see the issues in case if the signal source it is having finite source resistance R s and if we consider input resistance of this circuit we will see what kind of problem it will be there.

But for the time being let we consider the circuit it will be analyzed for voltage gain input resistance and output resistance little bit about. So, this is the basic operation little bit about biasing we can touch upon. So, in the next slide we will be discussing about the biasing of the common base yeah.

(Refer Slide Time: 20:35)



So, biasing of the common base amplifier, here how do you practically make this bias. Suppose you do have the BJT main BJT is here and here either we can put a put another transistor say npn transistor having a meaningful bias at its base.

So, based on the supply voltage here and then R B it produces a base current and then after multiplying with beta of this transistor we are getting the corresponding collector current. So, this collector current it is working as emitter current of the main transistor yeah. So, implementation of this circuit it is it may be like this.

In fact, this kind of arrangement it is good because output impedance of this circuit looking into the collector of the second transistor here it is r naught which is quite high. So, this is high. So, that gives us a good current source which we are looking for biasing this transistor

at the emitter. So, likewise at the collector side, either maybe we can put pnp transistor with a meaningful bias here.

So, we can have V dd here and then we can have another resistor there let me call this is R 2 RB 2, RB 1 here. So, this transistor again based on its base current and after multiplying with its own beta it provides the collector current, which is useful for this transistor main transistor for the biasing at the collector terminal. So, ideally speaking, this kind of biases are desirable, but even if we do not have for this bias circuit even if you have simple bias. Simple bias in the sense instead of the active device, even if you have say passive element that may be good enough even here also we can put a passive element and in between we can have the corresponding main transistor.

So, I should say this is a simple biasing scheme of the common base circuit. Now, at the base node on the other hand we are looking for a DC voltage here. So, to have a DC voltage there we require appropriate potential divider which may generate a DC voltage different from the main supply V dd to some intermediate voltage. Based on this potential division here let me call this is R A and R B we can generate a voltage here. So, this voltage it is V dd multiplied by R B divided by R A plus R B. And then, Thevenin equivalent resistance of this bias circuit if I consider this the bias circuit. So, if I call this is Thevenin equivalent resistance R th from the network analysis you may recall that Thevenin equivalent resistances is RA coming in parallel with RB.

Now, if we have some finite resistance here it is always better to take this node to AC ground. So, we can simply put a DC decoupling capacitor or I should say it is a capacitor which ensures that no signal it is practically no signal it is there. So, here also we can put a capacitor here. So, similar kind of things we can do here also for the simple biasing scheme. So, we can have RA and RB. So, whatever we do model wise, if we say that this is R 1 and this is R 2. So, directly we can say that this resistance it is R 2 and this is R 1 and this current is 0 this current is 0 for this simple biasing scheme.

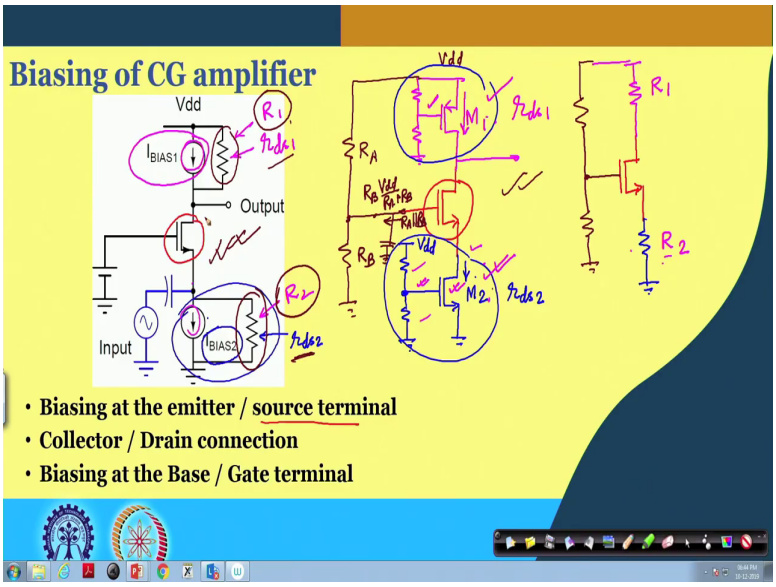
On the other hand if we have say active biasing scheme namely this one. So, you may say that this resistance it is r naught of this transistor say Q 1 and or rather let me call this is Q 2 and

no that will be confusing. So, let me call this is Q 1 no problem Q 1 then this is Q 2 and so here we may call this is r o 1 that is the r o 1 of this Q 1. And this resistance is r o of the second transistor and whatever the DC current we do have here without considering the early voltage whatever the DC current we do have that gives the nonzero value of this I BIAS1. So, likewise this DC current it is giving us the I BIAS2 ok.

So, in summary we can we can see that and the practical circuit is given here that can be translated into this idealistic situation. Whenever we will be talking about the numerical examples, we will be discussing little more about how to decide the biasing and all. But for the analysis point of view particularly to find input resistance and output resistance and voltage gain and current gain, we may use this this biasing scheme simplistic or model of the biasing scheme. And that may be good enough to get the information about the characteristic of the common base amplifier.

So, similar to the common base we can have biasing scheme for common gate. And there also will be having these three the terminal biasing arrangement and of course, after that we can feed the signal here. The signal can be either in voltage form or current form. So, that can be that will be discussed later.

(Refer Slide Time: 28:21)



So, the biasing scheme of the common gate on the other hand here we are having the main transistor. So, we do have the main transistor and then at the source side we do have. So, at the source terminal we need to have a bias here. So, we may say that we can put a transistor here with a meaningful vgs of this transistor. So, that this with a DC voltage meaningful DC voltage here this added transistor let me call this his M 2. And then likewise at the drain side we can add b MOS transistor again here we need to have meaningful DC voltage at the gate.

So, let me call this is M 1 and then the output it is coming from here and then at the gate of the main transistor we can have a bias DC bias here let you call this is RA and this is RB. So, that the V dd here it gives us a DC voltage here which is RB V dd divided by RA plus R B and then Thevenin equivalent registers looking into this circuit it is RA in parallel with RB.

So, we may add a capacitor here to avoid the consequences of this finite resistance of the bias here. And here the transistor 2 it provides the good biasing scheme here. So, the DC current here without considering the lambda effect whatever the DC current we do have that gives the I BIAS2 and then r ds of this transistor r ds 2; it is giving us the corresponding finite conductance of this bias circuit.

So, likewise M 1; M 1 it is giving us the; giving us the bias circuit here or the corresponding DC current without considering lambda it is given this part. And then r ds of transistor 1; it is giving this resistance or finite conductance.

So, that is the biasing scheme of the common gate. So, as I said that it while we will be talking about numerical examples, we will be discussing about how to find the value of these resistances and so, and so. In fact, you need to be careful here if the current flow here and current flow here they are not properly matched, then there will be a adverse consequences. So, we may have to pay very good attention, so that these two currents they should be quote and unquote equal. And that can be maintained by considering the individual transistors characteristic and whatever the corresponding voltage we do have here.

So, matching of this I should say the source bias source terminal bias and drain terminal bias is very important. On the other hand the simpler version of the biasing scheme similar to BJT is also applicable here it has in fact, many a times depending on the situation we may use simple resistor here. And likewise, the at the drain side we may put simple resistor. Note that we may have different combination namely at the source node we can have simple bias and at the collector we may have the active bias and vice versa. So, we do have different possible combination of the biasing scheme.

And so this resistor we may call this is R 1 and this is R 2. So, this R 2 it is giving this resistance R 2 and this R 1 it is given this resistance. And of course, if we have this passive biasing then the this current and this current they are they can be assumed 0.

So, whatever the biasing scheme we do have whether it is with active circuit or whether it is passive bias, that can be or may be combination of them that can be a model by this schematic. So, for our the circuit analysis small signal circuit analysis we may not be going to you know the detail circuit here. Rather we may use this simplistic biasing scheme and then will be going for the corresponding analysis.

Only thing is that you have to keep in mind that, we need to consider these two elements either R 1 or r d r ds 1 or R 2 or r ds 2; we need to consider finite value of this elements in our small signal analysis. So, let me take a short break and then, we will come back with a small signal analysis.