Analog Electronic Circuits
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Lecture – 44
Common Collector and Common Drain Amplifiers

So, dear students welcome back to our NPTEL online certification course. The course title it is Analog Electronic Circuit, and now myself Pradip Mandal from E and EC Department of IIT, Kharagpur. Today's topic of discussion it is Common Collector and Common Drain Amplifiers. Based on our overall flow let us see where we stand.

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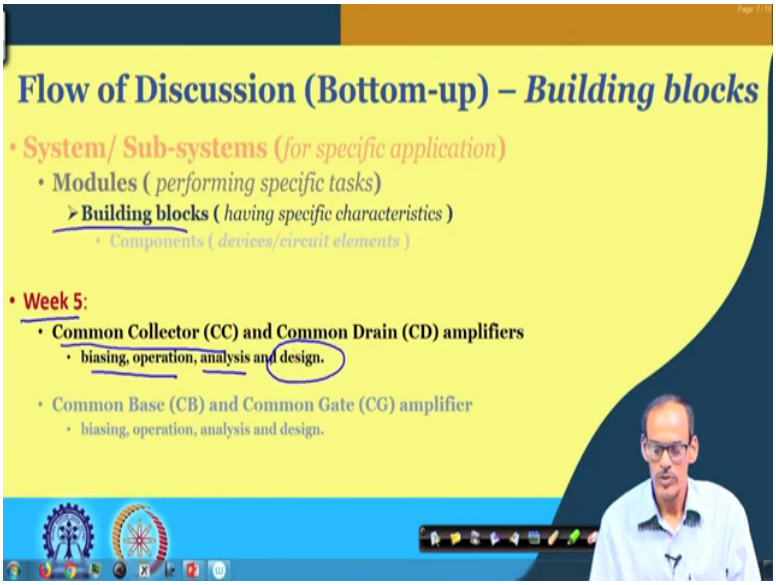

We are in week 5 and we are discussing about the building blocks, specifically we are going to discuss as I said common collector amplifier and common drain amplifiers. We will discuss about the basic operation and biasing, and then also we will be discussing about circuit

analysis to find its performance parameter expressions. Design part will be covering later, so in the next week probably next discussion will be covering that.

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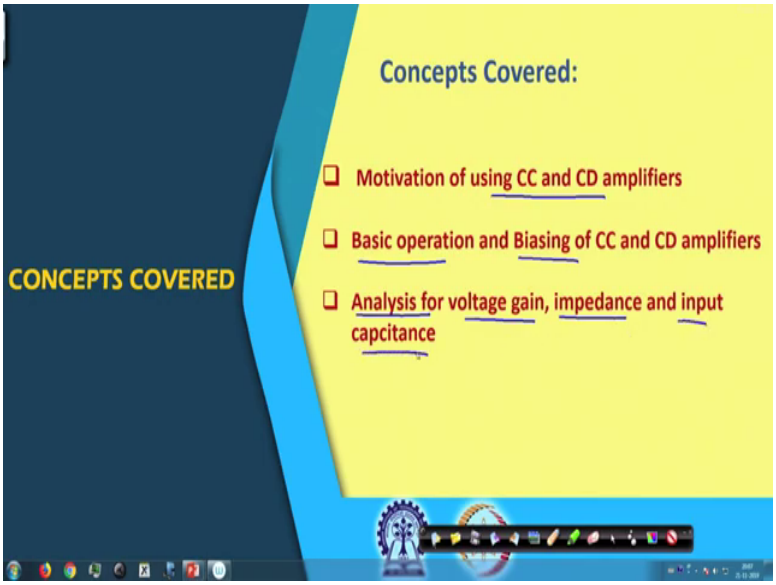

So, the concepts we are going to cover in today's discussion it is the following. We shall start with the motivation of going for this new configurations namely common collector and common drain amplifiers, and then basic operation biasing, and then analysis for specifically for voltage gain, input and output impedance of those amplifiers and then input capacitances.

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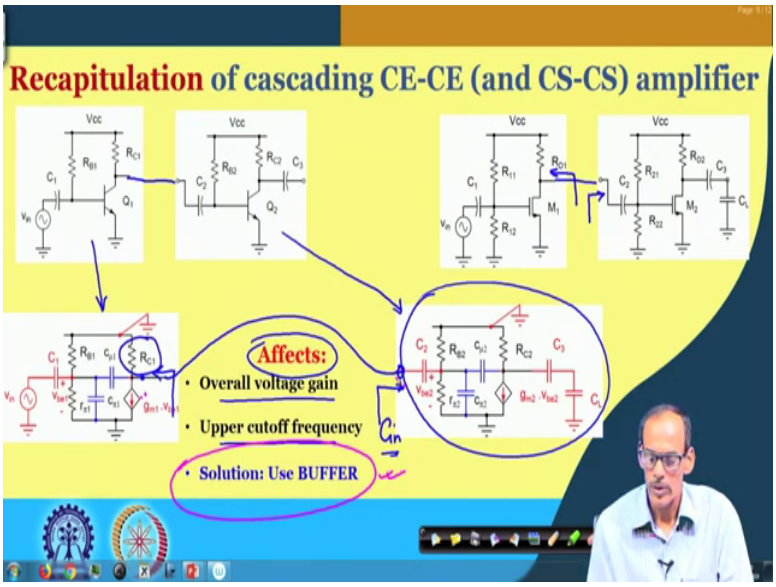

So, let us see what is the basic motivation, rather let we try to recapitulate whatever the discussion we had in the previous class. Namely, what are the limitations it was there for common emitter and common source amplifier specifically when we are cascading say two stages by connecting output of the one CE amplifier to the input of the next CE amplifier.

What we have seen here, it is suppose this is the small signal equivalent circuit and then small signal equivalent circuit of the second stage, and then if you directly connect it what we have observed that the input resistance and then output resistance of the previous stage, they were dividing the signal. As a result the signal arriving to the input of the second amplifier it is not same as whatever the signal we obtained there in unloaded condition.

And also what we have seen that the input capacitance at this the second stage, it is affecting the previous stage, namely output resistance of the previous stage and input capacitance of the

second stage they were forming one pole and it was affecting the upper cutoff frequency. In fact, this is true for common source cascaded with common source amplifier also.

So, even for common source to common source amplifier. What you have observed that the output resistance of the first stage and input resistance as well as input capacitance of the second stage they were affecting the overall performance. So, the affected parameters are in listed here. Namely, the voltage gain it was getting degraded and also the upper cutoff frequency of the overall amplifier it was getting and getting limited by input capacitance and then output resistance defined pole.

So, what is the solution for that? It is we can use a buffer in between these two circuits and if you have some specific buffer protecting the previous stage of the first stage from the loading effect coming from the second stage, then we can say that the overall gain of the system or overall the amplifier performance it remains intact even if you are cascading it. So, what is this buffer?

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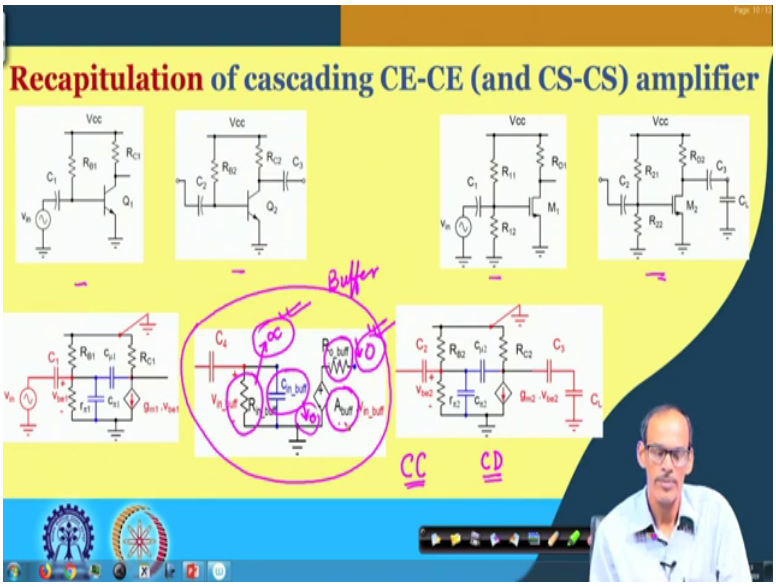

So, the model of the buffer it is given here. So, we can think of it is also a voltage amplifier. And what are the basic requirement of this voltage amplifier? It is that the input resistance here it will be it should be as high as possible and on the other hand input capacitance would be as small as possible. And then the output resistance of the buffer should be as small as possible. So, if we have this 3 important performance parameters are getting achieved by some circuit, then we can say that this is working as a buffer for cascading to amplifier so, whether it is CE-CE or CS-CS.

And this buffer it is to get this buffer what we are looking for it is as we said that the input resistance to be high, output resistance should be small, then input capacitance should be small, that is getting obtained from different configuration. If it is BJT based circuit it is

common collector configuration, if it is mass based circuit then it is common drain configuration. So, that is what the basic motivation of going for this new configuration.

But while we will be going for these two new configurations, we need to establish that we are really achieving the these requirements namely the input resistance to be high, output resistance should be small, and then input capacitance should be small. In addition to that the gain should be should not be say very much less than 1.

In fact, we want this gain should be high, but since we are trying to achieve low output resistance achieving this voltage gain along with output resistance to be small is not really a practical one. So, on the other hand while you are trying to achieve the low output resistance at least we can say that the buffer should not attenuate the signal. So, even if the voltage gain it is may be close to 1, we should be happy with that, ok.

So, this is the background of going for this new configuration, and let us see how and what are the performances we are getting out of the common collector stage.

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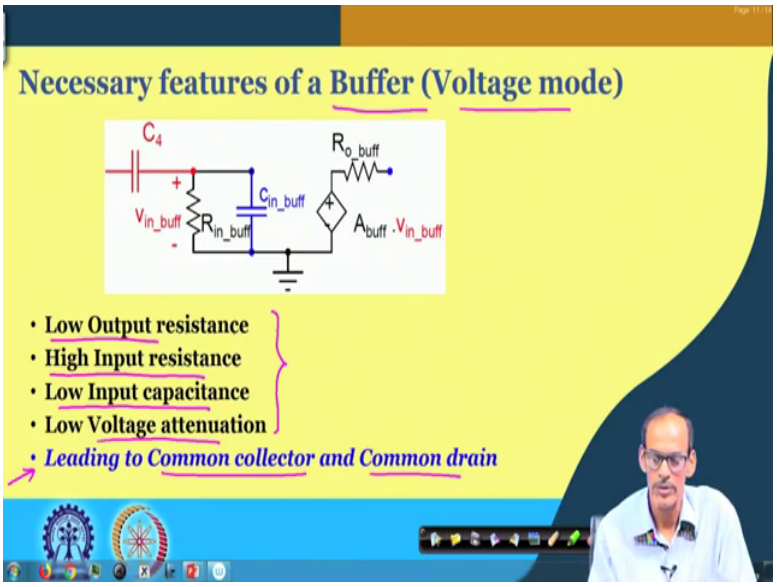

So, as I said this is the summary of that. Just know what we said is we are looking for this buffer circuit particularly for voltage mode amplification, and the important performance matrices we are looking for it is in summarized here. Namely, the output resistance should be low, input resistance should be high, and then input capacitance should be as small as possible, and then voltage attenuation should be low rather we should say the voltage gain even if you are not getting good gain, but the voltage attenuation should not be very high.

And that leads to this new configuration or different configuration namely a common collector and common drain for BJT and MOSFET version of the amplifiers. So, let us now go to this new configuration common collector configuration, ok.

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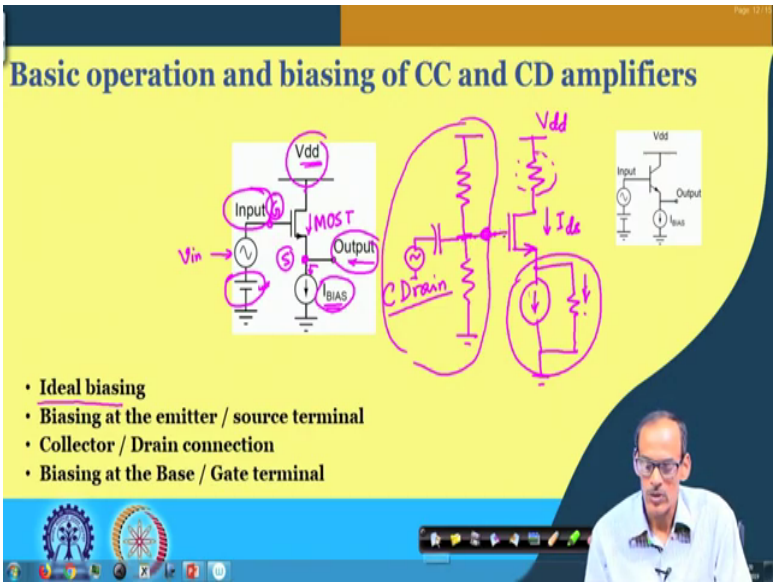

So, let me start with the common drain first say. So, here we do have the basic common drain configuration are listed here. So, we do have the MOSFET here, and at the input namely at the gate we are feeding the signal, the signal we are giving at the gate along with a meaningful DC voltage, so that the transistor it is really on and then the signal we are giving in series with that. So, this is the input signal.

So, on the other hand at the source of the mass transistor we are having a DC bias current. So, that it consumes the whatever the drain current drain to source current is flowing at the same time it is ensuring that this node towards the ground it is quote and unquote open. That means, it is having high impedance looking into the bias circuit.

And the output you are observing at the source; the third terminal namely the drain it is connected to V dd, ideally it should be connected to V dd which is AC ground. So, we can say

that we are feeding the signal at the gate and we are observing the output at the source and the drain preferably we are connecting to AC ground and hence we call this is common drain. So, that is why this terminology it is their common drain.

Now, in ideal situation if I say that ideal biasing situation, the drain it is connected to V dd and at the source we like to have ideal current source. Namely, its conductance should be as small as possible. But then if I consider a practical circuit what normally will be getting it is may be close to that. So, at the source we may not be having ideal current source, we may be having current source along with a finite conductance connected to ground. The drain side on the other hand, so the drain side it need not be connected to V dd directly, even if it is connected to through a resistance or some other element connected here, then also we call it is common drain.

At the gate on the other hand at the gate while you are feeding the signal we are expecting that there will be a DC voltage. So, either we may provide a meaningful DC here by using a potential divider and then feed the signal through a AC coupling capacitor or what we can say that we may say that the previous stage, whatever the previous amplifier stage it may be feeding the signal along with a meaningful DC voltage.

Note that if you observe carefully at the gate the current flow current flow of this transistor it hardly depends on the gate DC voltage. So, even if say this DC voltage may not be precisely to a target one then also it is it will be fine because the I ds current of the transistor, it is primarily defined by whatever the current we do have we are sitting there.

So, in case if the gate voltage it is not precisely at our target then the corresponding source voltage may change and maybe this current may change, but then assuming that this resistance is relatively high and the whatever the current changes we do have because of the gate voltage it is not exactly the target one then also it is ok, because even if the current is slightly different it hardly matters. So, instead of having a potential divider and fixing the DC voltage at the gate, what we have done for the common source amplifier, in this case it is very common to directly feed the signal at the gate, ok.

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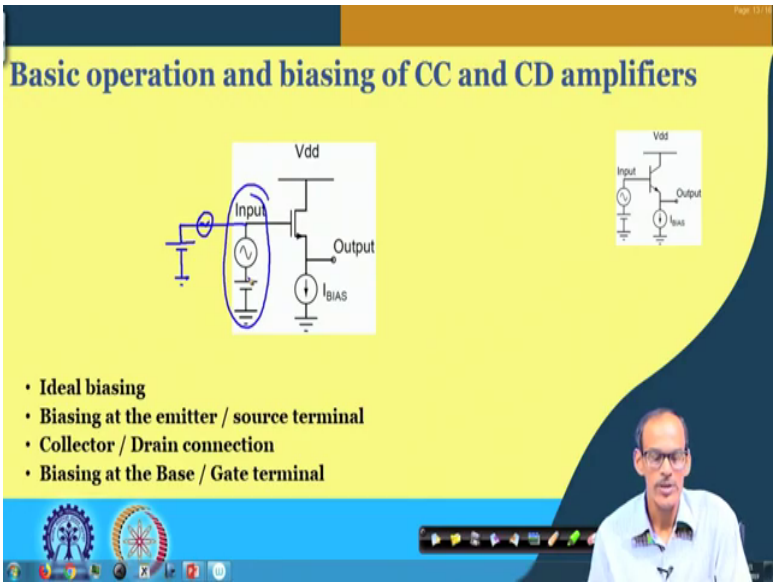

So, what we like to say that the previous stage DC voltage, whatever the previous stage DC voltage may be there that may be good enough along with whatever the signal we do have. So, that is why whatever the biasing arrangement we do have that is I should say it is quite practical. So, that is about the its operation and its biasing.

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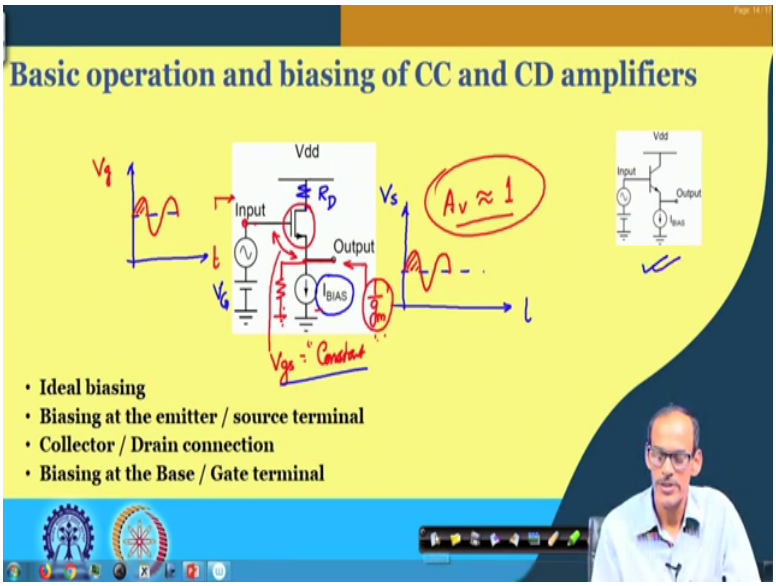

So, what we are expecting that at the gate node? If you see at its gate we are having a voltage, DC voltage, defined by this V g or whatever you say. And then on top of that we do have a signal riding over that and so this is the gate voltage V g as function of time.

Now, at the source node if the current is remaining constant then you can say more or less you can say that this V gs, V gs it is quote and unquote remaining constant. So, if I am having a signal, if I am having a signal at the gate, so it is expected that at the source node it will try to follow signal wise, it will try to follow the gate voltage.

So, if I observed the source voltage with respect to time and since this current is constant, this current is constant and that is making this V gs it is almost constant that is obtained by maintaining the same signal coming to the source. Note that the gate voltage and the source voltage amplitude it is quote and unquote equal and they are also in the in same phase. So, operation wise whatever the voltage you are applying here signal we are getting almost the

same voltage at the source node and so we can say that its voltage gain approximately equals to 1.

And now we claim that the input resistance of this circuit it is very high and output resistance it is quite low. In fact, output resistance it is 1 by g m. So, that is what we will we will derive that, but intuitively you can say that this is the basic operation of the circuit. At the gate we are feeding the voltage signal. At the source we are observing the corresponding output and the output it is almost having the same magnitude and having the same phase.

So, this the voltage gain approximately 1, what we said it is quote and unquote it will be again it will be approximately remaining 1, even if we put say significant amount of conductance. Mainly because the output resistance coming from the device here it is 1 by g m which is expected to be much smaller than this conductance path here.

So, even if you consider practical cases, namely even if you are having a load connected here or finite conductance coming from the bias circuit still the voltage gain it is approximately 1. In fact, this is also valid if even if you are having say drain resistance in between the drain terminal of the transistor and the supply voltage. So, that is the basic operation. So, similarly let us look into the common collector stage, its basic operation and how it is getting biased.

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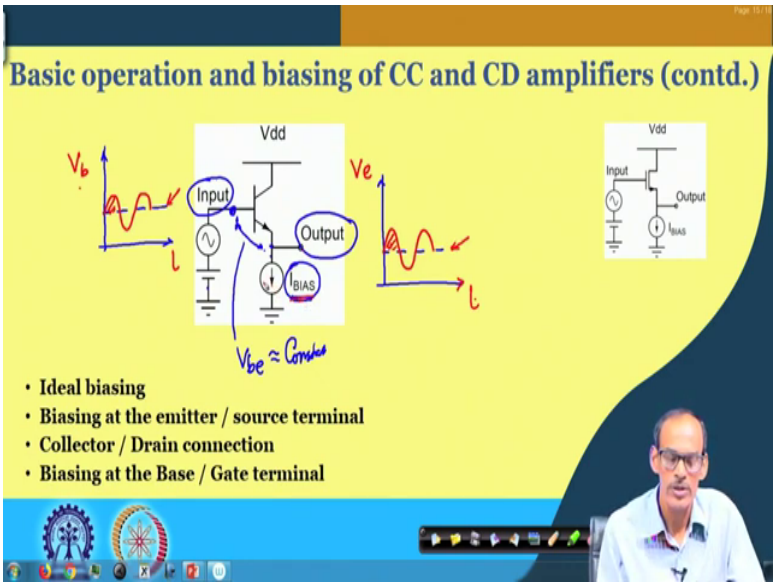

So, here we do have similar to the previous case, here we do have the base node it is getting the input signal and emitter node, at emitter node we are expecting that the signal will be sensing.

So, if you see here the again the biasing here it is at the emitter, we are fixing the current and whatever the voltage you are applying here and the emitter node it is getting self-adjusted to maintain the same current which means that at the base node if we are feeding a signal having a meaningful DC and then on top of that if you are having a signal, so this is the base voltage with respect to time, at the emitter node what we are expecting that the base to emitter voltage V be it is almost constant.

In fact, if this is ideal current source then I should say it is constant, and as a result V be if it is constant then at the emitter we do have a voltage DC voltage, on top of that we do have the signal.

So, we can say that the emitter voltage and the base voltage they are almost the difference is remaining constant. So, the signal here and signal here they are same, only the DC voltage level here and DC voltage level here they are different, they are different by V be on. Now, so this is the basic operation and it is biasing wise at the emitter we are connecting a we are expecting that will be having a good current source.

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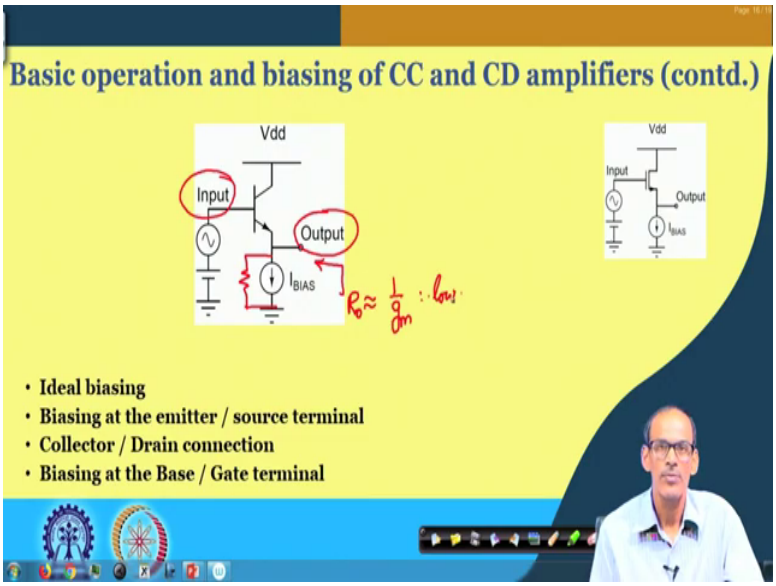

But even if we do not have a good current source, even if we have finite conductance of this bias circuit or even if you are connecting some load then also it is expected that the output

voltage very close to the input voltage and here also we are expecting that R out, R out to be very close to 1 by g m of the transistor which is low, this is low.

Now, let us go a little detail of this both the circuits, namely a common collector and common drain using their small signal equivalent circuit to really find whether the input resistance and output resistance, input capacitance whether they are at part of whatever our requirement we do have.

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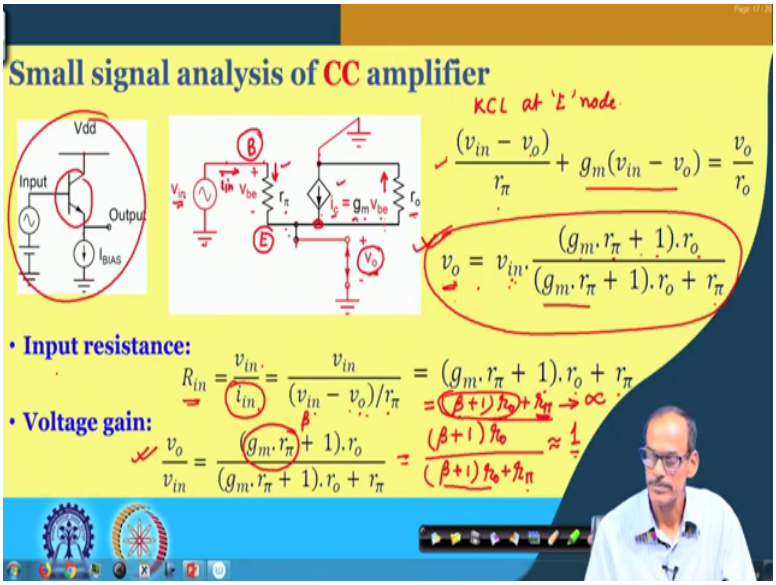

So, this is the small signal equivalent circuit of the common collector amplifier. So, we do have the common collector stage here the small signal equivalent circuit of the BJT. It is given here it is having r pi and then collector current it is g m into V be. V be voltage it is the voltage across base to emitter terminal and then at the collector we do have the V dd connected which is AC ground. We are also keeping this collector to emitter resistance r

naught and at the base we are given the signal, and at the emitter we are observing the output. Since, this is ideal current source this circuit is open.

Now, to get the input resistance or the voltage gain let us see if we apply KCL at the emitter node. So, if we apply say KCL at emitter node, so what we are getting here? It is the current coming through this r pi it is v in minus v o divided by r pi. So, this is the current. So, this is the first part. And then we do have the voltage dependent current source g m into V be and V be is v in minus v o. So, this is the g m into V be part, the second part.

And then if this is v o at this node it is v o the current flowing through this register it is in this direction which is v o divided by r o. So, summation of this current and then i c together it is giving the current flowing through this r o.

So, that is what we are getting here from the KCL if you rearrange this circuit and taking a v o on the left side, what we are getting here it is v o equals to v in multiplied by g m into r pi plus 1 multiplied by r o. In the denominator we do have g m into r pi plus 1 into r o plus r pi. So, this is the; this is the input and output voltage relationship. From that directly we can get the voltage gain v o by v in. In fact, that is what we do have here, voltage gain.

And then in fact, if you further look into this expression g m into r pi it is nothing, but beta of the transistor. So, it can be written in the in terms of beta. So, in the numerator we do have beta plus 1 into r o. In the denominator we do have beta plus 1 into r o plus r pi. And typically this term it is much higher than r pi, so we can approximate this equal to 1.

On the other hand, input resistance, so looking into the base terminal and with respect to AC ground if I want to know what will be the input resistance. So, that is if I call this is the input current i in. So, R in it is v in divided by i in and i in it is v in minus v o divided by r pi. So, i in it is v in minus v o divided by r pi.

And here we do have the expression of v o in terms of v in, so if you directly put that expression of v o here v ins getting cancel and after simplification what we have it is g m into r pi plus 1 into r o plus r pi. Again, this can be written in terms of beta namely beta plus 1 into r

o plus r pi. And as you can see here this is you can say that r pi coming in series with 1 plus beta into r o, and since this part is very high we can say that the input resistance overall input resistance it is very high.

So, the first two properties namely input resistance is very high that we obtain voltage gain. Of course, voltage gain we are not expecting much, but at least it is the circuit is not attenuating the signal. So, we do have the voltage gain approximately 1. So, similar kind of analysis it can be done for common drain. But before that so, let me go for the common drain circuit in the next slide and then after that we will see the output resistance.

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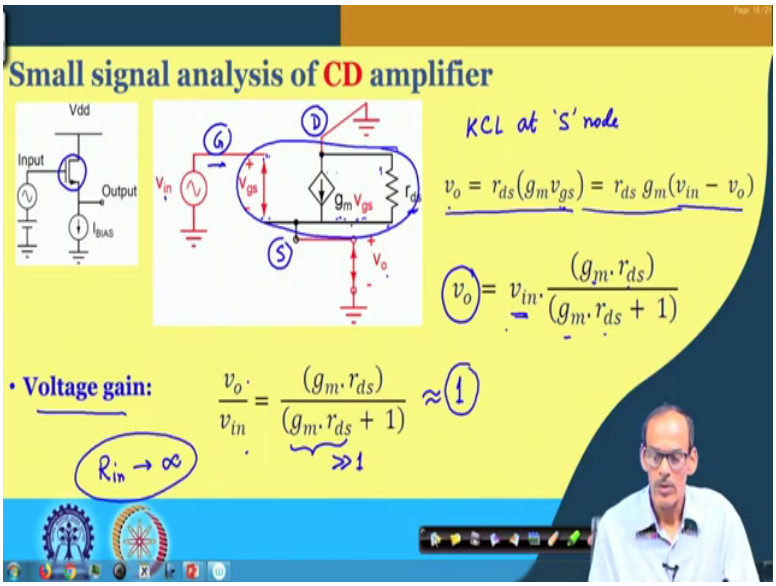

So, this is the common drain circuit and its small signal equivalent circuit is given here the. So, this part is the small signal equivalent circuit of the MOS transistor. Signal we are given here v

in at the gate, so we do have the V gs here, g m into V gs is the current flow from drain to source.

So, this is the source terminal, this is the gate terminal, this is the drain which is AC ground and in this case again if we apply KCL at the source node, KCL at source node so what we have of course this side, we do not have any current flow we do have this current is flowing here and the voltage here it is v o. So, we can directly say that this current equal to this current which is v o divided by r ds or we may say that this current is flowing through this one developing this v o voltage. So, v o it will be g m into V gs into whatever r ds we do have.

So, that is what either we can say it is KCL or if you analyze this loop and find the expression of v o that gives us this v o in terms of V gs. And then V gs is v in minus v o. So, from this relationship we can rearrange the equation and we can get the expression of v o in terms of v in which is v o equals to v in multiplied by g m into r ds divided by g m into r ds plus 1.

Now, from this one we can directly get the voltage gain. So, v o divided by v in, it is given here. Even for this case also this part it is much higher than 1, as a result this is approximately 1. And note that the input resistance since this gate to source input impedance is infinite. So, we can say that because of the property of the MOS and this R in any way it is very high. So, that is what we are getting two important characteristic. This R in it is anyway it is high, it is high for even say common source amplifier also, but this is what it is important that voltage gain at least it is not very different from 1.

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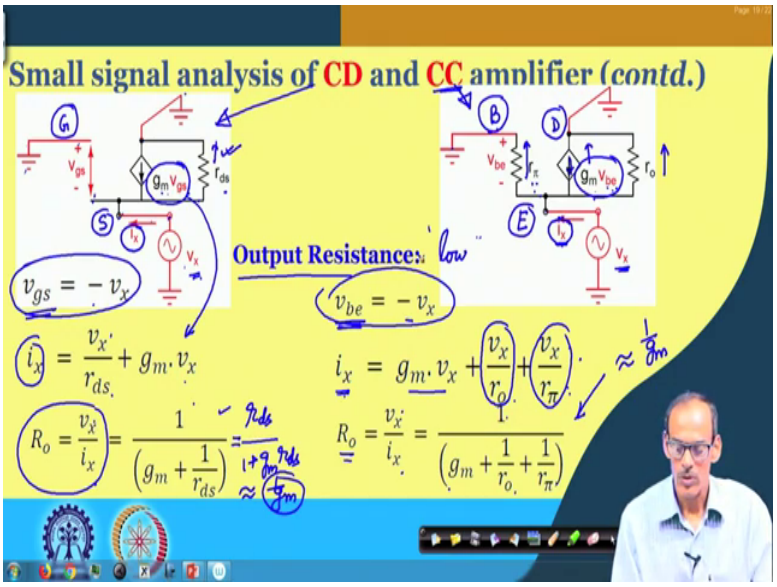

Now, let us see the output resistance. So, for output resistance what we have it is again the small signal equivalent circuit of the common source and common drain amplifier. So, this one is the common drain, small signal equivalent circuit of common drain and common source circuit model it is given here. So, to get the output resistance of this circuit, of course, the output terminal is the source 1. And so we have to make the signal at the gate to be 0, so at the gate we are applying 0 signal which means this is AC ground.

Drain anyway it is AC ground. And to get the output resistance, what we do? We stimulate this source by say signal source of v x and let me observe the corresponding current i x and if this if you take the ratio of v x and i x that supposed to be giving us the output resistance. So, that is why this v this r o equals to v x divided i x.

Now, how do you get this ratio? If you see here whenever we do have this i x and this current is basically g m into v gs with a minus sign and also this current which is actually this is v x divided by r ds. So, on the other hand if gate voltage it is 0 source is v x, so we can directly say that v x v gs equals to 0 minus v x. So, v gs we can say that it is minus v x. So, from that we can say the i x equals to v x divided by rds. So, that is this current and then we do have g m into V gs in this polarity, but we do have a minus sign, so we can say that this current it is same as g m into v x.

Now, if we rearrange this equation what we can get is ratio of v x divided by i x that is 1 by g m plus 1 by r ds. So, that is the output resistance. In fact, you can further simplify this is we can say that this is r ds divided by 1 plus g m into r ds. And this is you can see it is a normal approximation is 1 by g m. So, the output resistance it is 1 by g m which is quite low.

Now, similar kind of analysis can be done for the common collector amplifier also to get the output resistance. So, in this case again V be it is same as minus v x, where v x is the voltage stimulus at the emitter terminal. So, this is emitter terminal, this is base terminal and then this is drain. So, V be it is 0 minus v x. So, V be equals to minus v x and if you see here this i x, i x it is having 3 compound.

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So, what you are talking about is that common collector analysis. So, we do have at the base we do have ground connected, AC ground. At the emitter we are having the stimulus v x and we are observing the current flowing through the emitter terminal. At the base we are having 0 and at the emitter we do have v x. So, we can say that V be equals to minus v x.

Now, we like to get the expression of this current i x and i x it is having 3 components, one is the current flowing through this r pi which is the voltage here v x divided by this r pi and then this current which is v x divided by r o, so this is the second part. And then the third part it is g m into V be and its direction it is in this direction and V be is equal to minus v x.

So, we can say that this current it is g m into v x in the other direction. So, we can say that i x it is summation of all these 3 current components. So, we can say that i x equals to g m into v x, then v x divided by r o and plus v x divided by r pi. So, from that we can say that the v x divided by i x, it is 1 divided by g m plus 1 by r o plus 1 by r pi. So, that is nothing but the output resistance.

So, this again this can be well approximated by this g m terms which is a dominant term and we can say that this is equals to 1 by g m. So, for both the cases the output resistance it is 1 by g m and it is quite low. So, we can say summarize that this is low resistance.

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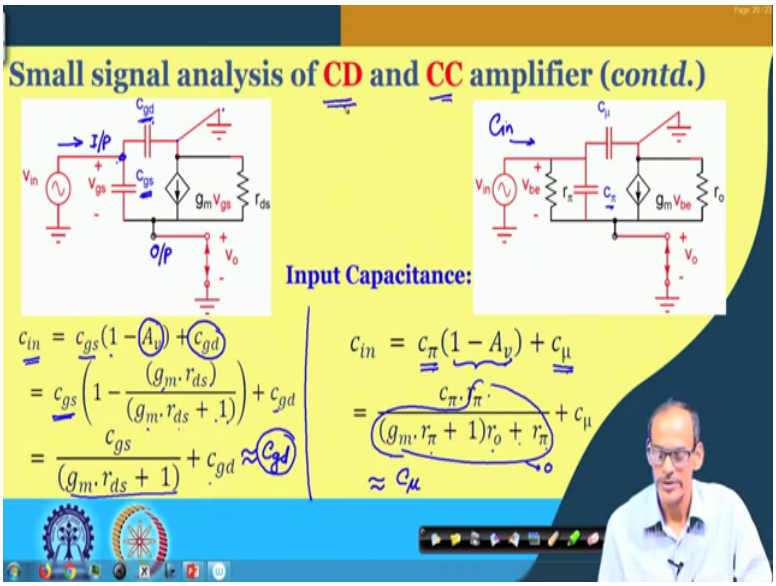

Now, coming to the input capacitance. So, we already got the expression of the voltage gain and its magnitude is very close to 1. So, let we use that information and let we draw the small signal equivalent circuit now we are including the parasitic components namely the C gs and C

gd for the common drain, likewise for common collector C pi and C mu we are including. So, let us see the common drain amplifier and let us try to see what is the input capacitance will be getting for this circuit.

So, input capacitance if we see at this node, C gd it is other end of this C gd is connected to AC ground, so the C gd it is contributing to this C in as the and On the other hand, C gs it is breezing the input and output of this circuit and we know that its voltage gain it is approximately 1. So, if I say that voltage gain it is A v then through Millers theorem we can say contribution of the C gs to input capacitance is C gs multiplied by 1 minus the voltage gain.

And if we put the expression of this voltage gain in terms of g m and r ds which is given here, then we do have 1 minus g m into r ds divided by g m into r ds plus 1. So, this part it becomes 1 by g m into r ds plus 1. So, the contribution of the C gs it is essentially C gs divided by this part. And then of course, C gd it is appearing as is and we can approximate this by C gd.

So, unlike common source amplifier, where the input capacitance it was quite big, in fact, C gd it was getting multiplied by Millers factor and the gain it was quite high. In this case we do have the input capacitance it is only C gd which is very small

So, similarly if I consider common collector amplifier. So, here also the input capacitance looking into the circuit it is having two component, one it is coming from C mu, another part it is coming from C pi. And its expression, it is C mu plus C pi into 1 minus voltage gain and this voltage gain expression of the voltage gain earlier we have seen.

So, if we put its expression and then this part it becomes r pi divided by g m into r pi plus 1 into r o plus r pi. And this part it is very small, so this part it is very small. So, again in this case also we can say that C in, it is approximately C mu. So, that basically says that whatever the in the characteristic we are looking out of the voltage mode buffer that is directly coming from common collector and common drain circuits.

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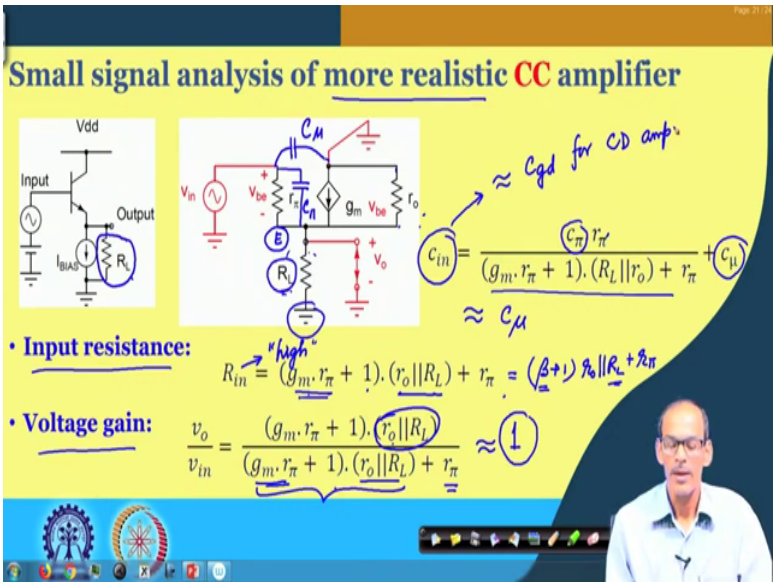

Now, in case if we have some more realistic circuit, namely in case the bias circuit it is having the conductance or maybe some load it is connected, so to represent that we are adding this R L. So, we can say that this circuit it is common collector stage, but it is more realistic. Then what is its consequence on the input resistance, and then input capacitance, and then voltage gain let us try to see that.

So, if you see here the small signal equivalent circuit earlier this part it was open, now we do have R L. And if you see this R L its connection, R L it is connected from this emitter terminal to the AC ground. In fact, this R L it is coming in parallel with r o. So, whatever the previous derivation we already have, wherever we do have r o we can replace this r o by this R L in parallel with r o. So, that is what we are saying here. If you see the input resistance expression

earlier it was g m into r pi plus 1 into r o plus r pi. Now, in presence of this R L instead of only having r o I do have r o plus R L coming in parallel.

So, even though this R L it is coming in parallel with r o, but this part it is quite high. In fact, this part is beta, so we can say that this is equal to beta plus 1 into r o in parallel with R L plus r pi. So, as long as this R L it is really not very small, even if say R L it is in the order of kilo ohms since we are multiplying with beta, so that gives fairly 100s of kilo ohms. So, again even in presence of this R L we can say that this input resistance is quote and unquote high.

Likewise, if you see the voltage gain whatever the previous expression we had where r o was there, instead of using only r o now we can replace that by r o in parallel with R L and this is the corresponding expression. And even in this case since this part it is dominating over r pi because we do have g m into r pi getting multiplied with this, so this is again it is approximately 1.

So, likewise if you see the input capacitance the input contribution of the input capacitor and it is coming from C mu, and this C mu it is appearing as is. And then we do have the C pi here and its contribution here it is C pi multiplied by r pi divided by this big resistance again this can be well approximated by C mu. So, even if you consider this practical value of this R L the input capacitance it is remaining low.

In fact, similar kind of analysis you can do for the common source amplifier also. And there also you will be converging to the similar conclusion, namely the voltage gain remains approximately 1, input resistance anyway it is high, and input capacitance for that case with if I consider C gs and C gd in place of C pi and C mu, so this will be equals to C gd for common drain, ok. So, I think this analysis is helping to establish that common source, sorry common collector and common drain amplifier really working as buffer for voltage mode amplification.

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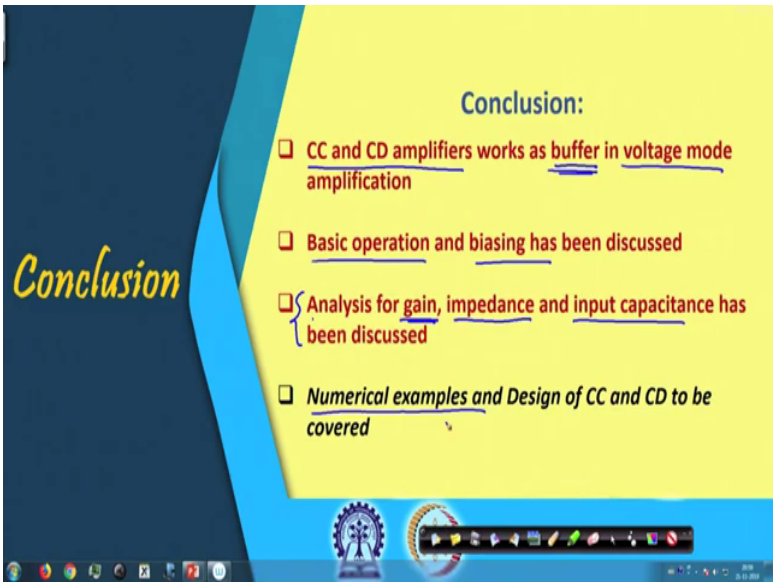

So, this is the conclusion of today's discussion. What we have seen in our discussion that common collector and common drain amplifier they are really working as a buffer in voltage mode amplification.

So, we have discussed about the basic operation, namely where to fit the input signal and where to observe the corresponding output, and then also some biasing basically the source or emitter terminal, we need to put a quote and unquote current source. And then we have done detailed analysis using small signal equivalent circuit to verify that the voltage gain it is remaining close to 1.

Input impedance it is remaining high, output impedance it is low and then input capacitance it is quite low. So, these are the important analysis. It is helping us to establish that it is really

that common collector and common drain can be used as buffer for voltage mode amplification.

Related to this common collector and common drain we need to cover numerical examples and designs that it will be done in the next class. I think that is all.

Thank you.