Analog Electronic Circuits
Prof. Pradip Mandal
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

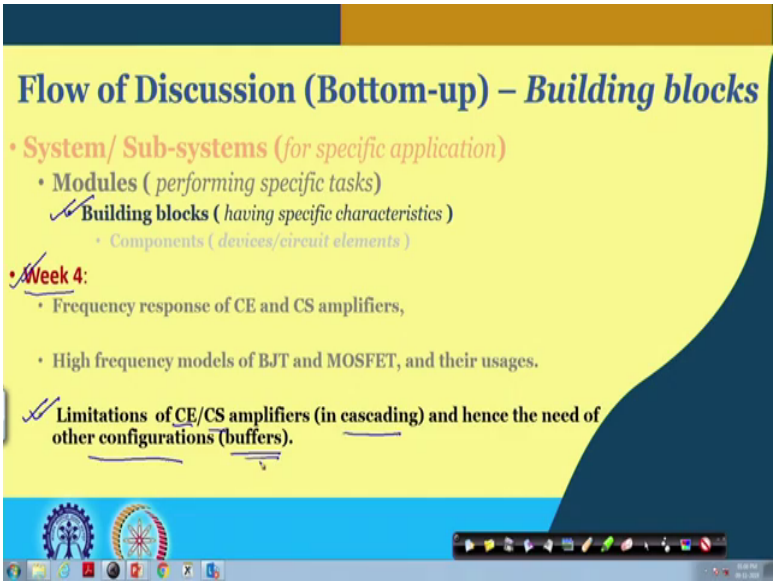
Lecture - 43
Limitation of CE and CS Amplifiers in Cascading

(Refer Slide Time: 00:27)

Dear students, welcome to this NPTEL online certification course on Analog Electronic Circuits, myself Pradip Mandal associated with E and EC department of IIT Kharagpur. So, today's discussion is primarily the Limitation of Common Emitter and Common Source Amplifier particularly when it is when those blocks are getting cascaded. We have discussed about the main feature performance of common emitter and common source amplifier in our previous lectures.

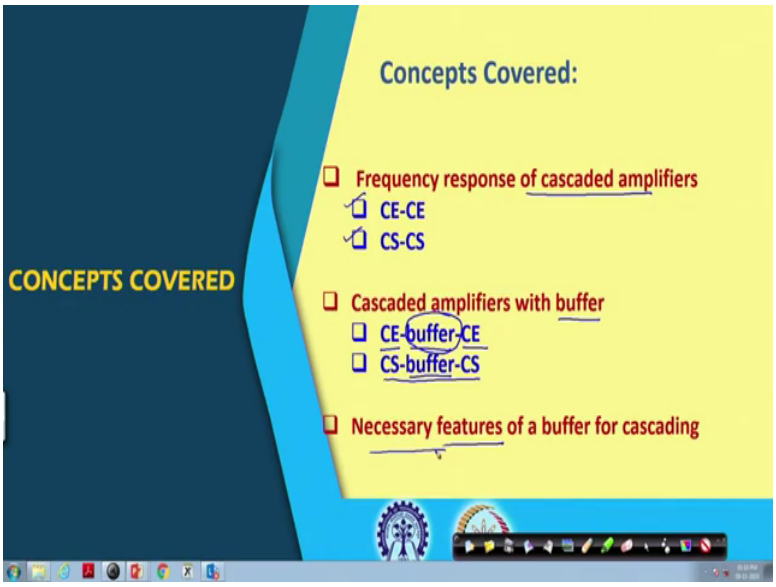
But, then today what we will be discussing it is what are the limitations of this configurations are there particularly when we cascade them. So, let us look into the flow what we have and where we stand today. So, this is the overall flow, present we are in the building blocks and under the building blocks we do have the fourth module or week fourth modules and in this fourth module we are very close to the last item namely the limitation of common emitter common source amplifier while we are cascading the circuit.

(Refer Slide Time: 01:31)



And hence, we establish the need of some other circuit configurations which are referred as buffer. So, we will be discussing those things in detail. So, what are the concepts it will be covered in this today's class.

(Refer Slide Time: 02:09)



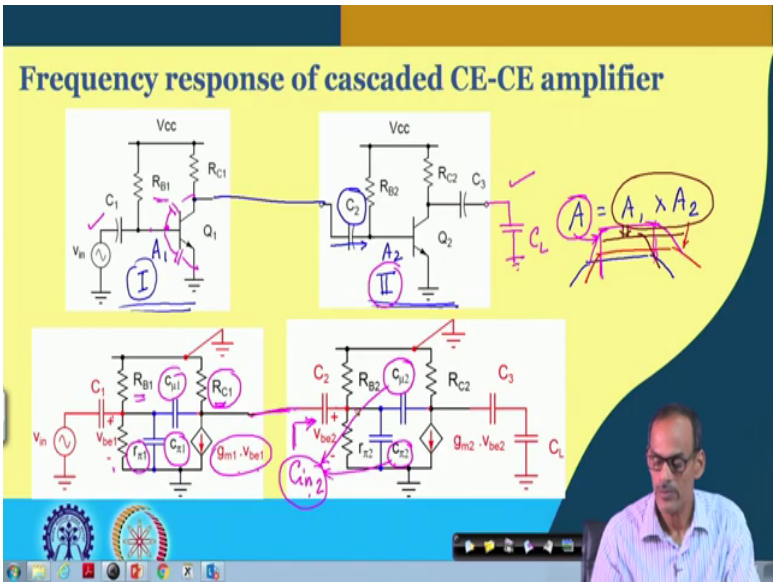
It is to appreciate the what are the limitations or restrictions are there for common emitter or common source amplifier configuration will revisit frequency response of common emitter and common source amplifier, but then the basic difference is that we will cascade to common emitter amplifier.

And then we will see that what is the effect of cascading is there in the frequency response. The effects are similar for common source also, but for completeness we are keeping both the circuits. So, those effects are getting reduced or I should say almost getting eliminated by introducing a buffer and hence, again we will be revisiting the frequency response of common emitter followed by buffer and then followed by common emitter.

So, by presence of this buffer in between we will see that it helps to retain the frequency response of the original common emitter amplifier or whatever the things we are expecting,

similar thing for the common source amplifier also. Now, when we are talking about buffer, we will see that to achieve meaningful cascading what are the features are required out of this buffer. So, that also we will be highlighting. So, that is the overall plan.

(Refer Slide Time: 03:57)



Now, the frequency response of say common emitter amplifier in this case we have discussed more detail of frequency response of individual common emitter amplifier. Let we talk about today it is we do have two maybe identical common emitter amplifier or architecturally they are identical. And to achieve say maybe higher gain or maybe for some other reason we like to cascade this C stage, it is first stage and then you may call it is the second C stage together.

So, how we do that output of the first C amplifier will be connecting to the input of the second C amplifier. But of course, with the use of C 2 we can isolate the DC operating point

of the first stage and the second stage. And of course, the capacitor C 2 it is suppose to be allowing the signal going from the output of the first stage to the input of the second stage.

So, in nutshell C 2 it is helping us to separate the DC operating point of the first stage and the second stage DC operating point. Now, while we will be connecting this circuit we may be expecting that suppose we do have a gain of this stage; it is say A 1 and then gain of this stage it is say A 2 we may be expecting that the overall gain say A equals to A 1 multiplied by A 2. So, that is what we are expecting.

And also in case this A 1 the first stage circuit, in case if it is having some certain bandwidth and the second stage may be having similar kind of profile; maybe it is having certain bandwidth. And then if we combined, so if we; so this is the second stage maybe second stage frequency response.

And if we combine these two stages through this cascading we may be expecting that the overall frequency response it may be having very high gain, and then the lower cutoff frequency it is may be defined by whichever the lower cutoff frequency of the two stay out of these two stages are higher.

And likewise the upper cutoff frequency it may be decided by the upper cutoff frequency of the circuit which is having lower value. So, this is what we are expecting the A should be having higher gain and then the lower and upper cutoff frequency may be decided by whichever is minimum or maximum out of this individual cutoff frequency.

But, in our surprise once we connect the circuit and if we if we make the observation from the primary input to primary output we will see a significant amount of change of this gain namely this gain may drop off here to some other value and also may be the upper cutoff frequency may come down.

So, the out of the observation we may see two important thing; that the gain low free or mid frequency gain it may be different from the product of mid frequency gain of the two individual stages, and also the upper cutoff frequency may be different. So, how and let us see

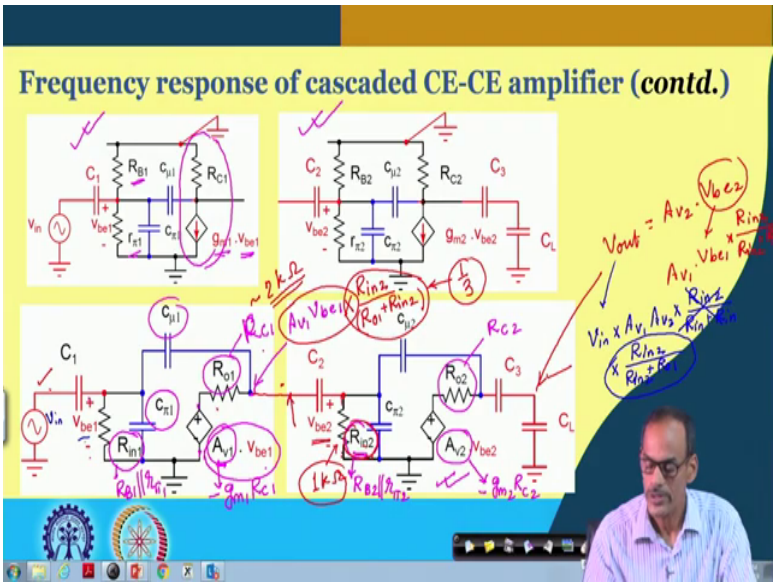
why we see that; here we have drawn the frequency in the low small signal model of the individual stages and if I say that these two stages they are connected here.

So, if we connect the two stages then the resistance here R C one it is coming in parallel with whatever the resistance it will be seen by the next stage. And also, if I see that input capacitance coming from the second stage; if I call say C in of the second stage which may be primarily due to the C pi of the second stage and then miller affected C mu.

So, this C in 2; it is getting contributed by miller affected C mu 2 and then C pi 2 together and then this C in 2 it may be forming a pole coming from this R C 1 and maybe the input resistance here. So, let we rearrange this circuit just to give a brief that in the small signal equivalent circuit what we have it is voltage dependent current source here g m 1 into v b e 1; where the v b e 1 it is v b e of transistor 1. And then we do have the bias resistance R B 1 and then base to emitter we do have R phi 1 and then base to emitter we do have C phi 1 and then base to collector we do have the C mu 1.

So, considering all these small signal parameters what we obtain here is the overall small signal model out of the first CE amplifier. Similarly, for the second stage second CE amplifier; we do have the corresponding small signal equivalent circuit. And let it consider that one load is connected here C L after the C 2, rather C 3. Now, if we further simplify; this two small signal equivalent circuit, we can translate into maybe simpler version. So, in the next slide we will be showing that.

(Refer Slide Time: 10:56)



So, here these two small signal circuits are coming from the previous slide, and we can simplify individual circuits like this. Say, we can translate this R B 1 and R pi 1 together in the form of input resistance R in 1, which means that R in 1 is R B of the this stage in parallel with R pi 1. And, then we are keeping this C pi 1 and then C mu 1 and this part we may translate into Thevenin equivalent

So, the voltage dependent current sources; it is getting converted into voltage dependent voltage source. So, the voltage here it is A v 1 multiplied by V b e 1; V b e 1 is here, and as you know that A v 1 it will be g m 1 multiplied by R C 1 with a minus sign ok. So, that is the A v 1 part. So, likewise for the second stage also we do have the rearranged or simplified equivalent circuit, it is having its corresponding R in again R in it is equal to R B of the stage R B 2 and R pi 2.

And likewise here we do have gain, we do have g m 2 multiplied by R C 2. And the resistance here it is basically it is R C 2, and here also this is R C 1. So, that is how we can translate this transconductance amplifier in the form of voltage amplifier and then input resistance and output resistance you can express in terms of internal resistances.

Now, after this if you see here whatever the signal we are getting here before we connect this circuit, we obtain the voltage here; it is same as whatever almost same as whatever the internal voltage you do have. So, we can see the voltage here it is A V 1 into V b e 1, before we make this connection. But, then the moment we make the connection; the moment we make this connection what will what will happen is that this R 2, it is loading the previous stage as a result whatever the voltage now will be getting here it will be different from this one. And the difference is coming due to the loading effect.

In other words, it introduces one attenuation factor which is defined by R in 2 and this output resistance here. So, R in 2 divided by R o 1 plus R in 2. Now, depending on the relative value of this R in 2 and R o 1 it may be having different value, but typically the these two resistances may be having the same order of magnitude.

In our previous example, we have considered that R C it was in the range of kilo ohms; may be around say 2 to 5 kilo ohms. And this resistance also may be in the similar range may be in the range of say 1 kilo ohm, as a result we can see this factor it will be one-third.

So, this factor with this value of R C 1 and R in 2 this is becoming one-third. So, the overall gain; whenever we see from primary input to primary output here to here the gain of the first stage considering the loading effect of R in 2, it is already having one-third attenuation. But, whatever the voltage it is we are getting here of course, that is considered as V b e 2 and the second stage it is amplifying that.

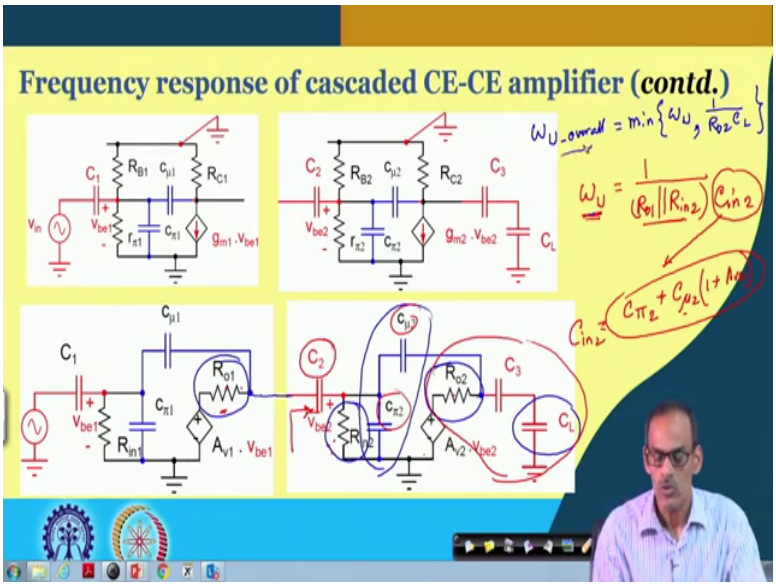
So, the voltage coming at the primary output we can say, it is say V out equals to A v 2 multiplied by V b e 2 and then this V b e 2; this V b e 2, it is A v 1 multiplied by V b e 1

multiplied by the attenuation factor R in 2, divided by R in 2 plus R o 1. So, what we are getting end of it is and of course, V b e 1 it is same as say V in.

So, we can say end of it what you are getting here it is V in multiplied by A v 1 multiplied by A v 2 multiplied by the attenuation factor, R in 2 divided by R in 2 plus R in sorry R. So, that attenuation factor it is R in 2 divided by R in 2 plus R o 1. So, this is one attenuation it is getting experience due to this cascading.

The second effect; second effect is on the cutoff frequency. So, let us see the cutoff frequency. So, what we can say let me clear here yeah, the cutoff frequency particularly the upper cutoff frequency it is having two candidates one is the cutoff frequency coming due to this R.

(Refer Slide Time: 18:10)



And then C L and second one it is of course, this resistance loaded with R in 2 and then whatever the input capacitance. So, do have that may be coming from C pi and C mu of the second stage.

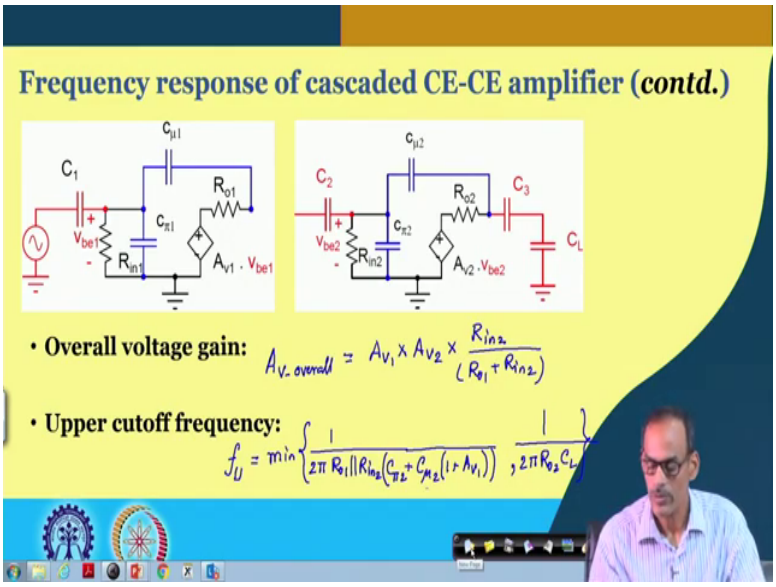
So, the this new candidate to define the upper cutoff frequency if you write. So, we can let me write the expression of that cutoff frequency if I say that is omega; upper cutoff frequency u. So, it is coming due to the resistance R o 1 and R in 2 in parallel R o 1 in parallel with R in 2 and then multiplied with the input capacitance here.

So, the input capacitance in the high frequency of course, this C 2 it will not be there whatever the input capacitance it is coming primarily from this C pi and C mu. So, that we can write say this is C in of the second stage; and then this C in it is C pi almost yeah C pi and almost the C mu multiplied by the 1 plus the second stage gain A v 2; and.

Since, we do have very good gain of the second stage that makes the C in this C in it is very significant, and as a result the pole may be created or whatever the upper cutoff frequency may be created by the C in 2 and then this effective resistance at that node that may define the lower cut the upper cutoff frequency. Of course, if this upper cutoff frequency it is less then whatever the original upper cutoff frequency defined by R o 2 and C L was there then only it will be prominent.

So, I should say that whatever the omega u we have written, this is only one candidate and affect that the overall we can say that omega u of overall. So, that will be of course, minimum of minimum of this omega u and whatever the original upper cutoff frequency we do have; namely 1 by R o 2 and C L ok. So, depending on the situation this upper cutoff frequency may be different. So, what we have said here it is in the next slide we are going to summarize yes.

(Refer Slide Time: 21:30)

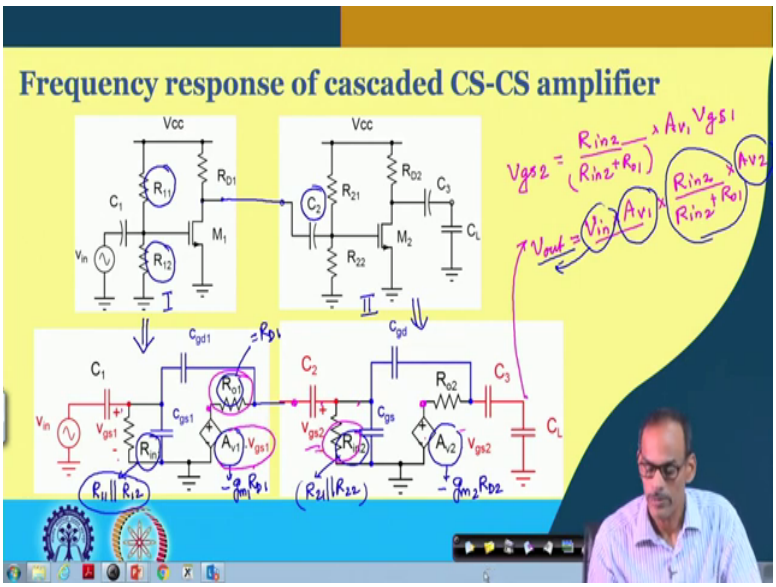


So, in the frequency response what we have seen in the CE cascaded amplifier. First of all, its voltage gain; voltage gain overall voltage gain A v overall, so, that is equal to A v 1, multiplied by A v 2 multiplied by this attenuation which is R in 2 divided by R o 1 plus R in 2. So, this is one change and the upper cutoff frequency as I was discussing there it is f; if I if I write in terms of the hertz then f u so that is minimum of whatever the cutoff frequency we obtain; the candidate of this cutoff frequency as you would say.

So, that is 1 by 2 pi R o one in parallel with R in 2 multiplied by C pi 2 plus C mu 2 into 1 plus A v 1. So, this is this is miller affected capacitance here coming to the input and the C pi 2 as I say that it is as; as it is. So, this is one candidate and then other one it is the original one 1 by 2 pi R o 2 multiplied by C L.

So, out of these two whichever is minimum we have to consider that is the upper cutoff frequency. So, the similar kind of exercise it can be done for a common source amplifier. So, let us look into the common source amplifier also.

(Refer Slide Time: 23:46)



So, here again so, we do have stage I common source amplifier and then another common source amplifier. Architecturally, we have taken they are very similar and we are cascading it to get a higher gain.

So, basically connecting the output of the first stage to the input of the second stage through this DC blocking or DC decoupling capacitor C 2. And, here what you have drawn it is the small signal equivalent circuit out of the first c amplifier. Note that here we have done the

similar kind of exercise namely, converting the transconductance amplifier in the form of voltage amplifier.

So, we do have A v 1 again A v 1 it is its expression is minus transconductance or transistor 1 m 1 multiplied by this R D 1 and here this R o 1 it is equal to R D 1, similar to the previous circuit CE amplifier circuit and here R in 2 it is coming from the two bias resistors in parallel. So, I should say that r in of this stage R in 1, it is R 1 in parallel with R 1 2.

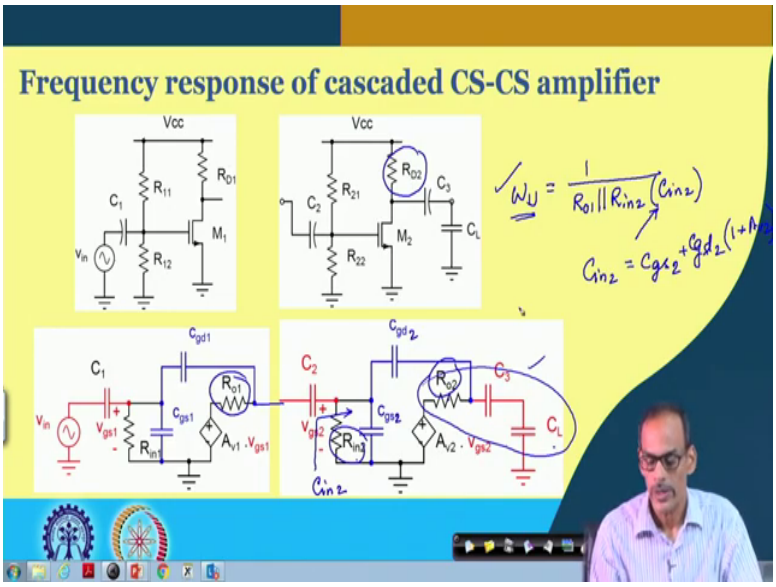
So, similarly for the second stage we do have a input resistance R in 2 which is R 2 1 in parallel with R 2 and its voltage gain A v 2. So, this is equal to minus g m 2 multiplied by R D 2 ok. So, now again for this case also the moment we make this connection there will be attenuation; there will be attenuation because, this resistance and this resistance they are forming a potential divider kind of circuit.

So, whatever v g s will be getting to the second transistor it is not just the entire internal voltage rather will be having one attenuation factor. So, v g s; v g s 2 it is R in 2 divided by R in 2 plus R o 1. So, this is the attenuation part multiplied by of whatever the A v 1 into v g s 1 we are having. And of course, this v g s it is getting multiplied by A v 2 to get the output voltage here.

So, the voltage coming here again if I call this is the final output. So, that becomes the input voltage multiplied by first stage gain if you want. In fact, input voltage it is same as v g s 1. So, this gives the voltage coming here and then we do have the attenuation factor R in 2 divided by R in 2 plus R o 1 multiplied by A v 2.

So, if I take the if I take the A v 1 here in the denominator. So, that gives the gain, so here again the original gain it was A v and A v 2. A v 1 and A v 2 coming from the two stages and then in addition to that we do have this attenuation factor. And, similar to the CE amplifier again here also we do have the upper cutoff frequency it will be getting modified. So, for upper cutoff frequency the new candidate to define the upper cutoff frequency it is.

(Refer Slide Time: 28:29)



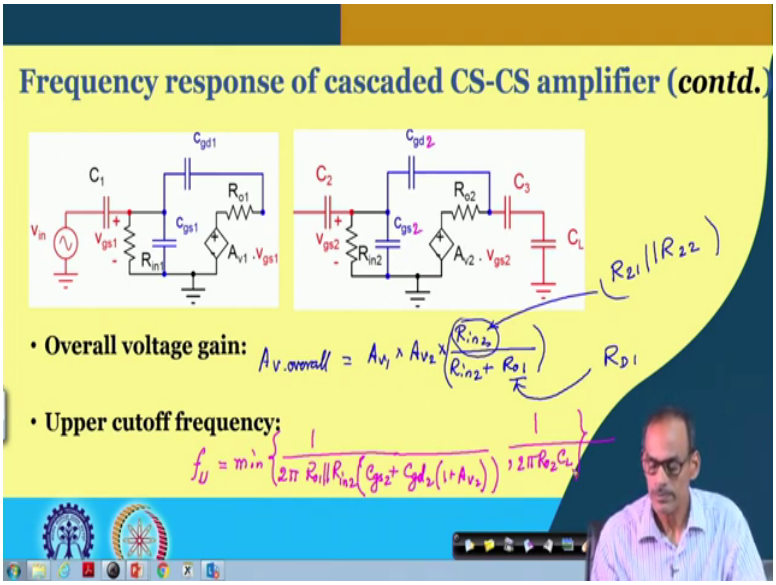
If I call say omega u, the new candidate for the upper cutoff frequency; it is coming due to the input capacitance here C in 2 and whatever the impedance we do have at this node namely R o 1 and R in 2.

So, the expression of this new upper cutoff frequency you are candidate of upper cutoff frequency. It is R o 1 in parallel with R in 2 multiplied by whatever the C in 2 we do have. And then this C in 2, it is C in 2 equals to C g s of the second stage; C g s 2 and then plus C g d 2 multiplied by 1 plus A v 2 right.

So, that is the new candidate and of course, we have to consider the original upper cutoff frequency defined by C L and the output resistance of the second stage by the way this resistance it is nothing but, this R D 2. So, the previous; so, if I consider these two candidate one is this one another is coming from this one. I have to consider minimum of the two. So,

again to summarize what we have it is in the next slide will be considering the effect on the gain as I said A v overall.

(Refer Slide Time: 30:22)

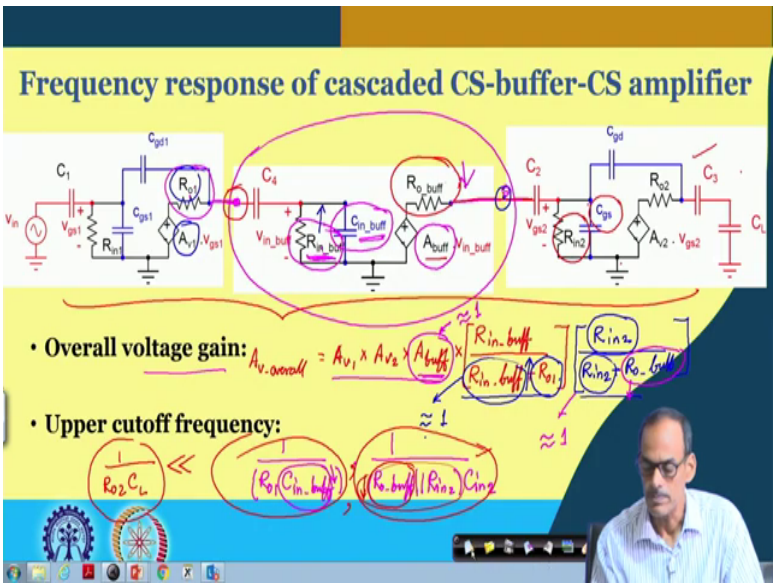


So, that is A v 1 multiplied by A v 2 multiplied by R in 2 divided by R in 2 plus R o 1. So, we do have this attenuation part and as I said that this R o 1 it is R D for the first stage; and R in 2 this part, it is coming from the bias circuit namely R 2 1 and R 2 in parallel and the upper cutoff frequency so again if we write in; in the unit of hertz.

So, f u it is minimum of the two candidate one it is coming from the C in 2 and the resistance there at the cascade cascading node. So, we do have 2 pi then R o 1 in parallel with R o rather R in 2; multiplied by C g s 2 plus C g s C g DC g d 2 right multiplied by one plus A v 2.

So, this is the new candidate and then previous one we are having 1 by 2 pi R o 2 and then C L. Now, next thing is that how do we minimize these two effects namely what may be a solution. So, let us see what may be the possible solution for that.

(Refer Slide Time: 32:54)



If we put a buffer; so if we put a buffer say or say some intermediate circuit having some important feature we will be discussing that such that, the input resistance of this stage; call R in buff. If it is quite high then whatever the attenuation it will be getting introduced by R o 1 and R in buff.

If that is approximately 1 then we can say that the cascading effect here it is very small and also at the same time, now if the input capacitance of this stage buffer stage if it is very small that is also needed to avoid the effect on upper cutoff frequency. So, the basic requirement here it is this resistance of the buffer stage should be very high, input capacitance of the

buffer stage should be as small as possible. And similar kind of thing the; the loading effect it is also possible at this node alright.

So, to avoid the loading effect at this node what you are looking for that input resistance of the second CS amplifier or C amplifier. We may not be having much control, but then in case if we say that if we make this resistance as small as possible then the attenuation factor here it will be less. And, on the other hand if this resistance it is as small as possible even if we have decent amount of C g s and C g d and the input capacitance coming from the second stage still it we can say that is the effect can be almost ignorable.

So, if I if I write the expression of the gain of the overall circuit. So, A v overall; so, we do have A v 1 multiplied by A v 2 multiplied by may be the buffered circuit having some gain A buffer multiplied by the attenuation factor coming at this node; first cascade node cascade node. So, that is R in buffer, divided by R in buffer; plus R o 1. So, this is one factor and then the second factor it is coming from this node; and this factor it is R in 2 divided by R in 2 plus R o buffer ok.

So, first of all to get rid of the this these two effect of this two factor what we can do we may say that we are not allowed to change this original R o 1 because, if I try to change this R o 1 which is coming from the R D 1 that may directly that. In fact, that will effects the A v 1. So, we are not allowed to change here. So, same thing we are not allowed to change the input resistance here only thing is let us see what is the thing we can do on this buffers circuit so that we can remove this effects.

So, if you see that if I want to make this part equals to 1. What you have to do it is, we have to make this; this part R in buff should be as high as possible compared to this one. So, if I make this part it is as high as possible; so we can say this input resistance should be as high as possible then I can make this part equal to 1. On the other hand, if I see the second factor if I want to make it approximately 1. So, what I can say that; this part this part I can make it as small as possible ok. So, if I do it at least in the gain of the entire cascade; cascade circuit you can say that we are retaining the gain of A v 1 A v 2 and A buffer.

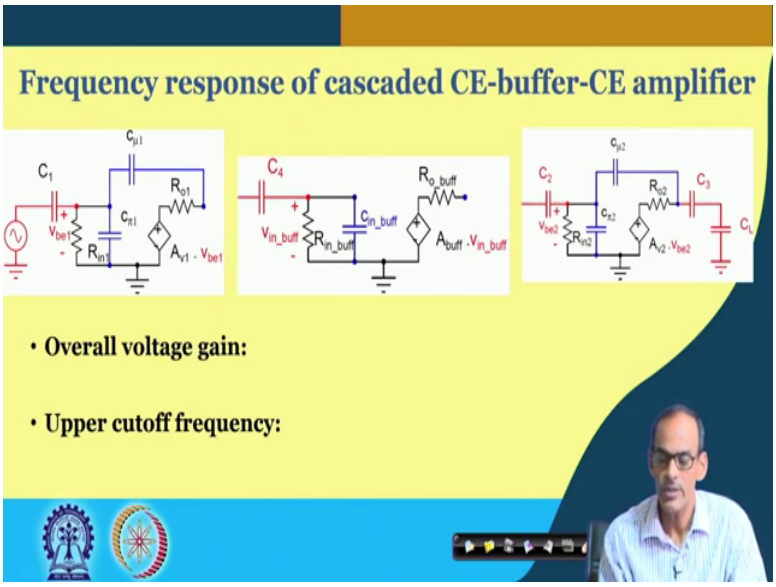
Now, this buffer circuit is we do have a special requirement on this impedance namely we have to make this output resistance as small as possible input resistance should be as high as possible. So, after assuming that we may not be able to really do get good gain, but we have to keep in mind that this A buffer should not attenuate the original signal. Namely, we should be rather happy in case if this part it is approximately 1 ok. So, from gain point of view that is the requirement.

And then if I see that cutoff frequency point of view if I say that this resistance it is this resistance say is very high. So, at this node whatever the pole defining the may be the potential candidate to define the upper cutoff frequency which is 1 by R o 1. And, since this resistance is very high I can ignore that part and then C in of the buffer it is there. So, to make this pole in to make this pole very high, so, that the overall upper cutoff frequency should not get disturbed by this cascading; what you have to do we have to make this part as small as possible.

So, likewise if I consider this node the cutoff frequency there it is defined by R o buffer and in parallel with R in 2 and then we do have the corresponding C in of the second stage. So, here we are already saying that we do require this R o buffer should be as small as possible. So, if this is very small. So, that makes this resistance very small and then corresponding pole here it will be it will be going to high frequency.

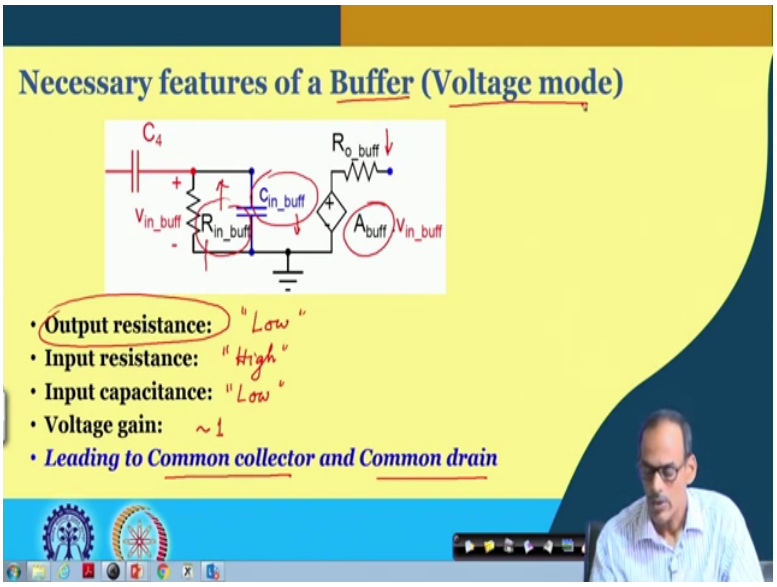
So, if I consider this two new candidate possible new candidate of defining the upper cutoff frequency if you push both of them beyond whatever the original cutoff frequency we do have namely 1 by R o 2 and then C L then we should be very happy about that. So, in other words, if both of these two poles new poles if we push them beyond the original cutoff frequency; then we can say that is it will be the cascading will not be having effect on the bandwidth of the circuit. So, in summary the requirement of the buffered it is the following ok.

(Refer Slide Time: 41:04)



This similar thing we can get for C followed by buffer and C. So, I will not be repeating this part.

(Refer Slide Time: 41:15)



So, you can you can you can do yourself. Now, what we are saying is that what are the necessity or necessary features of the buffer particularly if the circuit is in voltage mode what we just now said that, output resistance of this buffer this resistance should be as small as possible quote and unquote low.

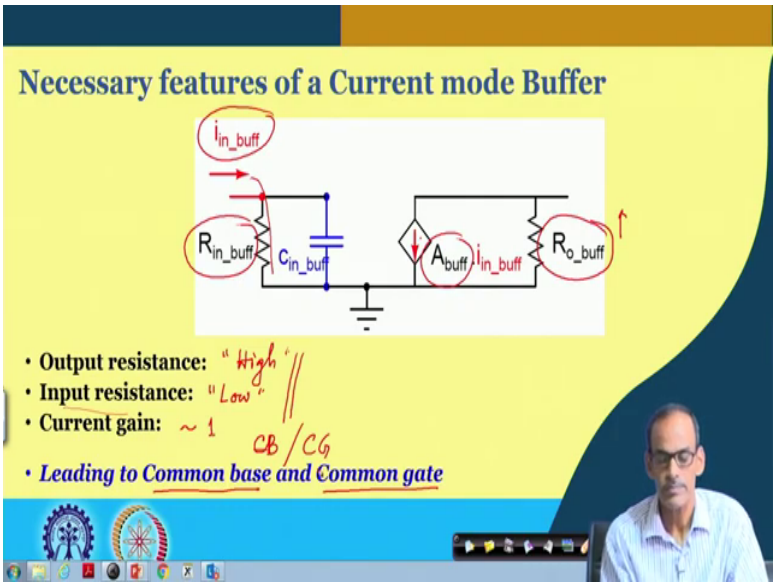
So, on the other hand the input resistance of this buffer should be as high as possible. So, quote and unquote high and then input capacitance again it should be as small as possible. So, that the cutoff frequency should not gets upper cutoff frequency should not get affected. So, again here it is quote and unquote low. And, then the voltage gain of this circuit preferably it should not be very small. So, we should be rather happy if it is in the order of 1 ok.

Now, this kind of requirement it is essentially it will be obtained by different circuit configuration namely; common collector if it is implemented by b j t. If it is implemented by

MOS transistor it will be common drain; which means that this buffer particularly for voltage mode amplifier cascading this buffer it will be implemented by common collector or common drains stage.

Now, we so far we are talking about voltage mode similar kind of things we may experience whenever we will be dealing with current mode amplifier. Namely, cascading current mode amplifier and for that buffer of course, we will be requiring complimentary kind of features. So, what kind of circuits and what kind of features are needed, let us see in the next slide yeah.

(Refer Slide Time: 43:30)



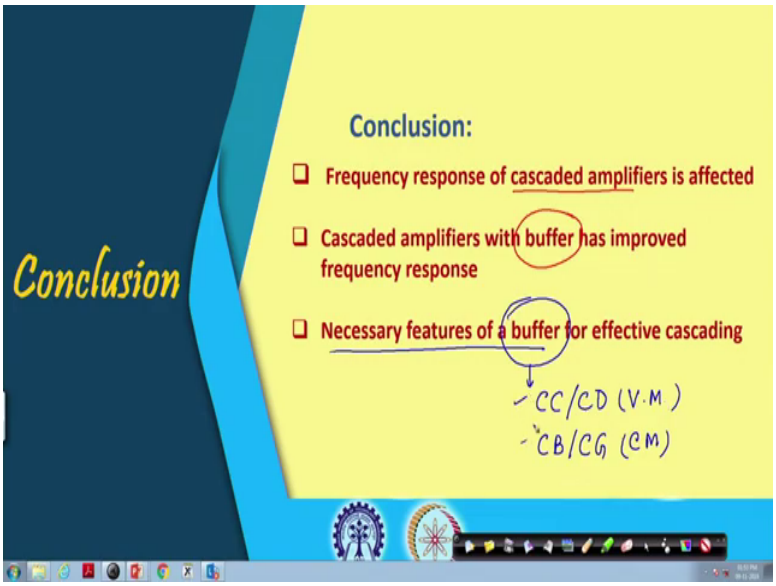
So, this is the required buffer for current mode amplifier cascading. What we are looking for it is that output resistance for this case to avoid the loading effect, output resistance particularly the resistance wise, it should be as high as possible quote an unquote high. And,

then input resistance it is the dual effect to avoid the loading effect the input current should be consumed by this circuit without any problem, so, that we can get the signal propagating there.

So the input resistance it should be quote and unquote low. And then of course, the current gain we should be happy in case we are not attenuating the signal, it may be in the order of 1. And such kind of requirements are getting implemented by the third configuration say for BJT it is common base and if it is MOSFET based then it is common gate.

So, I should say that current mode buffer it will be implemented by this common base configuration or and or common gate. I think yeah, so most of the things whatever we have planned we have covered.

(Refer Slide Time: 45:09)



So, what we have we are going to conclude now it is that the common emitter amplifier we have seen it is having some limitation particularly whenever we are cascading and the its not only its gain, but it is not only its gain it is the bandwidth is also getting affected.

So, that can be avoided or minimized by adding appropriates buffer, if you put in between wherever we are doing the cascading and that improves or rather brings back the bandwidth and expected a high gain of the cascaded amplifier. You also have talked about the necessary features of the buffer particularly for voltage mode buffer input resistance should be as high as possible, input capacitance should be as small as possible, and output resistance should be as small as possible.

And the complementary things are required for current mode amplifier. In case, if you have say transconductor or transimpedance amplifier you yourself can now find what kind of features are necessary for the corresponding buffer. And so this buffer it as I said that it invites new kind of configuration; it is either you can see that common collector or common drain stage for voltage mode buffer or common base or common gate for current mode, current mode buffer.

So, I think in the next class we will be able to discuss more detail about those different kinds of configuration and we will discuss about how they can be design that is all.

Thank you for listening.