Analog Electronic Circuits
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Lecture – 33
Common Source Amplifier (Part B)

Welcome back after the short break and we are about to start the small signal equivalent circuit for the Common Source Amplifier.

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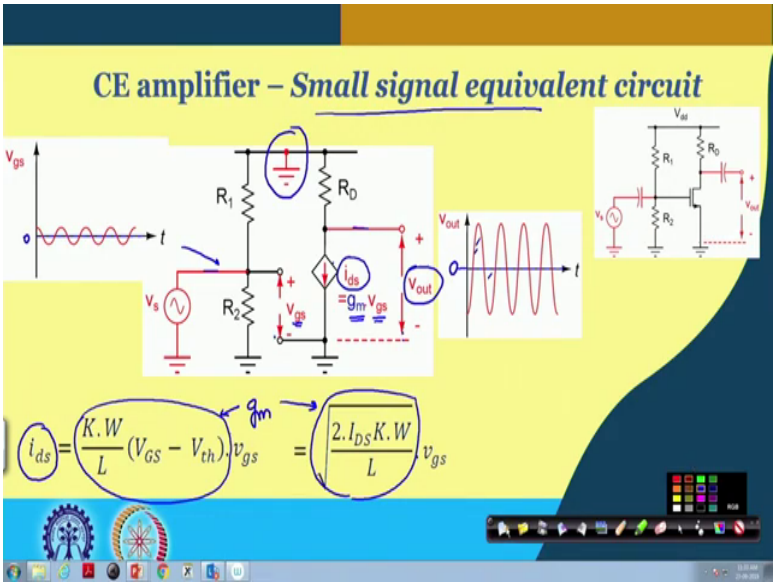

And, what we have said is that in the small signal equivalent circuit first thing is that we are making the DC bias to be 0. And, then the capacitor we have sorted here and the capacitor we have sorted here and then DC current in this voltage dependent current source we made it 0;

living behind the small signal current small i ds which is a linear function of the gs v gs here. So, the v gs is given here and this linear function.

So, the linearity is defined by this gm. So, the expression of the i ds it is given here, this part is the gm as I was telling before or we can have another expression of the gm here. So, that is the expression of the gm and then whatever the output we are observing here that is the small signal output. So, just to highlight that in the signal here, it is not having any DC it is having 0 here and whatever you are observing at the output that is also having DC equals to 0.

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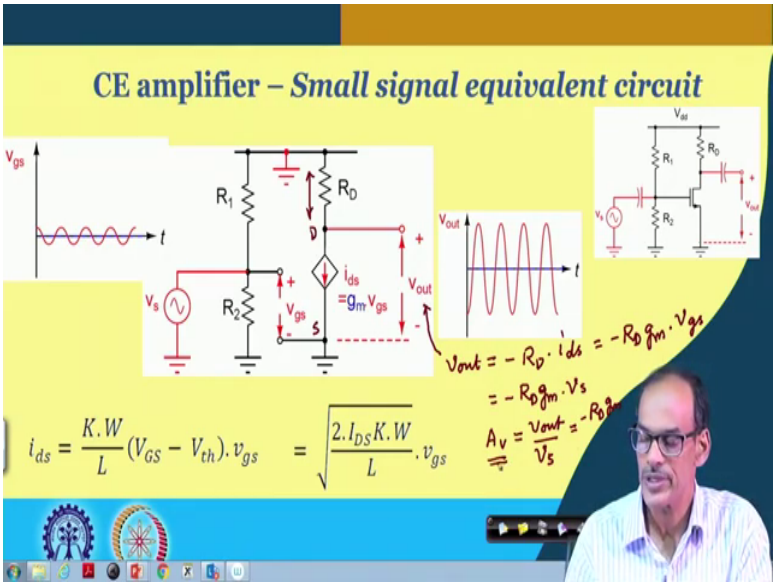

So, at the output we do have only the signal part and if you see this circuit and if you try to analyze this circuit quickly what we are getting let me. So, let me write the expression of this v out, it is v out equals to this what about the drop across this resistance you are getting the current is flowing from drain to source. So, the output voltage it is minus R D minus R D into

i ds and that is given as minus R D into gm into v gs and the v gs it is incidentally same as v s; so, that is equal to minus R D into gm into v s.

So, that gives us the voltage gain A v define as v out small signal v out by the primary input v s equals to minus R D into gm. So, this is the; this is the first parameter of the voltage amplifier namely the voltage gain.

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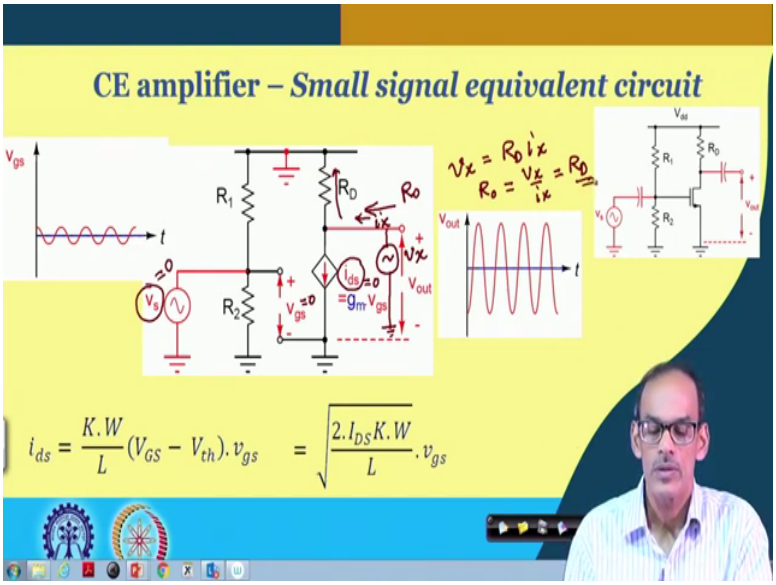

The second parameter it is the output resistance. So, if you look into this circuit and then if you observe this circuit from outside and if you see what is a corresponding output resistance. So, while we will be doing this as we said that we can connect a signal source here and then we have to make this part equals to 0. So, once you make this is equal to 0, this part it is 0. So, that makes this current it is also 0 and then if you stimulate this output port by say v x and then if you observe the corresponding current here as i x.

In fact, the current it is only going through this resistance. So, then v x and the i x relationship you will get is basically v x is equal to R D into i x. So, that gives us the expression of v out which is defined as v x by i x equals to R D; so, that is the second parameter we obtained.

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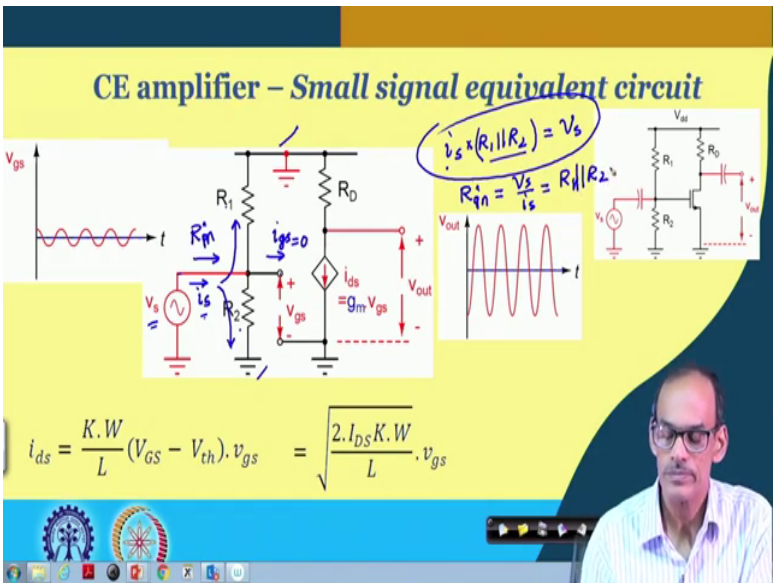

Now, the third parameter it is; so, at the input port if we see and if you see what is the corresponding resistance here. And, since the circuit here it is open namely the gate current is 0 whether it is large signal or small signal as long as we are not considering the effect of the capacitance from gate to source we can assume that this is equal to 0.

So, if we again stimulate this port by say v s and whatever the current we observe let you say that this is i s. And, this is incidentally it is the current flowing through this R 1 and R 2. In other words we can say that i s multiplied by R 1 parallel R 2 because this is connected to AC

ground, this is anyway it is ground. So, that is why that makes this R 1 and R 2 coming parallel while this is current i s flowing.

So, i s multiplied by this parallel connection that gives us the voltage there which is v s or we can say that i s equals to v s divided by parallel connection of this one. But, whatever it is that gives us the expression of i sorry i in sorry this will be in that is what I mean i in equals to v s divided by i s. So, that is equal to R 1 in parallel with R 2.

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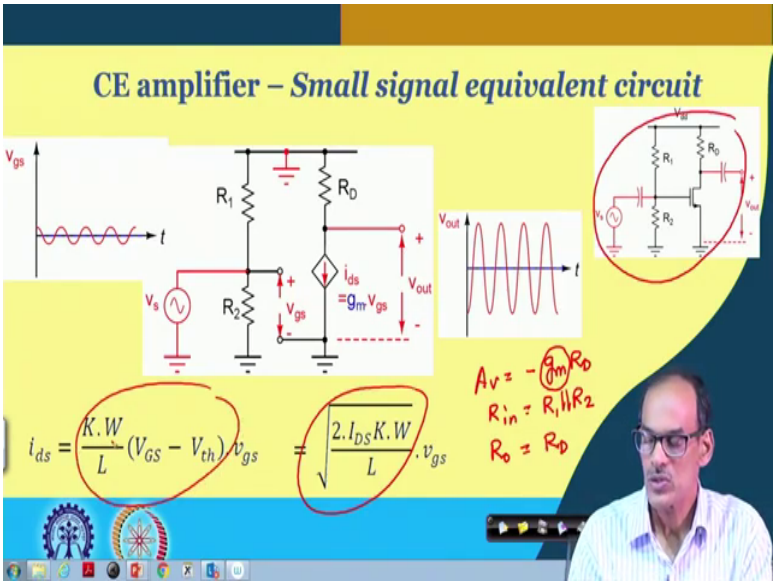

So, what do you obtain here it is A v expression of A v equals to minus g m into R D R in equals to R 1 parallel R 2; it is coming from the bias circuit and then output resistance equal to R D. So, that is how the entire circuit you can map into this voltage model. So, and the of course, the expression of this g m it is given here either here or here.

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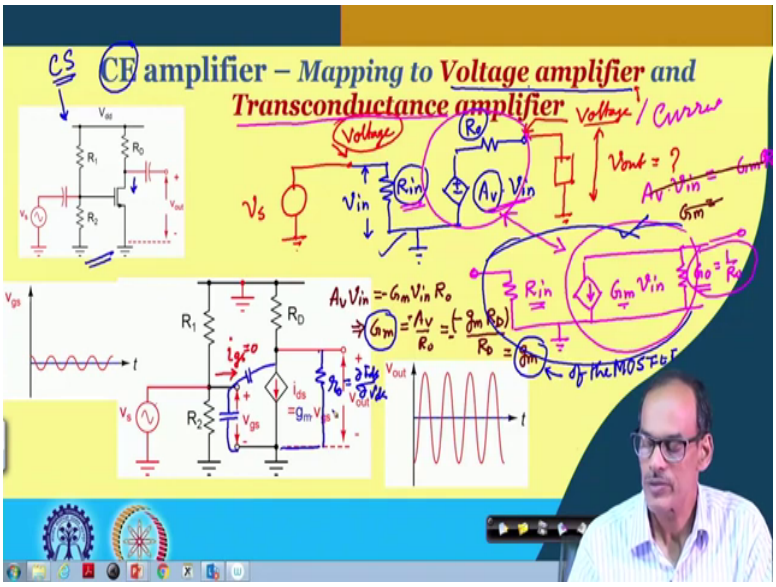

So, as a result what we are getting there it is once we map the circuit into a voltage amplifier what we are going to get here it is we do have R in then A v. So, this is A v times so, this side plus and this is minus A v times v in, where v in it is the voltage across the input port and then at the output we do have the Thevenin equivalent output port resistance R o so, that is the voltage model and we already obtained the expression of A v R o and R in.

And then of course, from outside if we are giving a stimulus say v s and then if you are connecting some load here then you can find the corresponding primary input to primary output voltage. Now, as we have given a hint that since the main circuit this current it is this i gs equals to 0 before we start considering the input capacitance.

So, we can say that the signal at this input port it will be always in the form of voltage. On the other hand the output port at the output port at the signal either can be voltage as we are showing here, but then it can be even current also.

I have a call now; I am going to restart. So, what we are discussing here it is the bolt at the signal at this point it can be either voltage and then we call it is voltage amplifier or it can be current. So, or it can be current and if it is current then the corresponding amplifier it will be called trans conductance amplifier. And, what may be the corresponding model?

At the input it remains the same namely R in, but at the outputs will be having different model. This is G m into v in, note that this G m it is in incidentally it may be same as the small gm that is the trans conductance of the device, but in general need not be the same.

And, at the output side we do have a not an equivalent resistance or say conductance output conductance G 0 which is equal to 1 by R 0. Now, these two circuits of course, they are equivalent. So, this R in and this R in they are same whereas, this G m and this A v must be having some relationship. So, that this circuit and this circuit they are equivalent, namely this Thevenin equivalent signal source need to be converted into Norton equivalent source here.

So, this G naught relationship of G naught and R naught it is already given here. On the other hand whenever the circuit is open and we are getting the voltage here it is same as the internal voltage which means that A v into v in that must be same as whatever the voltage it is getting developed here. Namely, this should be equal to minus G m into G into R naught.

So, that gives us expression of G m equals to sorry G m into v in into this one. So, let me rewrite this part, somehow here; so, A v into v in so, that is the open loop sorry open output voltage. So, that should be equals to G m into v in into R o with a minus sign so, that gives us the expression or the relationship between this G m and this A v.

So, G m equals to A v by R naught and of course, with a minus sign here and what we have seen that A v it is minus g into R D and R o it was R D, A v the minus sign. So, we do have

one minus sign here and then also we do have one more minus sign here. So, that gives us g m of the device; so, incidentally as I said that incidentally this G m it is same as this g m of the transistor of the MOS transistor, but in general it need not be.

So, that is how now the amplifier sorry this is there is a small mistake, this should be common source amplifier. So, there is the common source amplifier. So, that is how common source amplifier we can either map into a voltage amplifier which is given here or it can be mapped into this trans conductance amplifier.

Now, if we consider the high frequency situation; namely if we consider the signal you are feeding here it is in the high frequency range; then we need to consider parasitic capacitances here. Gate to source and then gate to drain capacitances and if you want to also include the effect of lambda, then at the output side it may be having finite conductance. So, we may have to include the output conductance also which is defined as which is denoted as R o and defined as change in I ds with respect to change in v ds.

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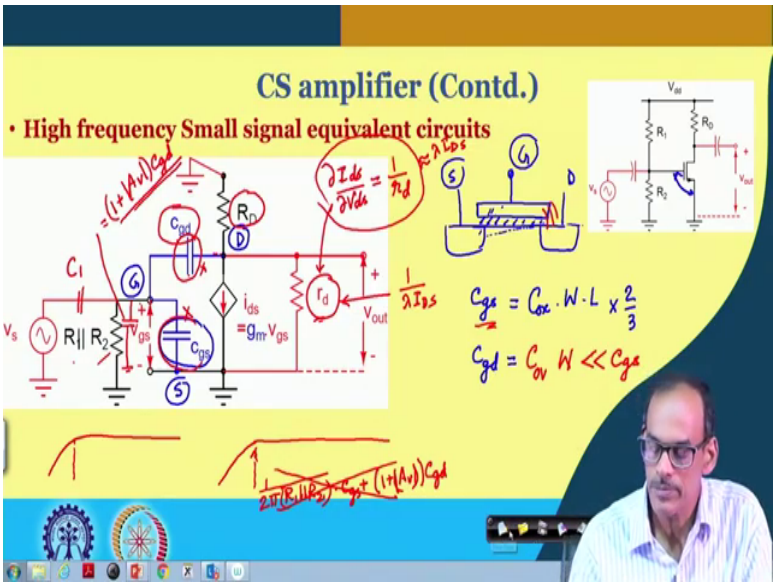

So, if you see the corresponding model; so, what we will be getting there it is. So, this is the high frequency model we can see that if we consider the device parasitics what are the components we do have it is, we do have the gate to source capacitance, this is the gate terminal and then this is the source terminal and this is the drain.

So, gate to source we do have one capacitance internally and that is coming from basically the this if you see if you recall the MOS structure; it is simplified cross sectional view and this is where we do have the thin oxide. And, here we may be having the channel; so, this c gs is primarily due to this capacitance. So, this is source and this is gate terminal and this is the drain terminal.

So, c gs is this capacitance which is C ox capacitance per unit top view multiplied by W into L and since it is in saturation you need to consider one factor two-third. And, on the other

hand if the device it is in saturation region we can say that the whatever the fringe capacitance will be there that is primarily contributing the c gd. So, there may be some fringe or overlap capacitance and that capacitance is proportional with W. So, this is something called another parameter called C overlap multiplied by W and typically this is much smaller than c gs.

So, I should say magnitude wise this is dominating individually over this c gd; however, this c gd it is at this end it is not; it is not AC ground rather it is having a signal. So, in case if we are thinking of the small signal capacitance and if we translate this equivalent this capacitance into an equivalent capacitance from input port to ground then we need to consider Miller effect.

So, the effect of this part c gs c gd at the input port it may be translated as equivalent another capacitance. And, the this is due to the c gd and it is equals to 1 plus this gain of the voltage gain of this circuit into this I should say magnitude wise c gd. So, we will be discussing this again later, but this is coming from the Miller's theorem and it is referred as Miller affected capacitance. In addition to that we are considering this r d into source resistance r d or r ds and this is coming due to I ds is having some dependency on v ds.

So, if I say that change in I ds with respect to v ds; so, that is the output conductance or we can say 1 by output resistance and the expression here it is typically it is approximately rather this is equal to lambda into I DS. So, that gives us this is equal to 1 by lambda into I DS.

So, this model as I said this model it is giving us the high frequency model and whenever we will be talking about frequency response of the circuit; in the mid frequency region we may ignore these two parts. And, whatever the in case if it is a resistive load then we may ignore this part and then we may get the mid frequency gain.

But, if you go to say higher and lower frequency depending on the coupling capacitance here and depending on the resistance here we may be having the lower cutoff frequency defined by the C 1 and R 2 parallel R 2. So, this lower cutoff frequency it is 1 by 2 pi this R 1 parallel R 2 into the input capacitance and input capacitance is c gs plus the effect of the c gd which is 1

plus A v times c gd sorry sorry; I will take it back I will take it back. So, the lower cutoff frequency it is defined by let me rewrite here the.

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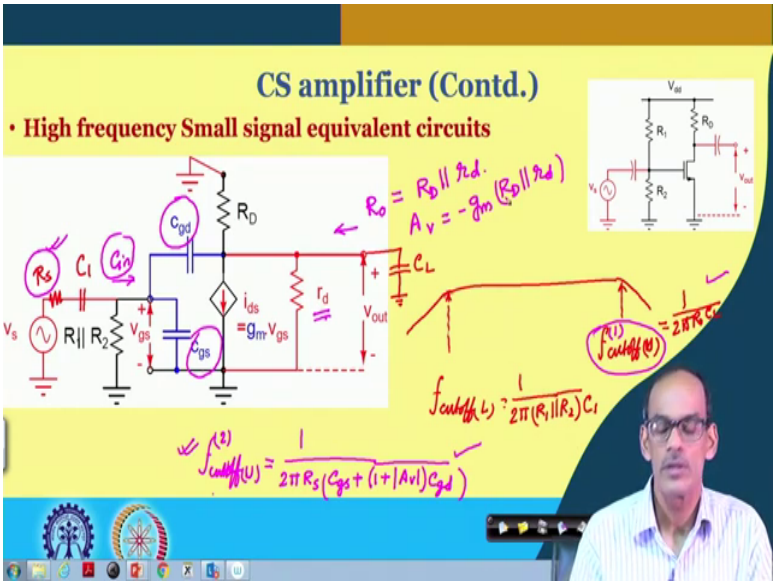

So far we are talking about the high frequency effect and the low frequency effect. So, as a result the previous analysis it was valid in the mid frequency region. And, if you go to lower and lower frequency, the lower cutoff frequency it will be defined by f cutoff low equals to 1 by 2 pi R 1 parallel R 2 into C 1, where C 1 it is the signal coupling capacitor C 1.

On the other hand whenever we are going to higher and higher frequency we will be having upper cutoff frequency here and that cutoff frequency it will be upper cutoff frequency U here. So, that is 1 by 2 pi R o and then C L C L we are assuming that to be coming from the next stage or maybe whatever the load we do have.

And, in case if we have the signal source having a source resistance say R s and then in the high frequency the upper cutoff frequency may be having one more possible candidate to define this cutoff frequency, in case if we have this R s. And, then if cutoff frequency upper cut off frequency in presence of this R s, it is 1 by 2 pi into R s into the input capacitance c in and then c in it is having; so, this c in it is having two part.

One is c gs another part is contribution from the c gd. So, this R s multiplied by c gs plus Miller affected part of the c gd namely 1 plus magnitude of A v into c gd; so, that is the input capacitance. So, based on the magnitude here this one, if I call say this is f upper cut off frequency 1 and this is f upper cutoff frequency is 2, then whichever is the minimum we have to consider either this one or this one.

So, that is the role of this c gs and c gd in the frequency response and for high frequency analysis we must consider these two capacitors. And, on the other hand r d in case if you consider the output resistance here including this r d then the output resistance R o it will be R D coming in parallel with small r d.

And, the gain on the other hand the voltage gain it will be minus g m into this total resistance which is R capital D in parallel with small r d ok. Now, so we have discussed about the mapping to small signal equivalent circuit and then biasing and all more from the analysis point of view.

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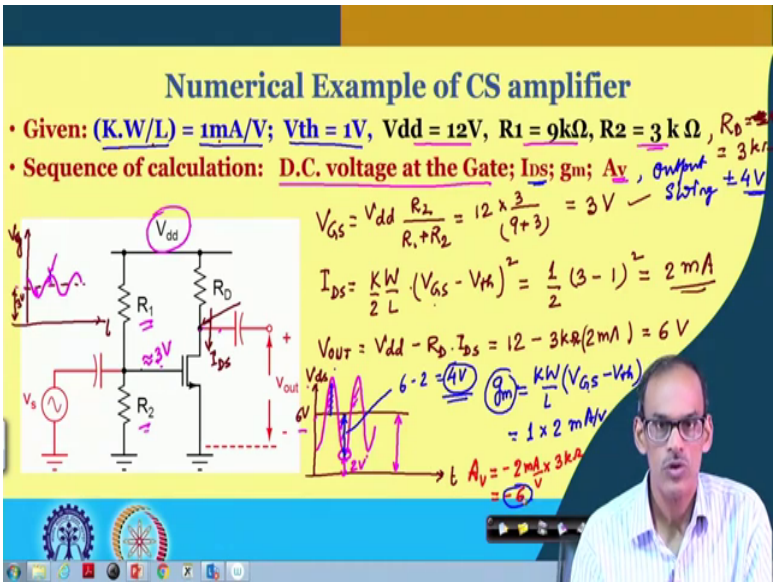

So, let me cover one numerical problem I think I do have I do have separate slide for that yes. The same circuit here we are considering and also we have been given this parameters that K into W by L equals to 1 milliampere per volt; suppose it is given to us. And, then threshold voltage of the transistor is say 1 volt. And, on the other hand the DC parameters are rather bias circuit information it is given as that V dd it is say 12 volt and then R 1 it is; so, 9 k and R 2 it is 3 k.

So, how do you then find the gain, how do you find the gain of the circuit and or from this information. So, what will be the procedure or sequence of calculation? First thing is the DC operating point and to do that we need to get the DC voltage at the gate or gate to source. So, if you consider this R 1 and R 2 value and then this is V dd equals to 12 volt what we are

getting is V G equals to V dd into R 2 divided by R 1 plus R 2. So, that gives us 12 into 3 divided by 9 plus 3; so, that gives us 3 volt.

In fact, this is same as V GS so, V GS is equal to 3 volt here. Now, using this information I can say that I DS which is K W by L and also 2 in the denominator V GS minus V th square. So, that gives us K into W by L it is 1 milliampere by 2 then 3 volt is the V GS minus V th square. So, that gives us 2 milliampere of quiescent current I DS.

So, the quiescent current flowing through the circuit I DS it is 2 milliampere and the value of this R D ok; I think the value of the R D we also need to find the operating point. Anyway let me consider that R D is also say 3 k and so, if this R D is equal to 3 k then V out V out equals to V dd minus R D into I DS.

So, that is equal to 12 volt minus R D it is 3 k into 2 milliampere so, that gives us 6 volt. So, the DC voltage here it is 6 volt. So, at the input so, at the input what you are getting here it is 3 volt DC here. So, this is 3 volt, I should say capital V small gs and on the other hand at the output we are getting DC voltage it is 6 volt.

So, this is V ds and then what is the value of the g m? Now, to calculate the gm it is so, we obtain I DS we obtained V out; now next thing is the g m. So, if you recall the expression of the gm it is K W by L into V GS minus V th right.

So, that is k is given as 1 milli so, multiplied by V GS minus V th; so, 1 into this is 2 3 minus 1; so, 2 milliampere per volt. So, the gm it is 2 milliampere per volt; so, the gain voltage gain A v. So, that gives us A v equals to minus g m which is 2 milliampere per volt multiplied by this R D which is 3 kilo ohm.

So, that gives us a gain of only minus 6 of course, this is say 4 gain, but whatever it is we assume that for the time being let you assume that is what we are looking for and that may be sufficient. And so, at the input at the input if we are giving say sinusoidal signal at the output; so, we are expecting that corresponding effect coming here.

So, let us try to see what is the corresponding signal swing we can get or maximum swing we can get. Note that at the input we are giving signal which is say one-sixth of the signal and for the time being if I say that the output or with this V ds variation is much more than whatever the variation we do have at the gate.

And, we do have the 6 volt here and we do have the 3 volt here. So, while it will be going to the valley of course, this may be going to the peak here. And, if I ignore this variation compared to this much of variation then the gate voltage DC gate voltage it is 6 volt and gate voltage sorry drain voltage DC it is 6 volt and then gate voltage it is close to 3.

So, the minimum possible drain voltage we can say that 3 volt minus 1 volt. So, the valley here it can be as low as 2 volt, if I ignore this variation and then the corresponding signal swing from 6 volt to reach to this 2 volt, it is 4 volt 6 minus 2 volt. So, that is what we can say that the output swing it can it can be as high as 4 volt, but in case if we are also considering this variation you need to consider the gate voltage going slightly above. And, based on the magnitude of this gain you can say that the if this is 4 volt the corresponding variation here it is 4 divided by 6.

So, then of course, the device it is just entering into the saturation anyway approximately we can ignore that part and then you can say that the output swing in addition to this the output swing. So, output swing it is plus minus at least lower side we had seeing that this is 4 volt positive side of course, it is not having any problem it can go higher.

And, to get this maximum swing of course, the required voltage at the input it will be and this plus minus 4 volt divided by 6. I think that is what I like to cover and so, let us see what are the things we have covered in today's module.

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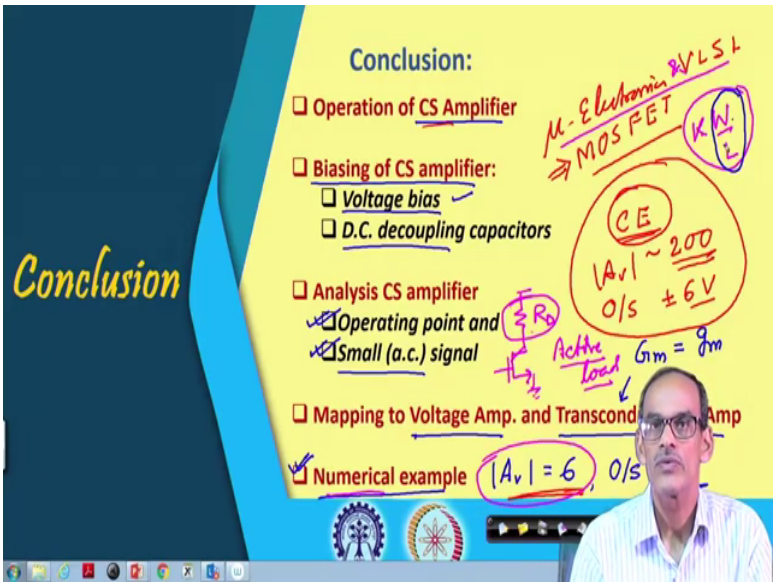

Yes. So, basically to today's primary discussion it was common source amplifier. So, we started with the operation of the circuit and then now we have talked about the biasing of the common source amplifier. Since, the gate voltage gate node is having 0 current we can say that it must be through voltage bias. And, then along with the voltage bias which is it is getting obtained by potential divider R 1 R 2 from the V dd we need to consider signal coupling capacitors at the input port and output port.

And, then we have discussed about the DC operating point analysis; so, we have basically the MOS transistor it has been replaced by equivalent circuit which it is representing the equation I DS in terms of V GS. And, then we have seen the small signal equivalent circuit where the transistor it was replaced by gm into V GS small signal V gs and then we got the expression of the at the output gain.

Then the small signal equivalent circuit after dropping the DC part we have mapped the amplifier into voltage amplifier where the input signal it was voltage and then output also was voltage. The other possibility of mapping the amplifier common source amplifier it is trans conductance amplifier and they are the though the input remains voltage and then output it was in the form of current.

And, in the trans conductance what you have seen is that trans conductance of the amplifier it is incidentally same as trans conductance of this MOS transistor in this case. And, then we have discussed about numerical examples where different biasing arrangements and it was given. And, then what we have seen is that the voltage gain it is quite low, magnitude wise it was we obtained for this numerical example it was only 6. The output swing on the other hand so, output swing we obtained it was plus minus 4 volt approximately.

So, probably for 12 volt supply output swing it is I should say it is lower. Now, if I compare this numerical example of this common source amplifier with the common emitter amplifier performance you may recall that the for common emitter amplifier the voltage gain it was much higher in the range of 200. So, definitely this is higher than the 6 and also the output swing in the common emitter amplifier it was in the range of plus minus 6 volt ah; so, close to plus minus 6 volt.

So, we can say that performance wise common emitter amplifier it is better than the common source amplifier. So, both the gain wise and the output swing wise. Then the natural question is then why do we go for common source amplifier? The answer is that whenever we will be going into micro electronics and VLSI design where MOSFET transistors are they are the primary elements. And, to realize this amplifier voltage amplifier we need to use MOS transistor rather than BJT.

So, I should say that whatever the technology will be it will be available to us and if we integrate analog and digital circuit together, then it is better to explore this common source amplifier. And, in case if we are not happy with this particularly the gain part maybe we can try to use some other alternative.

Namely, instead of using say passive load we need to consider active load, we need to consider active load. So, instead of R D we can use probably active device here or active load. So, in case if we are successfully replacing this one, there is a possibility of improving this gain and practically that is what it is done.

So, probably we will see that down the line whenever the situation permits we will replace this passive load by active load. The other information I like to capture here it is that particularly in the context of micro electronics and VLSI design situation in this numerical example, in today's numerical example we have considered that K into W by L it is given to us.

This is the case whenever we are doing the board level design we assume that this not only this parameter, but also aspect ratio of the channel of the device is given to us. But, when you consider VLSI design the additional flexibility is that the designer can decide what will be W and L. So, in the analog VLSI design W and L will not be given rather it will be the freedom it will be given to the designer. And the designer of course, have to make a meaningful selection of W and L to further optimize the performance of the circuit.

So, whenever we will be going for advanced level subject such as analog VLSI design then we will be dealing with variation of the W and L or rather how do you select W and L of the devices. But, in this subject in analog electronics we assume that this entire quantity namely K into W by L is given to us. And, then we proceed for design namely selecting the different bias components and the load; I think that is what we like to cover.

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Thank you for listening.