

Analog Electronic Circuits
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Lecture – 30
Common Emitter Amplifier (Contd.)
Design Guidelines (Part A)

Hello, so now so, welcome back to this NPTEL online course on Analog Electronic Circuits. This is of course, it is we are having this course for maybe last 2 to 3 weeks, it is continuation of that topic of Common Emitter Amplifier. We have discussed about the theoretical aspect and some of the numerical examples, and in the previous class we could not complete the numerical problems all.

So, today we are discussing some more numerical problems. In fact, in the previous numerical problem we have discussed about, how to find the gain numerically as well as how to analyze the circuit? And, today what will be doing is that in case if we have to design one common emitter amplifier for a given requirement, then how do you proceed and what may be the design guidelines we need to follow. So, that is what will be discussing.

And, also in case if you have see multiple common emitter amplifier cascaded to each other, then how do you find the overall gain? So, these are the two things we do have in mind.

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So, as I said that this is what we are from in fact, we already have covered significant part of the numerical examples. And, particularly the operating point and then the and it is stability and then finding performance matrices. And, today we are going to discuss about the design guidelines.

And, in case if we have say relatively bigger circuit then how do you proceed to analyze that circuit? So, let me skip a number of slides here.

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The slide features a yellow background with a blue header and footer. The title "Design guidelines: CE amplifier - Fixed-bias" is written in red and blue. Below the title, there are two bullet points: "Given: $V_{CC} = 12V$; $\beta = 100$; $V_{BE(on)} \approx 0.6V$;" and "Find: R_C , R_B , C_1 , C_2 ". Below these, it lists "Important performance metrics: A_v , Output swing, d.c. Power, R_{in} , R_o , C_{in} ". A circuit diagram of a common-emitter amplifier is shown, with a BJT transistor, a base resistor R_B , a collector resistor R_C , a collector load capacitor C_L , an input capacitor C_1 , and an output capacitor C_2 . A signal source V_s is connected to the input, and the output voltage V_{out} is taken across the load capacitor. A video feed of a man in a light blue shirt is visible in the bottom right corner of the slide.

So, we have covered these numerical problems the CE amplifier and then this is where we are going to discuss the design guidelines of common emitter amplifier. And, so, we are going to discuss detail about the design guidelines of common emitter amplifier. And, in case if the topology is fixed and if it is decided to be fixed by us topology.

And, then how do you proceed first thing is that we are assuming that these informations are available particularly the supply voltage it is given to us. Typically and the supply voltage it is given by the customer who requires this circuit. And, also this information may be available particularly, whether the BJT is silicon type or germanium BJT. Based on that we can decide what is the V_{BE} on of the device? And, also we are assuming that the beta of the transistor it is measured and may be 100 or 200 or whatever it is.

So, we assume that these 3 informations are given to us. Whenever then whenever we are talking about we have to design, what do we mean by designing is that finding the value of this bias registers and also these 2 capacitors C_1 and C_2 . So, our main task is to find the value of this bias components as well as some guidelines of how to select the value of C_1 and C_2 .

And, of course, the requirement here probably it will be in terms of the gain of the circuit and then the output swing, of the circuit namely what may be the available voltage here or available voltage here without having significant distortion and that is of course, very much important thing. And, then the power dissipation of the circuit. Namely, if the supply voltage is given to us next thing is that the power dissipation it will be decided by how much the quiescent current is flowing through the transistor I_C and I_B .

So, we can say that I_B and I_C predominantly I_C sorry I_C is defining the total current. So, we can say that in the power dissipation it is essentially means that, the value of the collector current. And, then the additional information it may be required is that what may be the input resistance of the circuit, small signal or large signal input resistance, then output resistance of the amplifier and then what may be the input capacitance C_{in} ?

So, input capacitance probably we can skip that part for the time being, but just to say that to calculate this C_{in} or to get some information about C_{in} , we require additional information from the device data set is that C_{π} and C_{μ} .

So, from that we can calculate the what will be the C_{in} ? So, as I said that may be in the we will skip this part, because this C_{μ} it is contribution to C_{in} it is through Miller effect. So, we get to cover that Miller effect whenever will be covering that we will discuss about this part.

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Design guidelines: CE amplifier – Fixed-bias

- Given: $V_{CC} = 12V$; $\beta = 100$; $V_{BE(on)} \approx 0.6V$;
- Find: R_C, R_B, C_1, C_2

Important performance metrics: A_v , Output swing, d.c. Power, R_{in} , R_o , C_{in}

Handwritten notes and equations:

- $|A_v| = g_m R_C = \frac{I_C \times R_C}{V_T} = \frac{V_{RC}}{V_T} < \frac{V_{CC} - V_{CE(sat)}}{2 \cdot V_T}$
- $|A_v|_{max} = \frac{12}{2 \times 0.026} = \frac{460}{2} \approx 230$
- $V_{CE(sat)} \approx 0.3V$
- $V_{RC} \approx \frac{V_{CC}}{2}, I_C = \frac{P.D}{V_{CC} - V_{BE}}$
- $R_C = \frac{V_{RC}}{I_C}, R_B = \frac{V_{CC}}{\beta I_C}$
- $R_{in} = \frac{100}{\beta} \approx 2 \Omega$

So, then what we are talking about that finding this components based on predominantly from these informations. Now, if you see the voltage gain of the common emitter amplifier A_v , we have discussed that it is magnitude it is g_m into R_C . And, the g_m it is and the quiescent current I_C divided by thermal equivalent voltage V_T . So, this multiplied by R_C what it is giving us that voltage drop D C wise voltage drop across this resistance R_C divided by V_T .

Now, of course, this upper limit of the drop across this resistance it is defined by this V_{CC} . So, it is hard limit is V_{CC} divided by V_T . So, we cannot get gain higher than this one. So, definitely I should say this is higher limit. And, in fact, if you consider drop across this resistance is V_{CC} then the required voltage here it is or rather the voltage here to be 0.

So; obviously, if we make this voltage 0 then output signal swing it will be getting affected. So, this is just to say numerical limit of the gain. Practically, you know if we have to consider

output swing and to consider the output swing you may recall the load line and then device characteristic and the operating point.

So, I_C versus V_{CE} characteristic curve of the device is say like this, then we do have the load line, which is defined by this V_{CC} point here and then the current here or which is V_{CC} divided by R_C . And, this is the operating point. So, lower side we do have a limit of the V_{CE} or output voltage it is $V_{CE\text{ sat}}$. So, this $V_{C\text{ sat}}$ again of course, it depends on the device..

Typically, in the order of say 0.2 or 0.3 volt and then we do have V_{CC} . So, over this limit the V_{CE} voltage or the V_{out} voltage it will be flying. As we are applying signal here the corresponding voltage here it will be flying over this range.

Now, to have a meaningful swing of the signal from this with respect to this quiescent point lower side and upper side, it is better to set this quiescent point at the middle. So, I should say that if the quiescent point it is set at the middle, then we can say drop across this resistance R_C instead of this the it is limit it should be rather V_{CC} minus $V_{CE\text{ sat}}$ divided by 2 and then of course, we have the V_T .

So, I should say this is the upper limit of the voltage gain giving importance to the output swing. And, in this case if I say that $V_{C\text{ sat}}$ is very small and then we can say that upper limit of the voltage gain, we can practically you can say this is 12 volt divided by 2 into V_T is 0.026 right.

So, that gives us upper limit how much this may be 4 around 460 something. So, beyond this definitely we cannot get the voltage gain. Let me check whether the numerical value, we obtain for this upper limit is this for 61 fine, 461 is the upper limit, but it is fine. So, based on this information and of course, if we do so, the output swing, this output swing it is becoming V_{CC} approximately V_{CC} by 2 plus minus with respect to the quiescent point, ignoring of course, this $V_{C\text{ sat}}$ assuming this is very small.

So, yes though we do have good swing and then we can have a very decent gain here and this is 6.6 divided by 2.2×10^4 sorry this by 2 rather. So, it is in the order of 231 or so yeah around 230 ok. So, now to get this 230 again, what you have to do that drop across this resistance is we are allocating this voltage drop close to V_{CC} by 2 . Now, next thing is that the power dissipation. So, based on this power dissipation information given to us, we can find the value of this current, because we can say this power dissipation it is approximately equal to V_{CC} multiplied by I_C quiescent current of the collector terminal.

So, if the power dissipation is given to us since we know this V_{CC} . So, from that we can find what will be the corresponding I_C ?. So, then if I know this I_C , if I know the drop across this V_{RC} equals to V_{CC} by 2 then I can find what will be the R_C ?.

So, what is the sequence of finding different parameters, first of all we can set the drop across this R_C , in the order of or very close to V_{CC} by 2 , that will be giving us good gain as well as output swing. Note that our target probably the again it is not specified it may be say that the gain may be as high as possible and for that to make a balance between this gain and output swing we can take this one.

So, the first thing is that a drop across this one we can take half of the supply voltage. And, then from power dissipation we can find what will be the current quiescent current. So, that is the power dissipation divided by V_{CC} . So, then next thing is that we can find the value of R_C which is of course, V_{RC} divided by I_C .

And, then from the information of the beta we can find what will be the I_B and from that we can calculate what will be the R_B . R_B equals to V_{CC} minus V_{BE} on divided by I_B and I_B it is I_C divided by the beta. So, from that we can find what will be the value of this element. In fact, this voltage drop it is very close to 0.6 .

So, in you may ignore even 0.6 for approximate calculation with respect to 12 volt and that gives you the value of R_B . And, from that we obtained the R_B and R_C and to find the coupling capacitor a signal coupling capacitor or d c, d e coupling capacitor say C_1 . We need

to find what is the input resistance R_{in} and you may recall in our previous example. So, if the collector current it was in the order of you know it was 2 milliamperes.

So, the corresponding R_{in} it was. So, R_{in} it was r_{π} in parallel with R_B , which is approximately equals to r_{π} and r_{π} equals to β/g_m , which is say 100 divided by g_m . So, from that you can of course, the g_m we know. So, once we obtain say $R_C R_B$ then we can find the corresponding r_{π} . And, then r_{π} gives us the input resistance R_{in} and from that we can calculate this C_1 , because the depending on this value of this R and C or time constant, we can find the we can get the lower cutoff frequency.

So, to be more precise to get meaningful value of this C_1 , we require additional information about the performance requirement, namely the lower cutoff frequency. So, if I know that if f_L lower cutoff frequency from that we can say that what will be the C_1 . So, let me consider that this parts are given to us next thing is that how do we find the C_1 ? So, let me clear it and then we assume that I_C it is known to us.

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Design guidelines: CE amplifier – Fixed-bias

- **Given:** $V_{cc} = 12V$; $\beta = 100$; $V_{BE(on)} \approx 0.6V$;
- **Find:** R_c, R_B, C_1, C_2

Important performance metrics: A_v , Output swing, d.c. Power, R_{in} , R_o , C_{in}

$$R_{in} = r_{\pi} = \frac{\beta \times V_T}{I_C} = \frac{100 \times 26}{1} = 2.6 \text{ k}\Omega$$

$$f_{cut-off(L)} = \frac{1}{2\pi R_{in} C_1}$$

$$\Rightarrow C_1 = \frac{1}{2\pi R_{in} f_{cut-off(L)}} = \frac{1}{2\pi \times 2.6 \times 50 \times 1000}$$

$$= \frac{10^{-5}}{2.6\pi} = \frac{10 \times 10^{-6}}{2.6\pi} \sim 1 \mu F$$

Then, R_{in} is approximately equal to r_{π} which is β divided by g_m which is I_C divided by V_T . And, if I consider I_C is say 1 milliamperere as a special case or one case and β is say 100. So, from that we can say that β multiplied by 26 millivolt divided by 1 milliamperere. So, this gives us 2.6 k all right.

And, the lower cutoff frequency $f_{cut-off(L)}$ equals to $\frac{1}{2\pi R_{in} C_1}$, where C_1 is this one. Now, if I consider this value of this R_{in} . So, from that we can see or we can rearrange this equation saying that C_1 equals to $\frac{1}{2\pi R_{in} f_{cut-off(L)}}$. And, suppose this R_{in} is say around 25 or 26 k and say lower cutoff frequency is a say 50 Hertz. So, then what may be the value of this C_1 ? Let us see $\frac{1}{2\pi R_{in} f_{cut-off(L)}}$ is $\frac{1}{2\pi \times 2.6 \times 50}$. So, k is 1000 you have to write here yes.

So, we do have 100 here. So, this is 10^5 divided by 2.6π or you can say that this is 10^6 divided by 2.6π into 10^6 farad, or you can say in the order of say micro farad to get a lower cutoff frequency of 50 Hertz. So, that gives you an idea that for a typical example case the C_1 should be in the order of micro farad.

In fact, the other coupling capacitor may be in the same order assuming that this resistance and input resistance there and also the output resistance here coming from the next stage, or I should say the input resistance of the next stage is may be in the same order of this input resistance. And, hence we can say that C_2 it is also in the order of C_1 .

So, what we have done here it is that we got guidelines that, how to design this C amplifier to get a decent performance? Namely, the gain here it is whatever the 20 around 230 and then output swing it is around plus minus 6 volt. And, then power dissipation for say 1 milliamperere of current here it is 1 milliamperere and 12. So, in the order of or close to 12 milli Watt ok.

And, the cutoff frequency $f_{cut\ off}$ particularly lower cut off frequency is equal to 50 Hertz right, for that at least we learn how to design the circuit. Let us see the similar kind of guidelines can be followed for CE amplifier with self-bias circuit.

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Design guidelines: CE amplifier –Self-bias

- **Given:** $V_{CC} = 12V$; $\beta = 100$; $V_{BE(on)} \approx 0.6V$;
- **Find:** $R_C, R_1, R_2, R_E, C_1, C_2, C_E$

Important performance metrics: A_v , Output swing, d.c. Power, R_{in} , R_o , C_{in}

$$V_{out} \approx \frac{\{V_{CC} - V_E\} - V_{CE(sat)}}{2} \leftarrow \pm \frac{10 - 0.3}{2} \approx \pm 5V$$

$$I_C \approx I_E = \left\{ \frac{V_{BB} - V_{BE(on)}}{R_E} \right\} \quad \text{for } (R_1 || R_2) \ll (1 + \beta) R_E$$

$$V_E \begin{matrix} 1 \rightarrow 2V \\ 0.5 \rightarrow 3V \end{matrix}$$

So, here we do have self-bias and here again we are assuming that these informations are given to us namely, the supply voltage is given to us V_{BE} on it is coming from the data set, the beta also may be coming from the datasheet or it may be you can use multi meter or by some other means to find the value of beta.

So, here we are assuming that this informations are is given to us, we need to find the value of different components namely the resistances here and the capacitor. So, we do have the C_1 C_2 and in addition to that this bypass emitter bypass capacitor C_E . And, here of course, we do have the important informations are like this power dissipation also. And, maybe the lower cutoff frequency, if you if this information is provided then it will be better to find the value of this C_1 , C_2 and in fact, C_E you also.

Now, compared to the previous circuit they approach it will be similar, but you need to understand that the entire V_{CC} voltage it is not available for this collector. So, we do have V_{CE} requirement, $V_{CE\ sat}$ minimum $V_{CE\ sat}$ requirement lower side, in addition to that there is a voltage $d\ c$ voltage require there. Note that while we are connecting the $C\ E$ and if we are applying a signal here the voltage here it will be $d\ c$.

So, this $d\ c$ voltage it depends on how much the value of this $R\ E$ we are taking and how much the current emitter current or collector current is flowing through the device. Now, since the voltage drop at this node, it is restricting the limit of this collector voltage of the transistor, then definitely higher the emitter voltage will get lower swing.

So, I should say now the available voltage for output signal it is V_{CC} minus $V\ E$ emitter voltage divided by. So, this is the; this is the voltage of course, I need to consider the other part also $V_{CE\ sat}$. And, then this is the entire swing available to us that divided by 2 may be the possible signal swing. So, plus minus this is the swing.

Now, if I take higher value of this $V\ E$ and that reduces the swing. On the other hand if I reduce this voltage at this node, which means that the value of this $R\ E$ it is also getting reduced and then you may recall that the role of this $R\ E$, namely the collector current expression it is V_{BB} minus V_{BE} on divided by the I should say not collected a to be more precise the emitter current, divided by this $R\ E$.

And, here the assumption is that, assumption is that, $R\ 1$ parallel $R\ 2$, which you call R_{BB} it is much smaller than $1 + \beta$ into $R\ E$. So, earlier we have discussed this part. And, we may of course, we can we may approximate this is very close to $I\ C$. So, why we are looking for this, because we like to make the quiescent point independent of β ?

So, if I satisfy this condition then we can say that this is independent of β . And to achieve this one I cannot take this $R\ E$ small, if I take $R\ E$ small that will reduce this R_{BB} . So, this is R_{BB} that in turn it will reduce this input resistance, because R_{BB} it is coming in parallel

with whatever r_{pi} you do have. So, if this resistance is smaller for a given value of C_1 the lower cutoff frequency it will be affected.

And, moreover there will be a d c current, if I reduce the value of this R_1 and R_2 then there will be d c current flow and that may increase the power dissipation. So, these 2 are having some trade off the namely the output swing and the value of this R_{E2} , which is playing the role to stabilize the operating point. And, the thumb rule it is that typically if the supply voltage is say 12 volt, the emitter voltage V_{dc} emitter voltage we can take in the order of 1 to 2 volts.

So, the this does not mean that if you violate this range you may be having severe problem, sometimes we may go lower side even 0.5 volt it may be going towards even 3 volt, but we suggest that may be this may be a good choice. So, we can decide on this one. And, then if we have say 12 volt supply. So, from that if I use say if you use say this is the emitter voltage. So, then the output swing it becomes $10 - 0.3$ divided by 2 approximately it is plus minus 5 volt that is fairly good.

So, once we decide that the output swing we want it should be 5 volt this is a 2 volt, then naturally the drop across this resistance it is also getting fixed, because this is the we like to say this operating point almost at the middle. So, ignoring this $V_{C sat}$ part compared to $12 - 2 = 10$ volt, we can say that this voltage in it may be 5 volt.

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Design guidelines: CE amplifier –Self-bias

- Given: $V_{cc} = 12V$; $\beta = 100$; $V_{BE(on)} \approx 0.6V$;
- Find: $R_C, R_1, R_2, R_E, C_1, C_2, C_E$

Important performance metrics: A_v , Output swing, **d.c. Power**, R_{in} , R_o , C_{in}

$V_E = 2V, V_{RC} = 5V$
 $I_C = \frac{P.D}{V_{cc}}, I_E \approx I_C$
 $R_C = \frac{V_{RC}}{I_C}, R_E = \frac{V_E}{I_E}$
 $R_{BB} = \frac{R_1 R_2}{R_1 + R_2} \leq \frac{(11*10)}{10}$
 $\frac{R_2}{R_1 + R_2} \approx V_{cc} \approx V_E + V_{BE(on)} = 2.6V$
 $1 + \frac{R_1}{R_2} = \frac{V_{cc}}{2.6} = \frac{12}{2.6}$

So, that gives us 2 information; the first of all the V_E , we are suggesting to take in the range of 1 to 2 volt as an example if I take say 2 volt, then V_{RC} drop across this resistance R_C . So, that is 10 divided 10 minus 2 minus 0.3 by 2. So, we can say that this is also in the order of say 5 volt and then next thing is that the power dissipation.

So, typically whatever the current it will be flowing here I_C the current base current it will be 2 order magnitude lower and we like to take this current may be in the order of one order magnitude higher than the I_B . So, still this current the current flowing through the bias circuit lower much lower than this I_C . So, the power dissipation still it may be considered as it is getting dominated by V_{CC} and I_{EC} .

So, from the power dissipation we can find what will be the value of this I_C . And, that is the 12 divided by sorry then this will be power dissipation divided by the 12 volt V_{CC} ok. So,

once we have emitter voltage the voltage drop across R_C and then I_C which is also approximately equal to I_E so.

Now, we can directly get the value of R_C and R_E . So, V_{RC} divided by I_C and R_E equals to V_E divided by I_E ok. So, now, we obtain this to next thing is that these 2 resistances R_1 and R_2 should be such that, the voltage coming here it should be consistent with the require 2 volt here. So, we want this voltage drop here which is R_2 divided by R_1 plus R_2 multiplied by V_{CC} .

So, that is the d c voltage here before we connect the transistor base. So, we can approximate that this voltage it will be very close to whatever the require voltage here, which is the emitter voltage plus V_{BE} on namely in this case this is 2.6 volt.

So, from that we can say that the R_1 R_2 ratio can be obtained right. In other words you can say that 1 plus R_1 divided by R_2 equals to V_{CC} divided by 2.6 12 divided by 2.6 . So, that gives us the ratio of R_1 and R_2 . So, either from this ratio and this information you can get the value of R_1 and R_2 or we can use the other the additional information we have discussed that R_{BB} , which is equal to R_1 in parallel with R_2 , this should be much lower than one plus beta into R_E , R_E we already obtained.

And, typically we can see that this is less than or equal to $1/10$ th of this. So, using this guidelines this is R_E . So, using these guidelines and the information we obtain here we can find the value of R_1 R_2 . So, now we obtain all the bias registers, next thing is that the C_1 . So, if you see the input capacitance of this circuit it is in case C_E it is dominating. So, for the signal the input resistance it will be the R_1 , parallel R_2 in parallel with the R_{π} . So, this circuit is having input resistance of R_{π} .

So, from that we can get the R_{in} . Now, similar to the fixed bias circuit we can find the expression of C_1 equals 2.1 by $2\pi R_{in}$, then the cutoff frequency, lower cutoff frequency. And so, for a give for the value of this for a given value of this lower cutoff frequency and then R_{in} . Since, this resistance may be in the order of r_{π} , again this register the value of this

capacitor C 1, it may be similar to whatever previously discussed value of the C 1. So, again this may be in the order of micro farad.

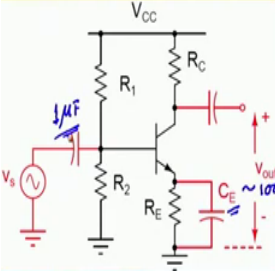
So, likewise the C 2 also it will be in the same order of C 1. Whereas, this C E, it will be having another role to play to define the lower cutoff frequency. And, the lower cutoff frequency decided or defined by this C E, it is coming from the 1 by g m of this device, because this capacitor it will be seeing the resistance of this circuit which is combination of R E and 1 by g m coming from the transistors looking into the emitter. So, the C E on the other hand it can be defined by that and its expression it will be similar.

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Design guidelines: CE amplifier –Self-bias

- **Given:** $V_{CC} = 12V$; $\beta = 100$; $V_{BE(on)} \approx 0.6V$;
- **Find:** R_C , R_1 , R_2 , R_E , C_1 , C_2 , C_E

Important performance metrics: A_v , Output swing, d.c. Power, R_{in} , R_o , C_{in}



$$C_E = \frac{1}{2\pi f_{cutoff(L)} \left(\frac{1}{g_m} \right)}$$

$$= \frac{1}{2\pi \times 26 \times f_{cutoff(L)}}$$

$$= \frac{1}{2\pi \times 26 \times 50} = \frac{10^{-3}}{2\pi \times 26} \sim 100 \mu F$$

$I_C = 1mA$
 $g_m = \frac{1}{26}$

So, let me clear and then write it about the expression of C E need to be followed. So, C E it is 1 by 2 pi then the f lower cutoff frequency, and then of course, the resistance which is 1 by g m of the transistor. So, we have seen that this 1 by g m it is for say 1 milliampere of current

1 by g_m it will be the resistance is very small. As an example here if I consider I_C equals to say 1 milliamper, then g_m equals to it is 1 by 26, because thermal equivalent voltage it is 26 millivolt.

So, that gives us with this information the expression the C_E , it is 1 by 2π then g_m it is 1 by g_m it is. So, g_m we do have here yes so, into 26 into f cut off all right. And, you can see here in case if I am looking for lower cutoff frequency of say 50 Hertz, then this will be 1 by 2π into 26 into 50.

So, we can write this as 10 to the power minus 3 divided by 2, then you know this is π then 2.6. So, it is almost in the order of milli farad. So, we can say that this may be coming in the range of milli farad; no it will be 100s of micro farad 100s of micro farad ok.

So, what I like to say that in case if this capacitor value it is in the order of 1 micro farad to support say 50 Hertz, then the required capacitor here capacitance of the C_E , it is 100 micro farad. So, the value of this capacitance it will be much higher than this C_1 and C_2 to get the same lower cutoff frequency. So, that is about the overall design guidelines. Let me take a short break and then again will be coming back to cover maybe a little different aspect of the design guidelines.

Thank you.