

Analog Electronic Circuits
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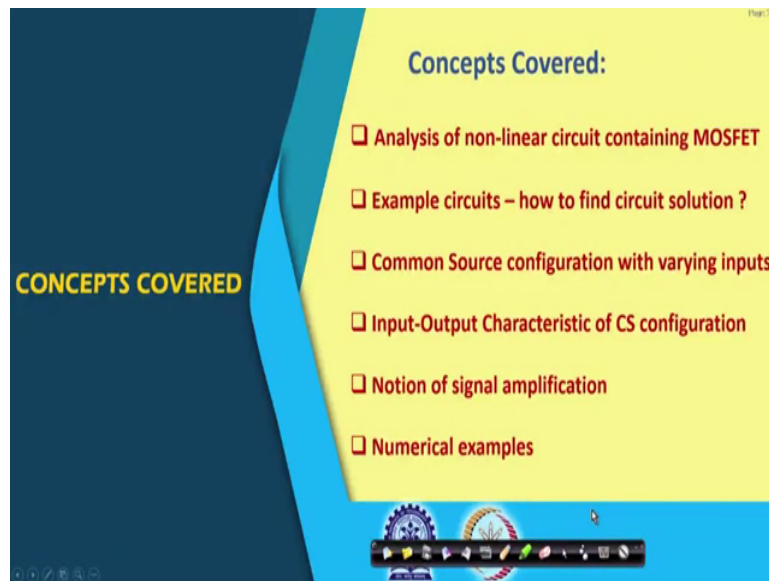
Lecture – 16
Analysis Of Simple Non–Linear Circuit Containing a MOSFET

Start sir.

So, dear students welcome back to this Analog Electronics Circuit. Myself Pradip Mandal from IIT Kharagpur, I am associated with E and ECE Department of the institute. So, we are going through the second module and so, it is continuation of that namely we are going through Analysis of non-linear simple non-linear circuit containing BJT and MOSFET.

In the previous sub-module we have seen that the circuit containing BJT how to analyze it and today we will be going to similar kind of analysis, but containing MOSFET, and we will also see what will be the difference. So, let us see what are the things we are planning to cover today.

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So, first we will cover the basic circuit configuration. As I said that it will contain only one transistor and then through two examples we will see how we can find the circuit solution; namely, the circuit current and voltage.

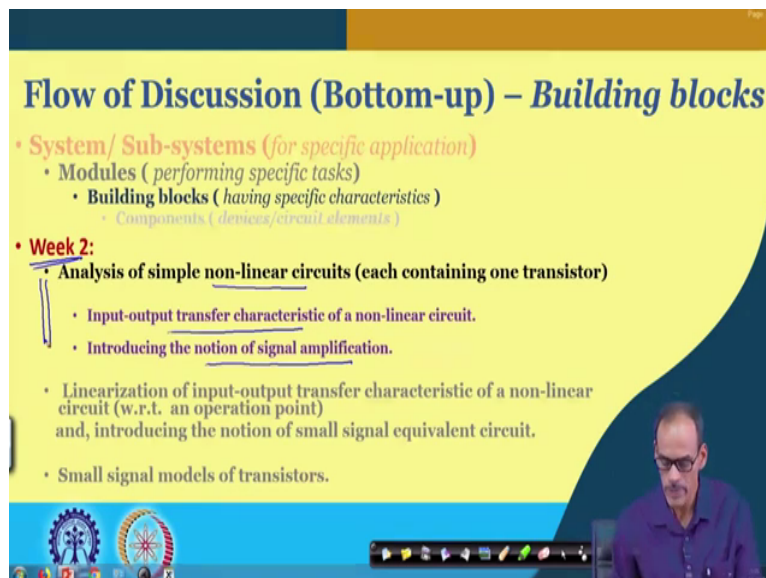
And then, further we will be going through the example and in fact, incidentally that that example it is common source amplifier where the source is common for input and output. And, we will be seeing that what will be the output for varying inputs and then from that we will be giving a giving any thought towards what may be the output variation whenever we are changing the input. So, in other words input to output transfer characteristic of the circuit.

And then, if we change the input in a regular pattern or maybe through some signal then you can see at the output. What kind of signal they associated signal we can get at the output namely, if we give a signal at the input of the common source configuration. What kind of

signal we are expecting at the output namely, we are expecting amplified version of the signal.

And then, we do have a plan to cover some numerical examples, if time permits we will go a little detail of that otherwise, probably we can give some hint and then you can work out those numerical problems. So, according to our overall plan of this course this schedule let us see where we are.

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The slide is titled "Flow of Discussion (Bottom-up) – Building blocks" and is set against a yellow background with a blue wave-like shape on the right. It lists the following topics:

- **System/ Sub-systems (for specific application)**
 - **Modules (performing specific tasks)**
 - **Building blocks (having specific characteristics)**
 - Components (devices/circuit elements)
- **Week 2:**
 - **Analysis of simple non-linear circuits (each containing one transistor)**
 - Input-output transfer characteristic of a non-linear circuit.
 - Introducing the notion of signal amplification.
 - Linearization of input-output transfer characteristic of a non-linear circuit (w.r.t. an operation point) and, introducing the notion of small signal equivalent circuit.
 - Small signal models of transistors.

The slide also features a small inset video of a man in a purple shirt and glasses in the bottom right corner, and a Windows taskbar at the bottom.

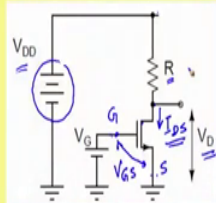
So, in this module namely week 2 modules, we are going through this non-linear circuit containing only one transistor and as I said that previously we have covered circuit containing one BJT. And, today we will be going through similar kind of circuit containing MOSFET one MOSFET and the overall plan as I said that to find the input-output transfer function and then also how the circuit can amplify a signal.

So, in other words how this the circuit simple circuit containing one transistor can amplify signal. So, this is what the plan and has said that compared to previous days. It will be the transistor instead of BJT will be going through MOSFET and whenever it is appropriate. We may also discuss about the difference between the circuit containing BJT versus circuit containing MOSFET.

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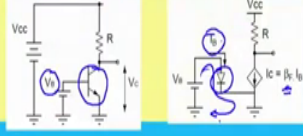
Analysis of a circuit containing MOSFET

• **Example circuit_1**



$$I_{DS} = \frac{\mu_n \epsilon_{ox}}{2 t_{ox}} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda_n V_{DS}) \quad V_{DS} \geq (V_{GS} - V_{th})$$

CE as reference:



So, let us see the basic circuit configuration. So, here we do have the example circuit, we called example circuit 1 and you see where we do have supply voltage. Main DC supply voltage V DD which is giving supply to the drain of the transistor through register R normally referred as load and at the gate we are applying V G.

And, we are assuming that the device it is in saturation region which is equivalent to active region of operation of BJT; namely, in the channel if you see the drain end the channel pinch

off it is happening. And if that condition is satisfied, in other words if V_{DS} is more than $V_{GS} - V_{th}$ then the pinch off is happening at the drain end.

And, then the expression of the current I_{DS} of the device can be given by this formula where $V_{GS} - V_{th}$ square it is having important role and in this circuit this V_G incidentally that is also same as V_{GS} . And if the device it is in saturation region then the current is having very weak dependency only through $1 + \lambda V_{DS}$ part which it is commonly known as channel length modulation factor.

On the other hand depending on the aspect ratio of the device W by L of course, it is having good influence on the current and the remaining part particularly $\mu \epsilon / t_{ox}$ this part it is you may say that is a device constant. So, we may say that this is simply a constant key.

Now, if you compare; if you compare the common emitter amplifier circuit which is similar to on this circuit common source amplifier, it is and the circuit just for your reference which it has been discussed previous class; I am also showing the circuit. And, here we will try to see that once the circuit is given how do you find the current here of course, the current equation is given here and then subsequently how do you find the drain voltage or V_{DS} or in this circuit incidentally that is the output voltage.

So, if you compare the common emitter configuration based on the bias condition at the base we are suggesting to analyze the base loop to find the base current. Whereas, for this circuit since the current is not flowing of course, this model it will not work and of course, the dependency of this I_{DS} on V_G or V_{GS} it is different from the BJT circuit.

So, let us see what kind of equivalent circuit we should be using and how this equation it is playing important role. In fact, this circuit as I said that we do not have any notion called beta of the transistor as we have seen for BJT instead the V_{GS} . V_{GS} it is directly controlling the drain to source voltage, and hence, this equation it will be directly used.

Whereas, for BJT what you have done is that we have analyzed this circuit, then diode we have replaced by its simplified linear model by whatever V_{BE} and then its equivalent resistance and so and so to find the I_b and then we have used this beta.

So, in this case; however, this part it is quite different. But of course, once you find the I_{DS} then finding the output voltage using the load line characteristic that is similar; that is similar to the discussion we made for the circuit containing BJT. So, let us see what is the model we use for this circuit.

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Analysis of a circuit containing MOSFET (Contd.)

• **Example circuit_1**

$$I_{DS} = \frac{K_n}{2L} (V_{GS} - V_{th})^2 (1 + \lambda_n V_{DS})$$

$$V_{DS} \geq (V_{GS} - V_{th})$$

$\lambda_n \approx 0$ ✓

CE as reference:

$I_C = I_E$

And here again just for your reference I am keeping the model corresponding to CE amplifier here and of course, this is our main circuit of our consideration. So, here as I said that this gate voltage it is forming or providing the V_{GS} . So, this is directly coming to the gate, but

then source at the source we do have 0 voltage. So, we can say V_G is nothing, but V_{GS} and depending on this V_{GS} drain to source current is flowing.

So, we can say that this device it can be modeled as voltage dependent current source and so, we do have this I_{DS} is function of V_{GS} and also the V_{DS} . So, this is the drain and this is the gate, this is the source and whatever the voltage you do have across this output port it is actually the V_{DS} .

So, the current flow here it is it depends on the V_{GS} as well as V_{DS} and we know its expression just now we are talking about it is K divided by 2. K is the trans conductance parameter coming from the device multiplied by aspect ratio of the channel multiplied by $V_{GS} - V_{th}$ square multiplied by $1 + \lambda V_{DS}$, assuming that this condition is getting satisfied namely the device it is in saturation.

So, once we get this the current definitely then we can see what may be the corresponding voltage here. By considering the, this part and this part together namely their characteristic, we can combine to find the output voltage as you have done for the BJT similar kind of approach we will be following.

So, once the circuit is given to us namely not only this voltages are given we are also assuming that the corresponding device parameter namely, V_{th} then K and then maybe the λ all are given. And here of course, in this module simplified module we have assumed that this λn is very very small namely, you may say that approximately 0.

So, this factor dependency of this current on V_{DS} you can say practically 0. So, that is the assumption. Later on we will see that this approximation may be important only for DC, but once you go for ac signal this may be very vital we may have to consider that part. So, to find the operating point or to find the solution point for given condition what are the steps we need to follow. So, let see what are the steps we need to follow in the next slide?

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Analysis of a circuit containing MOSFET (Contd..)

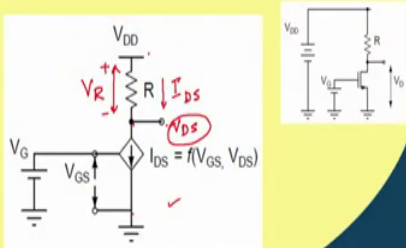
• **Example circuit_1 (contd..)**

Steps to follow:

1. Find, I_{DS} :

$$I_{DS} = \frac{K W}{2 L} (V_{GS} - V_{th})^2 (1 + \lambda_n V_{DS}) \quad \checkmark \approx 0$$

2. $V_R = R \cdot I_{DS}$
3. $V_{DS} = V_{DD} - V_R \quad \checkmark$



The diagram shows a MOSFET circuit with a drain resistor R connected to VDD. The gate is connected to VG, and the source is grounded. The drain current is IDS, and the drain voltage is VDS. A smaller equivalent circuit is shown to the right.

So, here we have written that this is the; this is the equivalent circuit. So, this is the at this point we do have the V_{DS} and we also assume that this part it is very small. So, we do have only this current which is function of V_{GS} alone and so, the first step it is we need to find the I_{DS} and then next one it is we can find the drop across this register while this current is flowing through this register.

So, we can say that applying KCL here at the drain node the same I_{DS} current is flowing through this register creating a drop across this register called say V_R which is having this side plus and this is minus. So, second step it is; so, it is basically I_{DS} multiplied by R it is giving us the drop across this resistance.

Now to find this V_{DS} which is V_{DD} minus this drop. So, that is the third step and, following this one we can find the circuit solution namely the current and the corresponding

voltage here. It is in fact, this procedure or from this whatever the steps we seen it is it can be viewed as more generalized approach and graphically it will be very interesting to see though actual circuit numerical solution we may be following this one.

But, many a times graphical representation may help you to understand whether the circuit will be providing meaningful performance; namely, gain or whether it is gain is sufficient, and under what condition the signal swing it will good or the signal will not be facing much distortion. So, to appreciate all these qualitative things it is better to understand the these steps in graphical way also.

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Analysis of a circuit containing MOSFET (Contd...)

• **Generalized method (graphical illustration)**

Steps to follow:

1. Combining Pull-dn and pull-up chars
2. Rearrangement of pull-up char
3. Superposition of Pull-dn and rearranged pull-up chars .

$I_{DS} = \frac{K W}{2 L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$

So, in the next slide what we are going to discuss is the generalized method. In fact, this method we have discussed for the BJT circuit as well. So, let see what are the steps we are following here, first step it is of course, we need to find the I DS. So, that is we have to use

this equation and the next thing is that we need to find this voltage we need to combine the characteristic of the upper element and the lower element.

And as we said in the previous class that we let we call this is pull up element pull up element and this one it is pull down element; So, we do have the pull down element. And, if we combined say pull up and pull down characteristic namely, the voltage across this one and their current need to be consistent and then we can find the solution point.

So, pull down element characteristic you may recall that similar to the BJT circuit. The if we plot the I_{DS} ; I_{DS} versus V_{DS} for a given value of V_{GS} and as you said that λ is very small. So, we can say this current is practically independent of this V_{DS} . Assuming that the pinch of it is happening; that means, we are not entering into this triode region we are keeping the device in the saturation region.

So, this portion it is saturation region which is equivalent active region of operation of BJT and then the pull the pull up characteristic; that means, the load line characteristic it is of course, it is linear. So, if we draw the current through this register I_R versus voltage drop across this resistance. So, the V_R is the voltage drop across this resistance and I_R is the current flow through this resistance.

And we know that if we plot this I_R versus V_R , this will be linear and slope of this linear line it is $1/R$ with a minus sign and so, if we combine these two characteristic then they will be giving us the solution. But, since the x-axis this is V_R and then here we do have V_{DS} , they are not same, in fact V_R if you see here it is nothing, but V_{DD} ; so, $V_{DD} - V_{DS}$.

So, since these two axis they are not consistent even though finally, we want this I_R and I_{DS} should be equal, but these two definitely we do not want equal, because rather it will be V_R should be V_{DS} . So, since we cannot directly combine these two characteristic we need to change this characteristic, what we call it is we rearrange this pull up characteristic and then we do the superposition.

So, similar to the BJT circuit what you do, first we flip this characteristic namely we plot the I_R versus $-V_R$ characteristic which is equal to $V_{DS} - V_{DD}$. So, that gives us the characteristic of the register it is going to the second coordinate.

This slope sorry, this will not be minus this will be plus, here the slope here it will be $-1/R$ and then this axis of course, it is having V_{DS} with plus sign here, but still we do have the $-V_{DD}$ part. So, to get rid of this one what we do we further rearrange this characteristic namely we plot I_R versus $V_{DD} - V_R$. So, that is of course, it becomes equal to V_{DS} .

So, now of course, if you plot this characteristic this characteristic it is getting shifted by V_{DD} amount to the right and so, this is getting shifted here. So, the origin it is getting or rather at this point of the characteristic curve touching the origin is getting shifted here to V_{DD} and the slope here of course, it remains $-1/R$.

So, considering this point and this slope what we are getting here it is V_{DD}/R that yourself can find it, and now this I_R to satisfy KCL at this point I_R need to be equal to I_{DS} and this axis of course, it is V_{DS} . So, now we can superimpose the two characteristic curve. So, this is the characteristic of the load line and its slope it is $-1/R$. So, wherever and also this point is V_{DD} and wherever they are intersecting we call the solution point or the operating point.

Now, so this procedure as I said it is very similar to the circuit containing BJT. If you see so far, we are talking about the circuit containing a MOSFET, but this MOSFET is a special kind of MOSFET or rather I should say it is n-type. In case if you are finding a circuit containing PMOS transistor then of course, the situation you need to adjust yourself; so, that whatever the technique we have we are following here that can be deployed.

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Analysis of a circuit containing MOSFET (Contd....)

- **Common Source (CS) circuit**
Any change with resistance at the gate bias ?

The slide contains two circuit diagrams and a handwritten equation. The left diagram shows a PMOS transistor in a common source configuration. The gate is biased with V_G through a resistor R_1 . The input is V_{in} and the gate current is $I_G = 0$. The drain is connected to V_{DD} through a resistor R_D , and the output is V_{out} . The drain current is I_{DS} . The right diagram shows an equivalent circuit where the gate is connected to V_{in} through a resistor R_1 . The gate voltage is V_{GS} and the drain current is I_{DS} . The handwritten equation is $I_{DS} = \frac{K W}{2 L} (V_{in} - V_{th})^2 (1 + \lambda V_{DS})$.

So, let us see an example having p MOS transistor sorry, before you go to PMOS, I sorry I do have another case to discuss in comparison with BJT. What is this one is in case we are having input voltage and then if it is having a resistance in series with that. So, let we call this is say R_1 and then so, this is same as whatever V_G and whatever the analysis in this case can we deploy or how do we find in this the I_{DS} and the V_{DS} for this circuit.

In fact, if you see here since gate DC wise gate through the gate the current is 0 so, we can say I_G is practically 0, even though we do have this resistance the drop across this resistance is 0. So, we can say that whatever the voltage you are applying V_{in} it is directly coming to the gate and if you see the if we draw the equivalent circuit of the transistor. What will be finding is that this register practically is not having any effect to the operating point.

So, whatever the voltage you are applying here even though we are applying through this register see R_1 so, and let you call this is whatever I say V_{in} and since this current is 0. So, since I_G equals to 0 at least DC wise that is valid. So, the drop across this resistance is V_{R_1} equals to 0.

So, we can see that the voltage from the drain sorry, gate to source of this device namely this V_{GS} ; V_{GS} equals to same as this V_{in} . So, as a result; as a result whatever the whatever the I_{DS} equation we are using we can directly use that I_{DS} equals to K divided by 2 W by L into V_{in} V_{GS} equal to V_{in} minus V_{th} square into whatever 1 plus λV_{DS} and all these things, but anyway we have considered this part is approximately 1 . So, whatever the equation we do have here, it is essentially saying that this register is not having any role to play.

However, if we are considering a signal you are applying here the gate to source there will be capacitance. So, then for signal of course, this register it will be having some role to play. So, that we will discuss later, but for the time being at least you can say that if you are having a register here the DC condition wise it is not having any influence.

In fact, this is a contrasting difference compared to the compared to the BJT circuit where if you put a register and then if you put say V_{in} to bias the base of the BJT, then we know that then the current flow; current flow through this circuit it will be affected by this resistance. And so, this V_{in} even though we are applying V_{in} here the V_B it will not be same as the V_{in} because there will be a finite drop across this resistance. So, this drop it will be non-zero.

So, that is one important difference of the while you will be analyzing the circuit containing MOSFET and circuit containing BJT and of course, later part it is this part it will be same further two cases. And let us see as I was giving a hint that so far we are discussing about the circuit containing n-MOSFET, n-type MOSFET or rather n channel MOSFET in case if you are experiencing a circuit which is having p-MOSFET then what do you do.

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Analysis of a circuit containing MOSFET (Contd.)

• **Example circuit_2**

$$I_{SD} = \frac{KW}{2L} (V_{SG} - |V_{th}|)^2 (1 + \lambda_p V_{SD})$$
$$V_{SD} \geq (V_{SG} - |V_{th}|)$$
$$V_{out} = V_R = V_{DD} - V_{SD}$$

The slide also features a small video inset of a man in a purple shirt in the bottom right corner and a Windows taskbar at the bottom.

So, here we do have an example. So, in this case the this is the transistor of our consideration its source is connected to V DD. In fact, need not to call V DD it is connected to source, but whatever the name you are giving it does not matter as long as this is at high potential at least compared to the gate and creating a voltage drop here sufficiently high. So, that the device it is on that is good enough.

Just for our consistency, we are naming this one V DD. So, you may you may not be sidetracked by that, but after that once you apply the voltage at the gate by the other source then how do you find the corresponding current through this device. Now, if you replace this device by its corresponding model here, what we have it is the; so, this is the source in this case, this is the source, this is the gate and this is the drain and we are expecting the current it will be the actual current it will be flowing from source to drain.

So, we may call this is I_{SD} and we are expecting that V_{SG} should be higher than threshold voltage of the transistor magnitude of the threshold voltage, and also at the drain end to have the pinch of happening we need to satisfy V_{SD} should be higher than V_{SG} minus V_{th} .

So, once we satisfy this condition then the expression of this current is given by K by 2 W by L V_{SG} minus V_{th} square multiplied by 1 plus λ into V_{SD} . Again just for simplicity, we may consider this is approximately 0 , but the rest of the things it is very similar to whatever we have discussed. Only difference is that the source is connected to the supply V_{DD} , gate is connected to at lower potential and then of course, drain it is preferably.

In fact, it is lower than the source voltage and preferably this drain voltage should be such that the pinch of it is happening namely, the channel is not appearing. In other words the drain voltage should not be higher than gate voltage by a margin of magnitude of the threshold voltage. So, that is the condition we are writing here.

And once it is done once the this condition is getting satisfied then you can see what is the V_{SG} namely, V_{DD} minus V_G in this case this is V_{DD} minus V_G so, that is the V_{SG} . So, we can say in this case this is V_{DD} minus V_G and so, that voltage we can plug in here and then you can find this current, and this current is of course, it is flowing from source to drain, this current is also flowing through the register or load.

So, we can you may call this is I_R which is equal to I_{SD} and that is producing a drop across this register called V_R , and then this V_R incidentally this is same as the output voltage. So, you may say that V_{out} is same as V_R equals to V_{DD} minus V_{SD} . So, of course, if you see the circuit, it will be relatively straightforward to follow, but then there will be a difference of whatever the generalized methodology we have discussed. So, let us see what kind of changes it will be there in that generalized methodology or whatever we see graphical interpretation of the steps.

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Analysis of a circuit containing MOSFET (Contd...)

• **Generalized method (graphical illustration)**

Steps to follow:

1. Combining Pull-dn and pull-up chars
2. Rearrangement of pull-up char
3. Superposition of Pull-dn and rearranged pull-up chars.

$$I_{SD} = \frac{K W}{2 L} (V_{SG} - |V_{th1}|)^2 (1 + \lambda_p V_{SD})$$

So, let us try to see what kind of things we have to do here, first of all again we may call this element and this element they are trying to adjust themselves to converge to a point where this V_{out} . It is consistent for the upper element as well as consistent for lower element and this V_{out} of course, and this V_{DD} minus V_{out} that is nothing, but the V_{SD} .

So, since the device it is in saturation region you may say that this current again it is primarily defined by V_{SG} and this part it is approximately one, but then the main the change here it is now we will be calling this is as pull up and this element as a pull down element. So, this is the pull down element.

So, then while will be rearranging the characteristic which one do we rearrange. Interestingly, V_{out} is this one; so, first thing is that let us draw the and the pull down characteristic first.

So, we do have the pull down characteristic namely I_R versus V_{out} and incidentally that is the drain voltage and we know that this is a linear element. So, we draw this one.

Now, if you consider the pull up element on the other hand. So, we know that pull up element is basically I_{SD} versus V_{SD} , and the V_{SD} what we said it is V_{DD} minus V_{out} . So, this is equal to V_{DD} minus V_{out} . Now, again this V_{out} and this V_{out} they are same, but then this axis and this axis they are not consistent. And of course, they are the characteristic this is the pull up characteristic, if I ignore lambda part it will it supposed to be quote and unquote independent of the V_{DS} or V_{SD} , but then this axis we want this should be equal, but then the x-axis parameter they are not same.

So, what you have to do we have to rearrange what we said we need to rearrange this pull up characteristic incidentally now this is non-linear in nature. So, it is bit tricky. So, first thing is that we need to flip it. So, let we flip and let the characteristic is going to the second quadrant and the characteristic it becomes like this, it is going to the second coordinate. So, this is I_{SD} versus minus V_{SD} or whatever you say V_{DS} , but then this is equal to V_{out} minus V_{DD} .

So, again we do have V_{out} , but still we do have minus V_{DD} . So, to adjust that what you have to do we have to shift this characteristic towards the right by an amount of V_{DD} . So, if you do that then the characteristic it is getting shifted. So, now, I_{SD} versus V_{DD} minus V_{SD} . So, that is of course, this is equal to V_{out} and since we are adding this V_{DD} part. So, this characteristic curve it is getting shifted to right by an amount of V_{DD} . So, you may say that this is the V_{DD} part V_{DD} point; so, V_{out} is equal to V_{DD} here.

So, what are the things we have done is that we have flipped it and then we have shifted right and now this took axis this axis and this axis they are same. So, now, I can overlay this characteristic on the pull down element namely the characteristic it becomes like this. So, we do have the V_{DD} here and wherever they are intersecting we call this is the operating point.

So, that is I think the method it is remaining same only thing is that you need to be comfortable to rearrange this pull up characteristic even though it is not linear and incidentally the pull down characteristic it is linear. In general, so, you should be comfortable

even if say both the elements pull up and pull down elements they are non-linear in nature.
So, let me take a short break and then we will come back to the subsequent point.