Digital Circuits
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Lecture – 49
8085 Microprocessor
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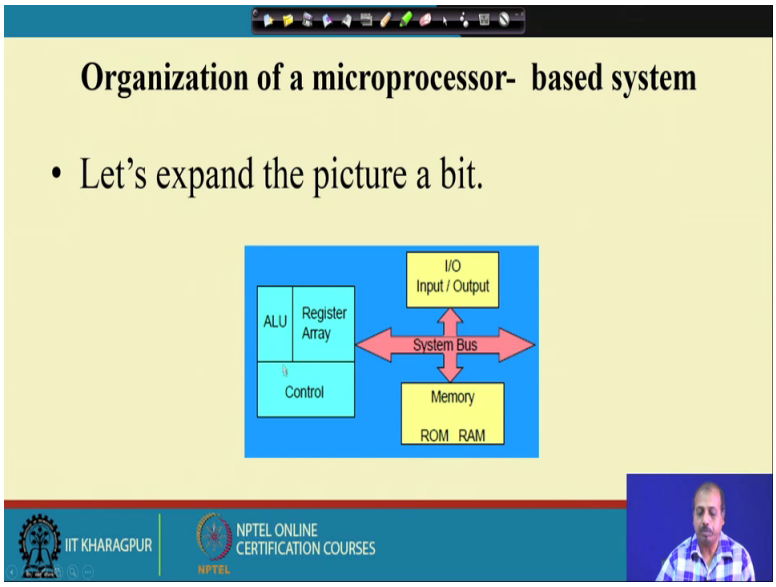

So, if we expand this microprocessor structure or system structure, then it consists of the modules. Like, if this is the microprocessor that we have consisting of this ALU the register array and the control.

Then we have got this memory and I O. So, they are that are the other parts that we will have in the system and they are connected by means of some bus. So, which his known as the system bus. So, through this system bus this processor, the microprocessor will talk to the memory will also talk to the input output devices.

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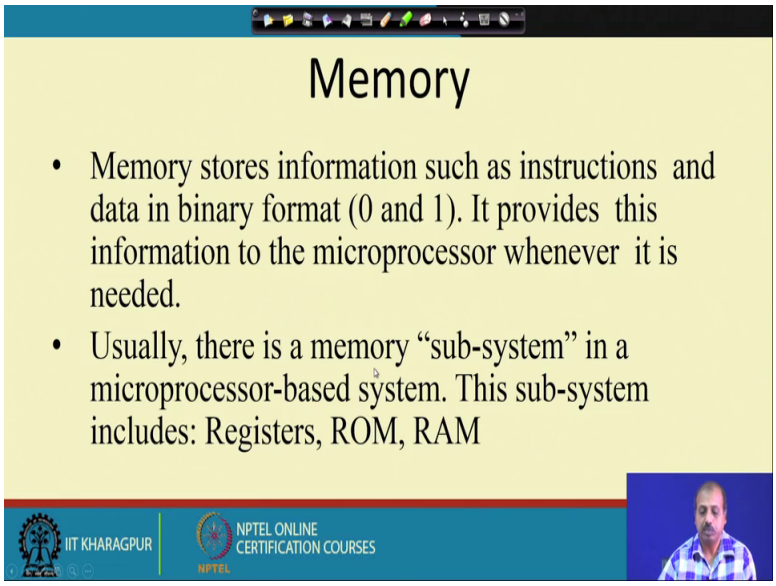

Now, under this, we have this memory will first look into this memory the part that we have and memory is nothing but a storage. So, it stores information such as instructions and data in binary format and it provides information to the microprocessor whenever it is needed. So, this is basically some storage that we have.

And as I said that when we compile a program and then load it into the memory. So, this memory is holding that program. So, like that it is a storage part. So, memory is a we talk about memory as a subsystem and in this subsystem; we have got registers ROM and RAM. So, registers are part of the CPU so that is inside the microprocessor, but this ROM and RAM. So, they are outside the microprocessor and they are as a separate chips ok. So, they are microprocessor actually talks to this ROM and RAM by means of that system bus that we have seen but from the angle of storage.

So, all these modules registers ROM and RAM. So, they are storing some information. So, we will put them under a broad heading of memory subsystem. So, in the memory subsystem all these information are stored, and then it can get the information the processor can get the information from that part.

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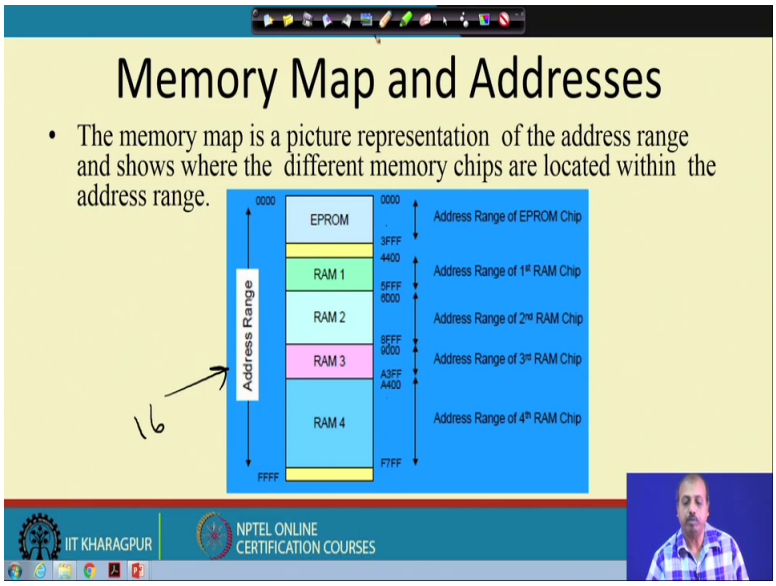

So, next we will be talking about an important concept which is known as memory map and address. So, as I said that a memory is nothing but a memory is nothing but some storage.

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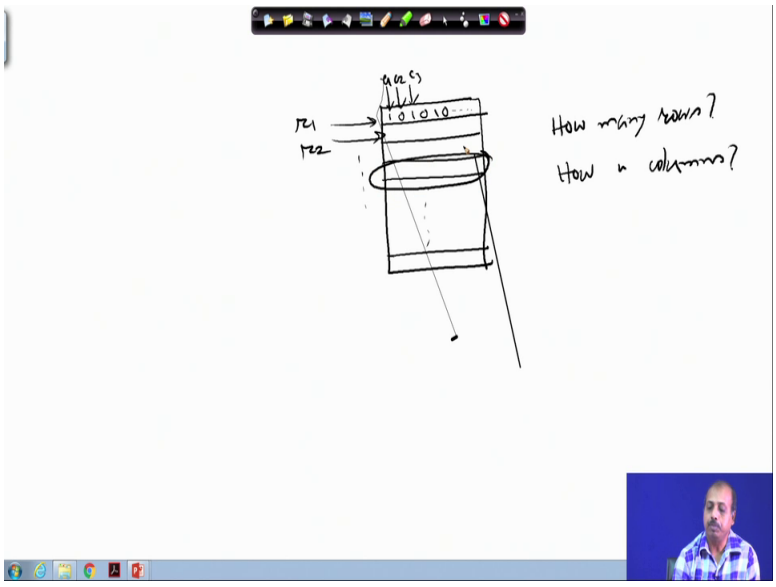

So, this is the storage then there are 2 questions to be answered like how are you storing information there. So, we I have said that this is in terms of 0s and 1s. So, these are the individual locations that I have individual rows that I have of 0s and 1s.

So, how many rows are there and how many columns? So, I can say my question is how many rows and how many columns. So, in individual column; so, this may be storing the parallel bit pattern 1 0 1 0 1 0 like that ok. So, these are the column. So, this is the first column, this is the second column this is the third column like that.

Similarly, so, these are the columns C 1, C 2, C 3, etcetera and these are the rows. So, this is the row 1 this is row 2 ok. So, like that. So, whenever I am trying to access this memory. So, it is always done in terms of rows ok. So, normally we do not access memory in terms of these individual bits or in terms of column. So, we will be always accessing a particular row together. So, we will always be accessing a particular row together ok. So, it is never that.

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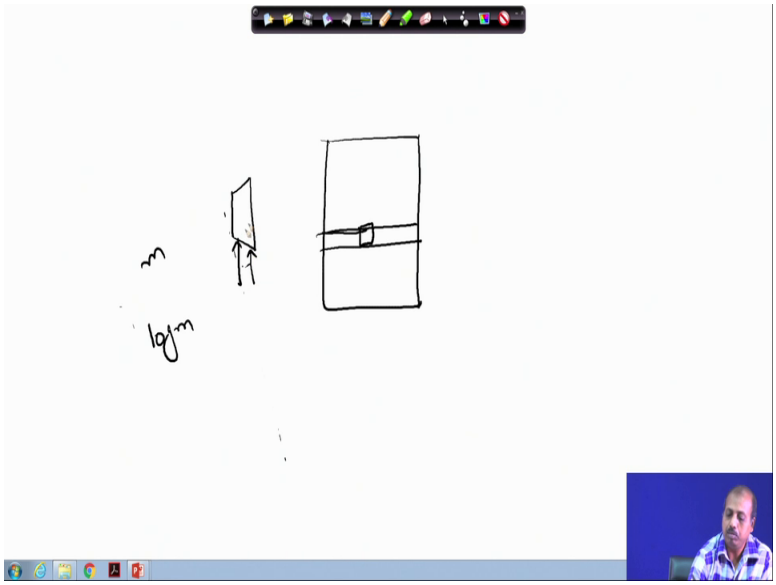

We access a particular bit within a memory say, it is not that we access a single bit separately ok. So, it is not done. So, this entire row is entire a this entire row is accessed by the processor.

Now, if I if this if I have got say m rows then somehow the processor need to tell like which row it wants to access fine; so to tell that it needs to; so, if there are n such rows. So, to identify any row here; so, I will need log of m, I will need log of m number of bits to be specified. So, what I can do. So, I can have a decoder where I can say. So, I can put a decoder and the decoder will be the decoder can find out like where to which location I

am talking about. So, it is like this that if I put a decoder here and then here I tell what is the here I put that log n bits better, I can I should make a different notation.

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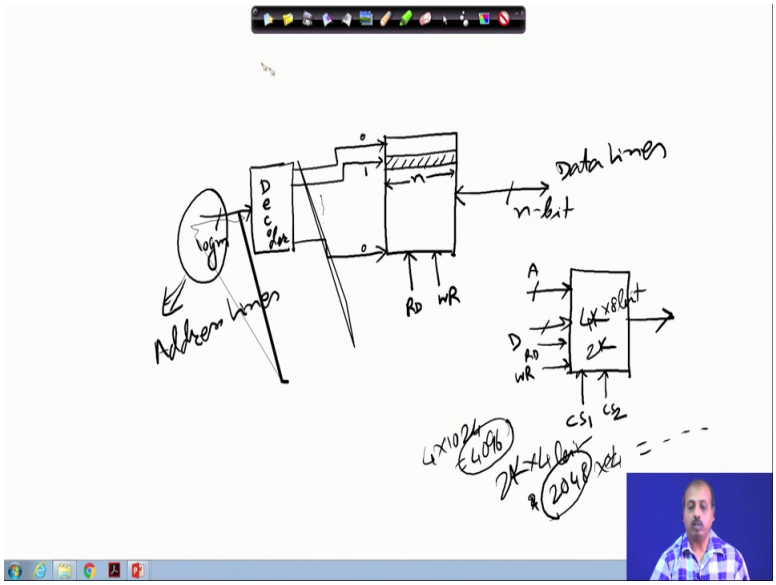

So, this is my memory block that I have and this is the decoder.

So, here I am feeding log m number of bits as a result this decoder generates m such enable signals, it generates m such enable signals and depending upon at the value that I have given here. So, one of these lines will be enabled and rest are all disabled. So, may it may be that it has enabled it, it has put this line as 1 and all these lines are at 0 as a result. So, this particulars row of the memory will be accessed.

So, if we look into a memory chip, then we have got this login lines coming as input one input and this is commonly known as the address lines. So, in the address lines, you need to tell which row, you want to access and as I said that all these location, all these bits. So, they are available at the output of this memory chip. So, this is output. So, if this is if the number of columns here is n the number of columns here is n, then at this point, I get an n bit output and this n bit output. So, they are known as the data lines they are called data lines, fine.

Now, if it as we know that if it is a ROM, then I can put the; I can give it address and I can tell it I can give it the signal read. Accordingly, this content will be available here on the other hand, if it is a RAM, then there are 2 controls read and write. Now if I am

trying to read the content, then I will give the read signal put the address here, if I am ask to trying to write something onto to the location, then this line is bidirectional in case of RAM, then I put the value onto the these data line. So, put the address here and then you give a write signal. So, that whatever value is available on the data line gets written onto the location.

So, this way, we this is the generic structure of a memory of a memory block. So, we can say that it is like this it has got the address lines or a it has got the data line or D and it has got some control line. So, it has got this read and write controls and also many of this memory chips. So, they will have some chip select signals CS and they may there may be multiple such CS chip select signal CS 1 CS 2 like that.

So, and each this memory chip has got some capacity like it may be say 4 K, it may be say 2 K. So, this is that is 4 K that identifies it is 4 kilobyte 4 kilo such locations are there. So, if it is 4 K into 8 bit; that means, individual locations are 8 bit Y and there are 4 K 4 K such that is 4 into 1024 that is 4096 locations are there in this chip.

Similarly, if it is 4 K by it is 2 K by 4 bit. So, this is 1024 into 1024 into 2 K by 4 bit. So, this is 2048 rows and each of 4 bits. So, total whatever be the number of bits coming. So, that is the total capacity of this, but this is this has this has got 2048 locations compared to 4096 location here. So, this 2 K chip will have 4 G or 2048 watts in it.

Anyways so, that we have seen in the while discussing about this memory chips and all. So, in the context of microcon processors what happens is that every microprocessor will have certain number of address lines and a certain number of data line. So, it will be coming from the microprocessor itself and they are they those lines are fixed ok. So, if a microprocessor has got m address lines, then it can access 2 power n memory locations from that and it has got a in the end data lines will tell that the memory chip that we gone to connect. So, to provide me n bit data at a time.

Now, depending upon the structure depending upon the depending upon the chips that we are connecting and then we can have different type of connection. For example, you may say that the this the total address range of the microprocessor like here it is said that ok; I have got this is running from 0 0 0 0 to F F F F. So, this is through if the microprocessor has got 16 bits address line because it is F F F F. That means, it is now all the 16 bit value. So, this has got 64 K alternative alternate values in the address range.

So, my microprocessor address bus the address lines that the microprocessor generates must be 16 bit and then using that. So, it will be able to distinguish between any of this 64 K locations, but the memory chips that we have. So, they are that memory chips may not be having a 64 K capacity in a single chip ok. So, they are so, I will need multiple such chips also I need to distinguish between some part of the um some part of the system. So, if the some part of the program may be fixed whereas, some part are varying.

So, for example, the operating system part of the program of the system. So, that is fixed so that we need to have in some part of the memory. So, normally what is done is that at the beginning of this address range. So, we have got this we try to put one EPROM and in this EPROM. So, we put the operating system part and then in the later part. So, we try to put the RAM chips ok. So, where for that is for the in for access for it to be used for different purposes for storage purpose.

So, the first RAM chip that is shown here so that will be ranging over the addresses 4 3 0 0 2 5 f f f in the second one, so that will be ranging from 6 0 0 0 to 8 f f f; so their capacities are not same, but in a general design. So, their capacities may be same also depending upon the RAM chip that we put and between this EPROM and this RAM 1. So, there is some space which his not utilized. So, this address range that is the 4 0 0 0 to 4 3 f f so that part of the address. So, that is not used by the process by the processor ok. So, there so, it is assumed that the processor will not generate any address in that range. So, if it generates then the system behavior is unpredictable.

However similarly towards the end so, it generates address up to X 7 f f and it does it. So, up from f 8 0 0 to f f f. So, this address range is never generated by the processor. So, it is assumed like that whatever program we will be loading into the memory execute the processor will be executing, it will never generate addresses in the range 3 f 3 4 4 0 0 0 2 4 4 0 0 4 3 f f and similarly from f 8 0 0 to f f f f. So, it will not generate any address in that range

Anyway otherwise, we can connect it like this now how do you make this connection. So, you are as said that if a if this is this is the address lines that we have. So, here I have got 16 address the 16 address lines coming here and how this address lines are going to select this individual chips ok. So, that has to be seen. So, we will take an example and try to explain that part.

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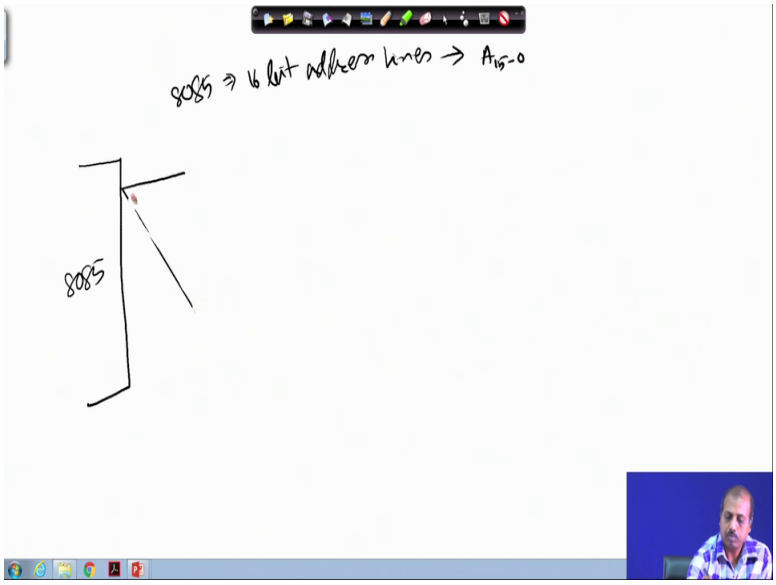

So, suppose I have um. So, in my in my in the 8085 based system that we have. So, it as said that it has got 6 16 bit address lines suppose 16 bit address lines are named as say A 0 to a 15. So, they are named as a A 15 2 0 where A 15 is the highest the most significant bit and A 0 is the least significant bit.

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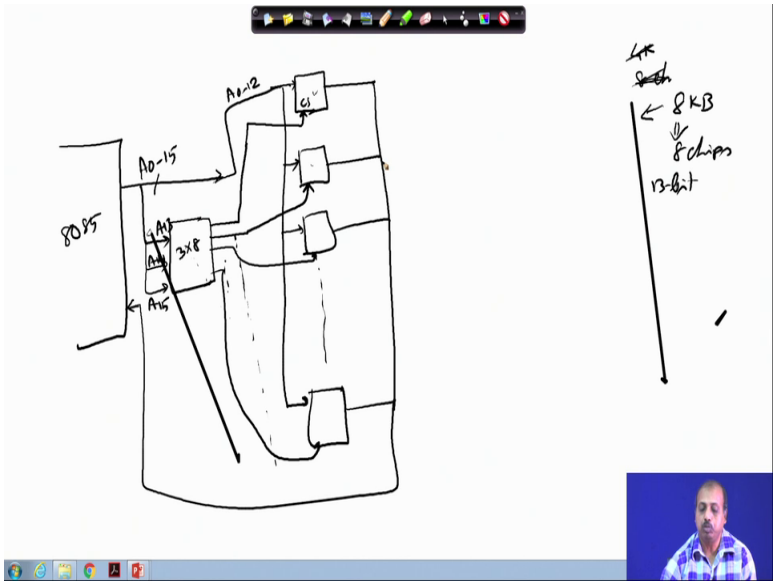

So, from my 8085 chip; so, if this is a 8085 chip. So, these 16 lines are coming out sorry. So, from my 8 0 8 from my 8085 chip is 16 lines are coming out. So, like this now this is my A 0 to 15 that is coming now in my system total 64 K. So, maybe I have got say chips

memory chips of size 4 kilobyte only. So, how do I connect them? So, I will need 8 such chips to sorry I will need say suppose let us take a slightly sized chip suppose, I have got 8 kilobyte chips if I have got 8 kilobyte chips, then for 64 kilobyte I will require A 8 chips in that case ok.

So, what I can do? So, I can I can put 8 I can put 8 such chips in this way 8 such chips in this fashion and for 8 kilobyte. So, for 8 kilobyte the address lines needed is your 10 plus 313 bit. So, 13 bits are the address lines for this individual chips. So, I take this A 0 to A 12 to each of this chips to all this chips we put A 0 to A 12. So, those lines are going there. So, so, so this part is A 0 to 12 and the bits 13, 14 and 15. So, they are fed to A 3 to 8 decoder they are fed to A 3 to 8 decoder and this output line. So, they will be selecting those lines the chips.

So, what I mean is that I have got A 3 to 8 decoder here 3 to 8 decoder. So, the lines A 13 lines A 13, A 14 and A 15, they come here and this is the. So, this first line goes to the first line goes to the ca chip select of the first chip, then the next line will go to the chip select of the next chip. So, like that. So, what I mean is this first line it goes to the chip select of the first chip the second line goes to the chip select of the second chip third line goes to the chip select of the third chip. So, this way the last line will go to the chip select of the last chip.

Then what will happen; any address that is produced; so, if it is in the range of 0 to 8 K first 8 K, then this chip will be selected and this data will be coming out of this chips. Now if I shot all these data lines together and feed it to the data line of the microprocessor feed, it to the data line of the microprocessor. Then this the location the correspond content of the corresponding location will be available to the 8085 one to the data line.

Similarly, if the address generated is between 8 K and 16 K. So, then this chip will get selected and this chip will provide the data ok. So, via this chip select line. So, it is ensuring that now what can happen is that many a times I do not need so many chips ok. So, that is I do not; so, in this case previous example.

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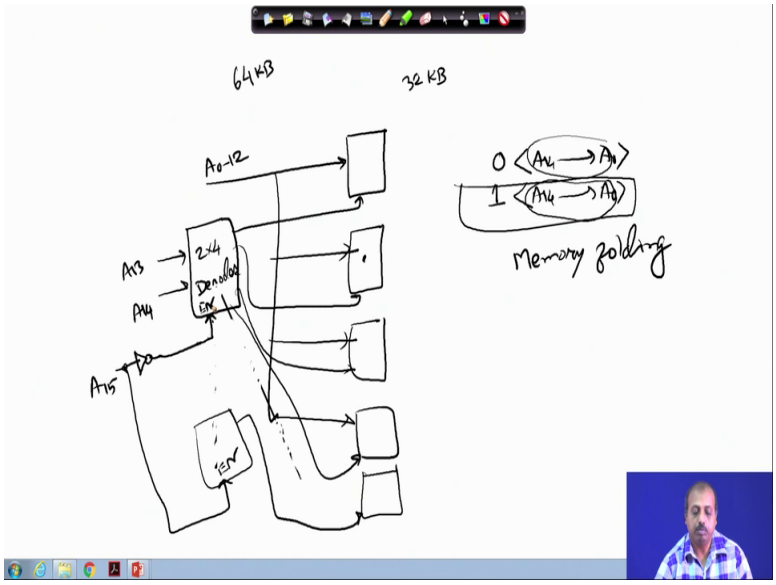

The memory that we connected was also 64 kilobyte in size now it may so happen that I in my system, I need only 32 kilobyte, I do not need others, then if I got say 8 kilobyte chips. So, I will take the this 4 such chips I will take 4 such chips and they will be getting the lines at this lines A 0 to A 12 as we have seen previously. So, they will be getting the line say 0 to A 12. Now for differentiating between 4 chips; so, I will need a decoder which is A 2 to 4 decoder this is A 2 to 4 decoder. So, this decoder it will get the lines A 13 and A 14 from the microprocessor at this lines and then it will be generating the chip select signals for them, they will be generating the chip select signals for the individual chips memory chips.

Now, so, what happens for the address range for the addresses in the range which is which is more than this 32 K; so, here it is implicitly assume that we have got this a thirty. So, A the bit A 15 is A A 15 is taken as 0 and this is the size A 14 to A 0. So, that will determine what we are going to which row which chip we are going to access.

Similarly, this A 15 if this A 15 is equal to 1, then also if you give some value. So, A 14 to A 0. Now suppose these 2 contents are same. So, this content and this content are same. So, you can understand that since this whole design that we have done, it is independent of the B A 15. So, in both the cases, it will access the same location. So, it will so, if the address range A 14 to A 0 is started at it falls into this chip, then in both the cases A 15 equal to 0 and A 15 equal to 1, it will be accessing the same chip.

So, this phenomena is known as memory folding. So, this is known as memory folding that is for the same for different locations. So, you see different addresses it is accessing the same memory location.

So, this may or may not be desirable; so, in some system; so, if the memory folding is there. So, I cannot expand the system because now I cannot put further chips here because the pin A 15 has not been used at all and if you can say that. So, how to how to stop this folding; so, folding can be stopped many a times what are consist that this 2 to 4 decoder. So, they have got some enable line as we know. So, it has got an enable line. So, if it has got some enable, then we can use that enable line to stop this phenomena ok. So, we can put an inverter and connect the A 15 line here; So; that means, when this A 15 equal to 0, then only this enable line will be equal to 1; as a result this decoder output is enabled other otherwise this decoder will be in a tristated state. So, it will not be selecting any of these outputs.

All the outputs will be in 0 state now. So, none of the chips will get enabled. Now if A 15 equal to 0, then only this enable signal is high as a result appropriate memory location will be selected. So, this way; so, this is this address does not have any meaning in this case. So, if A 15 equal to 1, then none of the memory chips will get selected.

So, that location is not within the addressable range generated by the processor in that case. So, that way memory folding can be resolved, but of course, if you are not bothered much, then you can definitely allow memory folding, because if you allow memory folding, then this extra logic gate this inverter and all are not required. Similarly, it may so happen that you can work with a simpler decoder that does not have any enable line in it.

So, you can directly use a chip which is a decoder, but does not use the enable line whereas, in this case you need to use a decoder where it has got a enable line if we are avoiding memory folding, then the advantage is that later on if you want to expand the system by putting another chip here, then you can have another decoder and for that decoder you take the enable line and connect it directly here, fine.

So, and this chip, our this decoder output say give chip select to the lower chip. So, that as a result what will happen is that this block will be selected only when A 15 equal to one. So, you get the addition. So, you do not need to generate; you do not need to expand

this decoding logic by putting by putting a larger decoder, but you can just extend the design you can just put another 2 to 4 decoder here and then by using this enable line. So, you can enable that decoder and the previous decoder. So, it will be valid for the upper 32 kilobyte and this decoder. So, this will be selecting the lower chip.

So, this way for memory expansion purpose it is better that we have got this memory folding resolved. So, that we can we can expand the system later that will not be possible, if we are not using memory folding. So, if we resolve it previously. So, if we have if we allow memory folding then of course, this cannot be done ok.

So, another possibility that we have is that this memory chips. So, it may not have um the data line may not be sufficient for example, may be I will I am I require some memory of capacity say 32 kilobyte ok.

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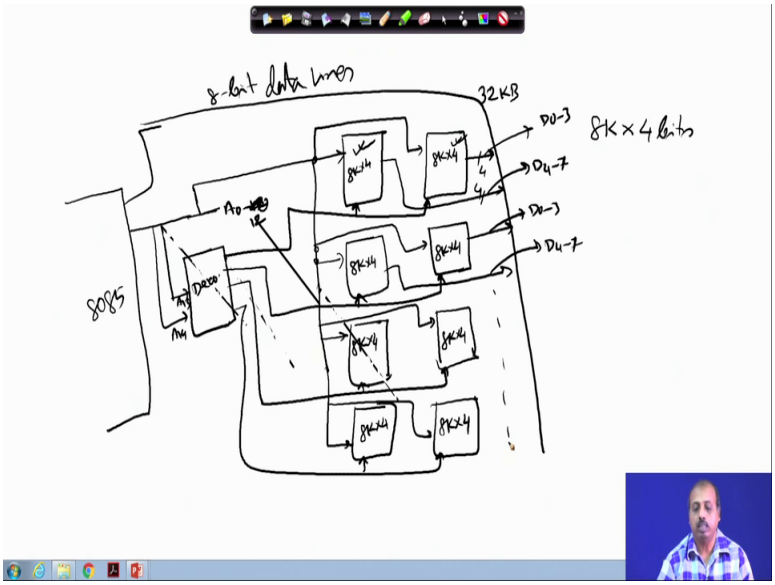

So, this individual chips that I have are say 8 kilobyte, it has got 8 kilobyte location, but 8 kilo locations, but individual locations are of 4 bits wide.

So, this we have seen previously that we have got 8 kilo and 4 bits. So, this is 8 kilo by 4 and this also. So, what you do in that case is you take 2 such chips in parallel ok. So, you have got this is another 8 kilo by 4. So, total 32 K. So, this is 8 kilo by 4 and this is another 8 kilo by 4. So, you take another such chips fine and then from the processor side and. So, this is a 8085 the address lines then the decoding and all. So, this address lines A

0 to. So, 8 K; so, A 0 to A 12; so, they go to individual chips the; so, A 0 to A 12 is connected. So, you are making connections like that.

So, this address lines A 0 to A 12 are connected and then from the decoder if this is my decoder then this is the lines. So, if this is the decoder then we have got. So, this is A 0 to twelve A 0 to A sorry A 0 to A 12. So, this is A 13 and this is a fourteen. So, they are. So, from this I get I generate the decoder signal and this chip select line goes to both the chips ok. So, these chips select line; it goes to both the chips which are in parallel. So, here this one this next chip select line, it goes to both the chips which are in parallel, third one goes to both the chips in parallel and the fourth one again goes to both the chips in parallel.

So, what happens is that if this decoder is selecting one chip. So, this is actually selecting a pair and then for the address bus what we do if this is for the data bus, what we do is that this will give me 4 bits and this will give me 4 bits and they will be connected to the 8 bit output. So, this is suppose this is an 8 bit data bus date 8 bit data lines for the processor. So, first most significant 4 bits will be coming may be from come from this memory and the least significant 4 bits will be coming from this memory.

So, this lines; so, they will be connecting to the data line D 0 to 3 and this lines, they will be connected to D 4 through 7. So, everywhere it is like this. So, this is connecting D 4 2 7 and this is connecting D 0 2 3. So, this way we can make the other connection. So, this way you can make a memory system which is using the basic memory chips of different sizes as we as it is available and then we can connect them in some fashion by means of this decoding logic from the processor to get the full memory system implemented.